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Design and Performance Analysis of Tri-gate GaN HEMTs

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Abstract

GaN-based high electron mobility transistors (HEMT) are promising devices for radio frequency (RF) and high-power electronics and are already in use for RF power amplifiers and for power switches. Commonly, these devices are normally-on transistors, i.e., they are in the on-state at zero applied gate voltage, what limits their suitability for various applications, such as fail-safe power switches and RF amplifiers with single-polarity power supply. Unfortunately, in contrast to GaAs- and InP HEMTs, achieving normally-off operation, i.e., a positive threshold voltage, for GaN heterostructures is difficult due to the high density of the polarization-induced two-dimensional electron gas (2DEG) at the barrier/buffer interface.

For fast RF HEMTs, short gates are required. However, HEMTs with aggressively scaled gate length frequently suffer from short-channel effects caused by a degraded control of the gate over the channel. This leads to a deterioration of the transistors off-state performance (increased subthreshold swing and drain-induced barrier lowering) and on-state behavior (increased drain conductance).

The tri-gate design has recently been applied to MOSFETs and HEMTs to improve the gate control and suppress short channel effects. Experimental tri-gate transistors show excellent down-scaling characteristics, improved performance, and, in particular for GaN tri-gate HEMTs, a significant shift of the threshold voltage toward positive values. On the other hand, tri-gate GaN normally-off HEMTs are still suffering from increased parasitics causing degraded RF performance (particularly in terms of cutoff frequency) compared to their planar counterparts. Improving the RF performance of GaN tri-gate HEMTs by reducing the parasitics is essential, but this requires a deep understanding of device physics and a thorough analysis of the root causes.

In the present work, in-depth theoretical investigations of GaN tri-gate HEMT operation are performed and extensive simulation studies for these devices are

conducted. As a result of these efforts, improved insights in the physics of GaN tri-gate HEMTs are achieved, the potential of this transistor type is assessed, design guidelines are elaborated, and advantageous designs are developed. It is shown that the 2DEG sheet density decreases by shrinking the body width, that the threshold voltage of GaN tri-gate HEMTs strongly depends on the width of AlGaN/GaN bodies, and that solely by decreasing the body width a transition from normally-on to normally-off operation can be achieved. The separation between adjacent bodies is shown to have less impact on threshold voltage. The results also show that for wide bodies (> 200 nm) the channel is controlled by both the top-gate and the sidewall gates, while for decreasing body width the control by top-gate gradually diminishes and the channel will be only controlled by side-gates.

Furthermore, the impact of AlGaN barrier design (Al content, thickness) is studied, and the results show a limited dependency of the threshold voltage on the barrier design for very narrow bodies. The tri-gate concept enables normally-off operation, provides improved on-state performance (higher transconductance), and effectively suppresses short-channel effects in the off-state. Moreover, the simulation results show that GaN tri-gate HEMTs can exhibit higher breakdown voltages and operate closer to the theoretical limit for GaN devices than their planar counterparts.

Moreover, the simulations indicate that the RF performance of GaN tri-gate HEMTs with optimized body designs can be superior to that of conventional planar devices. A means to improve the RF performance is the reduction of the body etch height, leading to a decreased parasitic coupling between the sidewalls and the source/drain electrodes. Thus, reducing the body height leads to a decreased overall gate capacitance and an improved RF performance. Another way to reduce the overall gate capacitance is to cover the body sidewalls with a dielectric (e.g. SiN). This reduces the fringing capacitance components since the gap between neighboring bodies that is filled with gate metal is narrower compared to the case without dielectrics.

Finally, the polarization charge at the barrier/channel interface and thus the electron density in the 2DEG) can be increased either by increasing the aluminum content of the AlGaN barrier or by using a different barrier material (e.g., lattice matched $In_{0.17}Al_{0.83}N$). In the frame of a joint DFG project, GaN tri-gate HEMTs designed based on the improved insights in the physics of these devices have been fabricated and characterized at Fraunhofer IAF. These devices having a gate length of 100 nm are by far the fastest GaN tri-gate HEMTs worldwide and

show record performance in terms of cutoff frequency (120 GHz) and maximum frequency of oscillation (300 GHz).

Kurzfassung

HEMTs (high electron mobility transistors) auf GaN-Basis besitzen großes Potenzial für die HF- (Hochfrequenz) und Leistungselektronik und werden bereits in HF-Leistungsverstärkern und als Leistungsschalter verwendet.

Üblicherweise sind GaN HEMTs Normally-On Transistoren (d.h. Transistoren, die sich bei einer Gatespannung von 0 V im Ein-Zustand befinden), was für Anwendungen wie Fail-Safe-Leistungsschalter und HF-Verstärker mit nur einer Versorgungsspannung nachteilig ist. Es schwierig, GaN HEMTs mit Normally-Off-Charakteristik (HEMTs mit positiver Schwellspannung) zu realisieren, da in diesen Transistoren die Dichte des sich an der Grenzfläche Barriere/Puffer ausbildenden 2DEG (zweidimensionales Elektronengas) auf Grund starker Polarisationseffekte erheblich größer als in GaAs und InP HEMTs ist. Die Realisierung schneller HF-HEMTs erfordert kurze Gates. Allerdings leiden Transistoren mit sehr kurzen Gates häufig unter Kurzkanaleffekten und einer reduzierten Steuerwirkung des Gates, was zu einer Verschlechterung des Verhaltens im Aus-Zustand (erhöhte Werte für den Subthreshold Swing und das Drain-Induced Barrier Lowering) und im Ein-Zustand (erhöhter Drainleitwert) führt.

In jüngster Zeit wird bei MOSFETs und HEMTs das Tri-Gate-Design angewendet, um die Gatesteuerwirkung zu verbessern und Kurzkanaleffekte zu unterdrücken. So wurden bereits Tri-Gate-Transistoren mit ausgezeichnetem Skalierungsverhalten, verbesserten Eigenschaften und, speziell im Fall von GaN Tri-Gate-HEMTs, positiver Schwellspannung, demonstriert. Auf der anderen Seite leiden GaN Tri-Gate-HEMTs mit Normally-Off-Charakteristik jedoch unter großen Parasitäten, die das HF-Verhalten (insbesondere die Transitfrequenz) beeinträchtigen. Die Verbesserung des HF-Verhaltens und eine Reduzierung der Parasitäten von GaN Tri-Gate-HEMTs ist daher dringend nötig. Das erfordert jedoch ein tiefes Eindringen in die Physik dieser Bauelemente.

In der vorliegenden Arbeit werden umfassende theoretische Untersuchungen

und Bauelementesimulationen zu GaN Tri-Gate-HEMT beschrieben, die zu einem deutlichen verbesserten Verständnis der Wirkungsweise von GaN Tri-Gate-HEMTs führten. So konnten das Potential dieses Transistortyps bewertet, Designregeln erarbeitet und vorteilhafte Transistordesigns entwickelt werden. In der Arbeit wird gezeigt, dass eine Verringerung der Bodyweite bei gegebener Gatespannung zu einer Verringerung der Ladungsträgerdichte im 2DEG führt, dass die Schwellspannung maßgeblich von der Bodyweite bestimmt wird und dass bei hinreichend geringer Bodyweite der Übergang vom Normall-On- zum Normally-Off-Betrieb erfolgt. Es wird auch gezeigt, dass der Abstand zwischen benachbarten Bodies nur einen geringen Einfluss auf die Schwellspannung hat. Darüber hinaus wird demonstriert, dass im Fall weiter Bodies (> 200 nm) der Kanal sowohl durch das Top-Gate als auch durch die Seiten-Gates gesteuert wird, während bei schmaleren Bodies die Steuerwirkung durch das Top-Gate geringer wird und die Verhältnisse im Kanal im Wesentlichen durch das Seiten-Gates bestimmt werden.

In der Arbeit wird weiterhin Rolle des Designs der AlGaN-Barriere (Al-Gehalt, Dicke) untersucht und demonstriert, dass die Gestaltung der Barriere bei schmalen Bodies nur einen begrenzten Einfluss auf die Schwellspannung hat. Die Untersuchungen zeigen deutlich, dass das mit dem Tri-Gate-Konzept Normally-Off-Transistoren realisierbar sind, dass das Transistorverhalten im Ein-Zustand verbessert (höhere Steilheit) wird, und dass Kurzkanaleffekte im Aus-Zustand wirkungsvoll unterdrückt. Es wird auch demonstriert, dass GaN Tri-Gate HEMTs höhere Durchbruchspannungen zeigen und näher an der theoretischen Grenze für GaN-Bauelemente arbeiten als planare GaN HEMTs.

Ein weiteres Ergebnis der vorliegenden Arbeit ist der Nachweis, dass GaN Tri-Gate-HEMTs mit sorgfältig optimiertem Design den planaren HEMTs auch hinsichtlich des HF-Verhaltens überlegen sind. Ein Mittel zur Verbesserung des HF-Verhaltens ist die Reduzierung der Body-Ätzhöhe, die zur Verringerung der parasitären Kopplung zwischen den Body-Seitenwänden und den Source/Drain-Elektroden und somit zu einer geringeren Gatekapazität führt. Eine weitere Maßnahme zur Reduzierung der Gatekapazität ist die Beschichtung der Body-Seitenwände mit einem Dielektrikum (z.B. SiN). Das verringert die Streukapazität, da jetzt die mit dem Gatemetall gefüllte Lücken zwischen benachbarten Bodies schmaler sind. Schließlich wird gezeigt, dass die Polarisationsladung an der Grenzfläche Barrier/Kanal und somit die Elektronendichte im 2DEG durch Erhöhung des Al-Gehalts der AlGaN-Barriere oder durch Nutzung eines anderen Materials für die Barriere (z.B. gitterangepasstes $In_{0.17}Al_{0.83}N$) gesteigert werden kann.

Im Rahmen eines gemeinsam mit dem Fraunhofer IAF bearbeiteten DFG-Projekts wurden auf der Grundlage der in der vorliegenden Arbeit beschriebenen Erkenntnisse und Designregeln am IAF GaN Tri-Gate-HEMTs entworfen, prozessiert und charakterisiert. Diese Transistoren mit einer Gatelänge von 100 nm sind die mit Abstand schnellsten GaN Tri-gate-HEMTs weltweit und zeigen Rekordwerte für die Transitfrequenz (120 GHz) und die maximale Schwingfrequenz (300 GHz).

Contents

Contents xiii

Chapter 1 Introduction **1**

1.1 Overview of GaN RF Transistors . . . 1
1.1.1 Key Challenges of GaN-based RF HEMTs . . . 4
1.1.2 The Tri-Gate Architecture . . . 5
1.2 Research Aims and Objectives . . . 8
1.3 Original Contribution of Research Field . . . 9
1.4 Organization of Thesis . . . 10

Chapter 2 Overview of the GaN-Based HEMTs **13**

2.1 Structure and Operation . . . 13
2.1.1 Conventional GaN HEMT . . . 14
2.1.2 Polarization Effects in GaN HEMTs . . . 16
2.1.3 GaN tri-gate HEMT . . . 20
2.2 Simulation of GaN-Based Devices . . . 23
2.2.1 Transport Model . . . 24
2.2.2 Traps . . . 26
2.2.3 Simulation of 2DEG in GaN-Based Devices . . . 27
2.2.4 Carriers Mobility and Saturation Velocity . . . 29
2.2.5 Metal-Semiconductor Contacts . . . 30
2.2.5.1 Schottky Contacts . . . 31
2.2.5.2 Ohmic Contacts . . . 32
2.2.6 Material parameters . . . 33
2.3 Calibration of Simulation Tool . . . 34
2.4 GaN-based HEMTs Device Figure of Merits . . . 36
2.4.1 DC Characterization . . . 36
2.4.2 RF Characterization . . . 38
2.5 Summary . . . 41

Chapter 3 DC performance of GaN Tri-gate HEMTs 43

3.1 Electron Distribution . . . 44
3.2 I-V characteristics . . . 48
3.3 Threshold voltage . . . 51
3.3.1 GaN Tri-gate HEMT's Geometry Scaling . . . 52
3.3.2 Effect of process-induced damage on side-walls . . . 58
3.3.3 Strain Relaxation Effects . . . 61
3.4 Electric Field Distribution . . . 64
3.5 Short Channel Effects . . . 69
3.6 Breakdown Voltage . . . 71
3.7 Summary . . . 73

Chapter 4 RF performance of GaN Tri-gate HEMTs 75

4.1 Surface Passivation and Gate Geometry . . . 75
4.2 RF characteristics . . . 78
4.3 RF Scaling Potential of GaN HEMTs . . . 82
4.4 Performance Degradation Analysis . . . 83
4.5 Optimization of GaN Tri-gate HEMTs . . . 86
4.6 Summary . . . 94

Chapter 5 Conclusion and Outlook 97

5.1 Conclusion . . . 97
5.2 Outlook . . . 99

List of Figures 101

List of Tables 109

Bibliography 111

List of Symbols 121

List of Abbreviations 123

Theses of Dissertation 125

List of Publications 127

Journal Publications . . . 127
Conference Proceedings . . . 127

Chapter 1

Introduction

1.1 Overview of GaN RF Transistors

Silicon (Si), Gallium Arsenide (GaAs) based field effect transistors (FET) have been the dominant devices of choice in the RF market to date. However, some of these technologies approaching their theoretical limits imposed by the the intrinsic properties of device material, such as low saturation velocity, energy band gap, breakdown field and thermal conductivity. For high frequency application, it is desired to have higher saturation velocity and band gap. This two main features as are provided by GaN based-FET technology as shown in Fig. 1.1.

The HEMT (High Electron Mobility Transistor) attracted many researchers in the last couple of years due to their promising properties and characteristics (large band gap, strong polarization effects, good electron transport) and they are promising devices for RF (radio frequency) and high-power electronics and are particularly suited for power switches and RF power amplifiers [1],[2],[3]. These properties have made these devices of a great importance in many applications, such as power electronics and RF technology (high frequency). Particularly, these GaN HEMTs is important for energy-efficient fast power switches and RF power amplifier with high operating frequencies. Experimental devices have already been presented with impressive electrical parameters in both areas. Also, due to its high band gap of 3.4 eV, GaN devices can be used even at high temperatures (over 750°C) without problems. In addition to the low noise figure and the relatively high power and current gains. The associated high cutoff frequencies of the GaN HEMTs are due to the high Electron mobility (around 2000 cm^2/Vs) and the high peak velocity achieved in the 2DEG (around $3x10^7$ cm/s).

To a large extent, the impressing performance of GaN HEMTs results from the

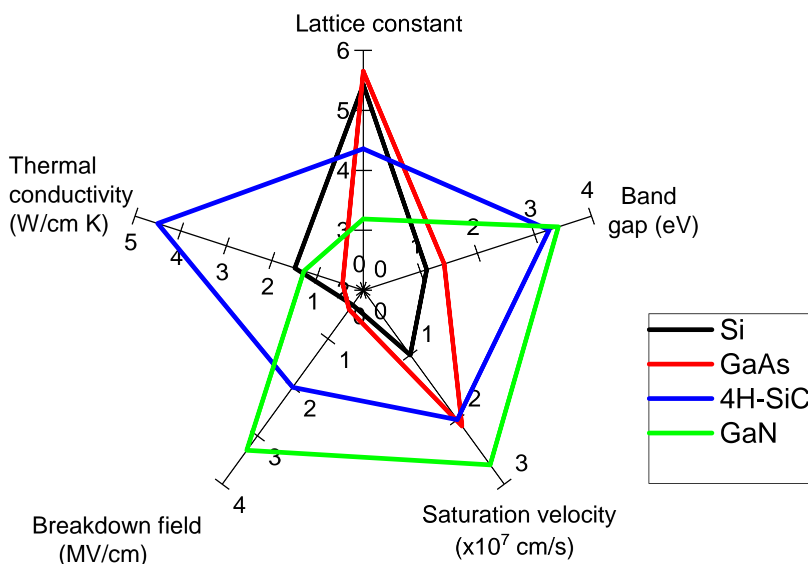

Figure 1.1: Overview of Si, GaAs, SiC and GaN relevant material properties.

outstanding material properties of GaN and of the wide range of heterostructures that can be realized in the Al-Ga-In-N material system. Figure 1.1 shows a comparison of device-relevant properties of GaN with the those of Si, GaAs, and SiC. As can be seen, GaN outperforms the other materials in terms of band gap, breakdown field, and maximum electron drift velocity. However, in terms of thermal conductivity GaN is outperformed by SiC. However, this does not represent a serious drawback since GaN can be grown epitaxially on SiC. Table. 1.1 summarizes the GaN material properties in comparison to other competing in semiconductors market [4],[5],[6]. A GaN with band gap of around 3.4 eV, high breakdown electric field of 3.3 MV/cm, high electron saturation velocity of 2.5×10^7 cm/s and high density carriers due to high mobility mentioned here, giving GaN a super intrinsic properties that allow GaN to play a key role in RF application. In optical (Light emitting diodes LEDs and blue violet laser diodes LDs) and electronic application (microwave, millimeter-wave and RF amplifiers, space and radar electronics..,etc). Moreover, in Tab. 1.1, Johnson Figure of Merit (JFoM) which represents here how suitable a material for high power application at high frequency. Here, GaN and its competing material are presented in Tab. 1.1. JFoM data implies that a material with the highest value is ideal for high power and frequency applications. JFoM can be calculated as:

Table 1.1: Properties of GaN in comparison of other competing materials.

Matrial/ Parameter	Si	GaAs	SiC	GaN	Application
Band gap $E_g(eV)$	1.1	1.4	2.9	3.4	High operating voltages, High temperature operation
Breakdown field $E_c(kV/cm)$	300	400	2500	3300	High operation voltage, High input impedance
Saturation velocity v_{sat} (x$10^7 cm/s$)	1.0	1.0	2.0	2.2	High current density, High DC gain
Dielectric constant ϵ_r	11.4	13.1	9.7	9.5	Lower capacitance, lower parasitic delay
Electron mobility μ $(cm^2/V.s)$	1300	5000	260	2000	High operating frequency, High DC gain
Thermal conductivity χ (W/cmK)	1.5	0.46	4.9	1.3	Efficient heat dissipation,
JFoM	1	2.7	20	27.5	Frequency limits of semiconductor materials

$$JFoM = \frac{v_{sat}E_c}{2\pi} \tag{1.1}$$

where E_c is the critical electric field and v_{sat} is the saturation velocity.

A rapid research on GaN material properties has lead to the fabrication and characterization of the first Metal Field Effect Transistor (MESFET) based on single GaN crystal GaN [7], followed by reporting the first evidence of existing the two-dimensional electron gas (2DEG) at the AlGaN/GaN interface were reported in 1993 by Khan et al [8]. The first GaN heterostructures field effect transistor (HFET) were reported in 1994 by Khan et al [9] and ever since the performance of GaN HEMTs has continuously been improved.

1.1.1 Key Challenges of GaN-based RF HEMTs

Although GaN HEMTs have shown attractive RF performance, most of these transistors are normally-on (depletion-mode) devices, i.e., they have a conducting channel at zero gate voltage and can only be switched off by applying a negative gate voltage. However, for many applications normally-off (enhancement-mode) transistors with a positive threshold voltage are desirable. Realizing GaN normally-on HEMTs is challenging due to the high polarization-induced electron sheet concentration of the 2DEG channel at the AlGaN/GaN interface, which must be completely depleted for zero gate voltage. Several approaches for achieving normally-off GaN HEMTs have been reported in the literature, e.g., using a very thin barrier, etching a gate recess, fluoride plasma treatment of the region underneath the gate, exploiting the piezo-neutralization technique, and following hybrid MIS-HEMT (metal-insulator-semiconductor-HEMT) structures [10],[11],[12],[13],[14],[15],[16],[17].

Each of these approaches have their advantages and disadvantages, but they have in common that conventional top gate structures are used and that the enhancement performance is achieved through the vertical design of the layer stack under the gate. Despite the impressive cutoff frequency(f_T) and the maximum frequency of oscillation (f_{max}) behavior of GaN HEMTs [18], there is still much room for improvement. The presented results in Tab. 1.2 of the GaN HEMTs show that a high f_{max} and a small drain conductance g_{ds} are essential [18], [19]. The effect of a high drain conductance to the RF behavior of FET (Field Effect Transistor) has been studied in [20] and the negative effect of g_{ds} specifically on power amplification and f_{max} were discussed in detail [21].

The shown data in Tab. 1.2 show that by shrinking the gate length from 40 to 20 nm as expected leads to a significant increase of f_T. However, only the 20 nm normally-off GaN HEMT also provides a higher f_{max}, while the 20 nm normally-on HEMT, partly because of its poor electrostatics in the channel and the resulting higher drain conductance, with regard to f_{max} is even worse than the 40 nm normally-on GaN HEMT. A good electrostatics and a low g_{ds} are therefore essential for transistors with high f_{max}. A comparison of the GaN HEMTs [18] clearly demonstrates that for RF applications there is a need to reduce g_{ds} for GaN HEMTs. Figure 1.2 shows RF performance of GaN HEMTs in terms of cutoff frequency f_T and maximum frequency of oscillation f_{max} versus gate length (status as of mid-2013). The results clearly demonstrate that by shrinking the gate length, both frequencies f_T and f_{max} increase. This means

Table 1.2: Comparison between the ratio (g_m/gds), transconductance (g_m), drain conductance (gds), cutoff frequency(f_T) and the maximum frequency of oscillation (f_{max}) of experimental HEMTs: normally-on and normally-off GaN HEMTs.

Device	L_G (nm)	g_m (mS/mm)	g_{ds} (mS/mm)	g_m/g_{ds}	f_T (GHz)	f_{max} (GHz)	Ref.
Normally-on	40	1285	108	11.9	186	400	[19]
Normally-off	20	1250	245	5.1	310	364	[18]
Normally-off	20	1620	149	10.9	342	518	[11]

for GaN HEMTs with sub-100 nm gates, extremely thin barrier to achieve the enhancement performance and sophisticated design to reduce the series resistance, a better performance can be achieved. The strategy to be implemented is a combination of this barriers, short gate and minimal series resistances is very popular.

1.1.2 The Tri-Gate Architecture

To find ways to improve the normally-off GaN HEMTs for power switches, improvement of electrostatics and reduction of g_{ds} for RF HEMTs, a look at developments in Si MOSFETs is very helpful. For over 20 years of Si tri-gate MOSFETs (called also FinFET in literature) in which the channel body (hereinafter referred to as body) is surrounded from three sides by metal-gate [22]. Tri-gate MOSFETs have, compared to conventional top gate MOSFETs several advantages [23],[24],[25]: For small bodies, the threshold can be adjusted via the Body cross section and increases with n-channel MOSFETs with decreasing cross-section. The breakdown voltages of tri-gate MOSFETs are higher than comparable single-gate MOSFETs. Tri-gate structures show significantly better electrostatics and suppress short-channel effects significantly more effectively than top-gate structures. While for digital MOSFETs the short-channel effects are relevant for sub-threshold operation in the dc-state are essential, poor saturation of the drain current and large drain conductance for RF. The tri-gate concept has originally been developed for Si MOSFETs and leading chip makers, e.g., Intel, have already introduced tri-gate MOSFETs into mass production

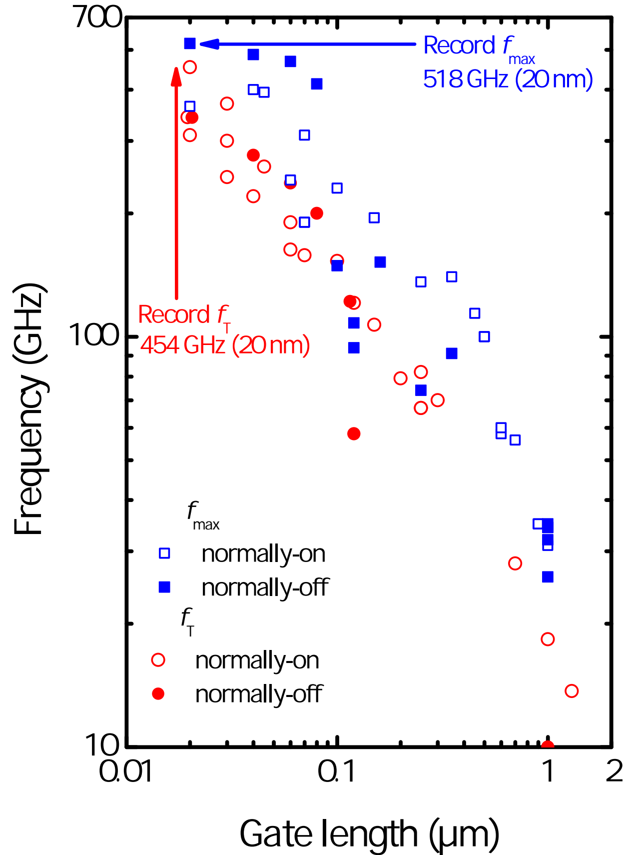

Figure 1.2: The State of research on the normally-on and normally-off GaN HEMTs. (a)Transit frequency f_T and (b) Maximum oscillation frequency f_{max} as a function of gate length. The experimental data presented are compiled from the current literature.

[26],[27],[28],[21],[29]. The long-term research on Si tri-gate MOSFET have paid off and Intel now applies these transistors in its latest processors [30]. This successful development leads to the conclusion that intensive investigations on the suitability and potential of the tri-gate concept for GaN HEMTs approach should be performed.

Recently, the tri-gate concept has been proposed as an alternative approach to improve gate controllability of GaN HEMTs [31]. The tri-gate takes advantage of the three dimensional non-planar design where the gate is wrapped around narrow bodies from three sides. The tri-gate concept is interesting not only for Si MOSFETs but for GaN RF HEMTs as well, since it is an alternative option to achieve normally-off operation and to suppress short-channel effects. Indeed, experimen-

tal GaN tri-gate HEMTs showing a positive threshold voltage shift compared to conventional planar transistors have been demonstrated [32],[33],[34],[30]. In-depth insights into the dependence of the HEMT threshold voltage on the body width and etch depth have been presented by the author [35], [36]. A general advantage of the tri-gate design compared to conventional planar is the improved electrostatics leading to a better suppression of SCEs [37],[38],[39]. However, as can be seen from Fig. 1.3, until mid-2013 GaN RF tri-gate HEMTs still performed worse compared to their single-gate planar counterparts.

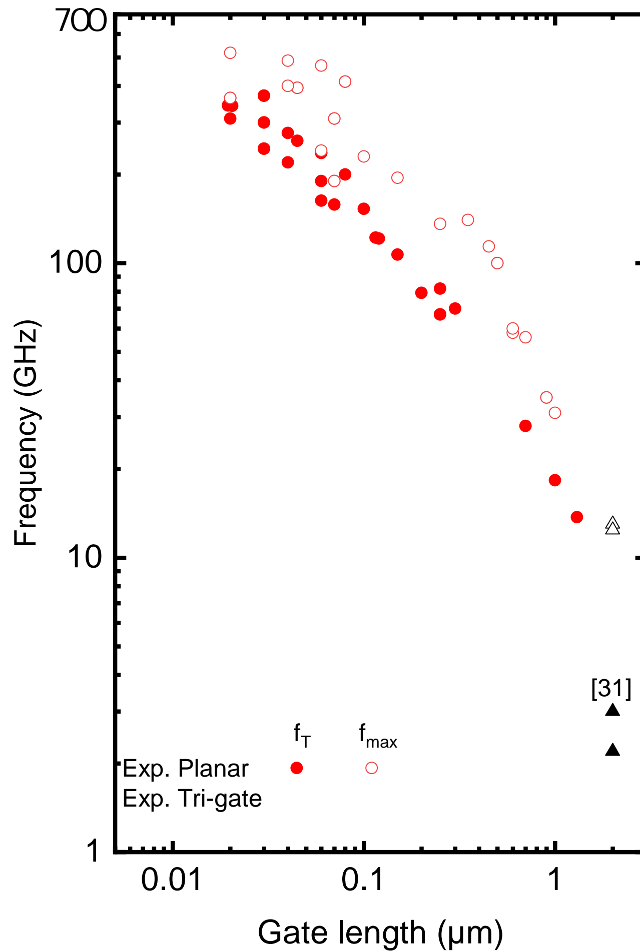

Figure 1.3: The State of research on GaN HEMTs: Transit frequency f_T and Maximum oscillation frequency f_{max} as a function of gate length for both planar and tri-gate ([31]) GaN HEMTs until mid of 2013.

The tri-gate concept represents a real breakthrough for GaN HEMTs. However, many of the tri-gate advantages are not fully exploited due to the lack of theoretical studies, specific advantages, technology limitations, optimized device designs and reliability issues. Furthermore, the elaboration of design guidelines and optimized transistor structure for high-frequency application required a great research effort.

1.2 Research Aims and Objectives

The advantages of the tri-gate architecture for the behavior of Si MOSFETs are meanwhile well established and relatively good understood. Although the GaN tri-gate HEMT also exploits the gate effect from three sides, the details of its operation are quite different. This becomes obvious when considering the position of the channel in the Si tri-gate MOSFET and comparing it to that in a GaN tri-gate HEMT. In a Si tri-gate MOSFET with relaxed body dimensions (large body cross-section), in the on-state three inversion channels (2DEG channels) are formed at the left, top, and right body/oxide interfaces.

If the body cross-section is reduced, the situation gradually changes and finally in Si tri-gate MOSFETs with very narrow and thin bodies the three channels merge to a single channel located at the center of the body cross-section (this effect is called volume inversion). In the GaN tri-gate HEMT, the conditions are entirely different. Here, regardless of the body dimensions, only one single 2DEG channel exists at the AlGaN/GaN interface and when shrinking the body cross-section, this channel merely gets narrower.

For fast transistors, short gates are mandatory. However, down scaling the gate length into the deep sub-100 nm range leads to undesirable short channel effects (SCE) which degrade the control of the gate over the channel resulting in an increase of the output conductance, which in turn, degrades the RF performance, in particular the power gain and the maximum frequency of oscillation [40],[41]. SCEs can be suppressed by different approaches, each with specific advantages and drawbacks. Examples are thin AlGaN/InGaN back-barriers, [42],[43],[44], N-polar GaN channels [45], and gate recessing [12]. It should be noted, however, that the improved performance of GaN HEMTs by using these approaches is achieved at the expense of a sophisticated processing.

Moreover, it has been already reported by Palacios et al, that GaN HEMT at very short gate lengths show a pronounced decrease at higher gate voltages due to the increase in access resistance which causes a drop down of the cutoff frequency

f_T which limits the usage of GaN HEMT devices for high frequencies application [46]. As the tri-gate topology is proven to tremendously suppress short channel effects, one expects that GaN tri-gate HEMT should mitigate this linearity issue and improve the RF parameters.

For a theoretical description of GaN tri-gate HEMTs and simulation of their electrical behavior there are yet not many publications. However, to understand the physics of these transistors in order to assess their potential and to develop advantageous designs, in-depth theoretical work is essential. The state of research shows that GaN tri-gate normally-off HEMTs represents a very promising option for power switches. However, for RF applications, it seems that GaN tri-gate HEMTs are performing worse in terms of the cutoff frequency than planar counterpart [31], and the reason was not clear at the time I started my research on GaN tri-gate HEMTs. Therefore, further research on the theory and technology of GaN tri-gate HEMTs will advance our knowledge and improve their future applications. The present thesis aims at performing in-depth theoretical investigations on GaN tri-gate HEMTs and to develop optimized transistor design to fully exploit the potential of the tri-gate architecture. To this end, extensive 2D (two-dimensional) and 3D device simulations have performed. The thesis provides systematic theoretical studies in the following areas.

1.3 Original Contribution of Research Field

In 2012, when this work has started, there was no clear understanding of tri-gate physics. There was only few published research on GaN tri-gate HEMT/MISFET [17], [31]. During this work, the author was able to achieve and publish valuable information that helped to enrich the knowledge on GaN-based tri-gates HEMTs and inspired other research groups and was able to:

- Obtain an encompassing picture of the GaN tri-gate HEMTs physics and elaborate of the similarities and differences between Si tri-gate MOSFETs and GaN tri-gate HEMTs.

- Compare and calibrate physic-based simulation tools with respect to measured AC and DC data and include many expected physical behaviors.

- Use physic-based device simulations to reliably calculate DC and AC-small signal analysis characteristics of GaN tri-gate HEMTs reported in literature and fabricated by our project partner (IAF, Freiburg, Germany).

- Investigate the DC performance of the GaN tri-gate HEMTs design and compare it to that of conventional planar HEMTs such as threshold voltage dependency on body with, etch depth and separation.
- Provide guidelines to achieve normally-off operation on several structures.
- Investigate of the origin of short-channel effects in GaN tri-gate HEMTs in the off- and in the on-state.
- suppressing the short channel effects by achieving the optimum GaN tri-gate HEMT's geometry to ensure better electrostatic improvement.
- Investigate the RF performance of the GaN tri-gate HEMTs design, compare it to that of conventional planar HEMTs and elaborate the merits and drawback of GaN tr-gate HEMTs.
- Investigate the effects of unavoidable process-induced variations, particularly of the properties of neighboring parallel bodies, on the overall transistor performance.
- Propose design guidelines to reduce the parasitic elements which has led our project partner IAF Germany to demonstrate one of the fasted GaN HEMT devices.
- Characterizing measured and simulated data to provide valuable set of results that can be trusted.
- Make suggestion for a future research work that can leads to more improvements.

1.4 Organization of Thesis

The thesis contains 5 chapters and is organized as follows: After the introduction, a brief survey of the history of GaN HEMTs, of their main applications and their limitations will be provided in Chapter 2, together with relevant background information on the framework of GaN HEMT simulation and the models needed for device simulation.

Chapter 3 deals with DC simulations of GaN based HEMTs and discusses in detail the DC behavior and related figures of merit (such as threshold voltage, short-channel effects, breakdown voltage) of GaN tri-gate HEMTs and compare these to their conventional planar counterparts.

In Chapter 4, the RF performance of GaN tri-gate HEMT structures is investigated and discussed. Additionally, measures to improve the performance of these devices by proposing design guidelines are elaborated in this chapter. Finally, Chapter 5 summarizes the work, draws conclusions from the simulation results, and provides an outlook for future work.

The research in the frame of the present thesis has been performed in close collaboration with Fraunhofer IAF in Freiburg, Germany. At IAF, appropriate designs for GaN tri-gate HEMTs considering both the fabrication capabilities available at IAF, existing processing limitations, and the findings of the author′s simulations presented in this thesis, have been elaborated and transferred to experimental devices. A thorough electrical characterization at IAF revealed world record performance of these GaN RF tri-gate HEMTs as will be shown at the end of thesis.

Chapter 2

Overview of the GaN-Based HEMTs

The following chapter deals with the basics of GaN HEMTs. It presents first a brief history on GaN as a material for semiconductor technology and the advantages of such material in RF electronics. Furthermore, the structure, operation and important characteristics of conventional GaN HEMTs are discussed. This chapter also deals with the physic-based device simulation tools (Nextnano^3, 2D and 3D TCAD Silvaco) used to simulate GaN HEMTs. It presents the used carrier transport and mobility models used in simulations, possible effects such as traps in bulk material, formation of 2DEG in the GaN HEMT channel. A brief overview on the commonly used figures of merits to characterize the DC and RF performance are also presented in this chapter.

2.1 Structure and Operation

A GaN-based HEMT is a three-terminal device in which the carriers, electrons, are traveling through a 2DEG channel at the AlGaN/GaN interface and the number of electrons is modulated by the electric field that results from the gate bias. First report on the fabricating of a HEMT using an AlGaN/GaN heterojunction with n-doped barrier was presented by Khan et al. in 1993 [8], reporting 23 mS/mm transconductance and 563 cm^2/Vs 2DEG mobility at 300K. Only one year later, the same group reported first microwave results for GaN HEMTs, with cutoff frequency (f_T) of 11 GHz and maximum frequency of oscillation (f_{max}) of 14 GHz [9]. This, however, was very low compared to theoretical material limits, and a lot of research has been conducted to improve the performance of GaN

HEMTs.

2.1.1 Conventional GaN HEMT

Essentially, a GaN-based HEMT consists of a 100-120 nm nucleation layer grown on a substrate material (Si, Sapphire or SiC), followed by a thick isolating GaN buffer layer (1-3 μm), a barrier layer (in this work AlGaN and AlInN) and a relatively thin GaN cap layer to reduce leakage current and suppress current collapse [47]. Figure 2.1 shows the cross section of a GaN HEMT. Normally, substrates have different lattice constants than the GaN layer, which in other words means a lattice-mismatch inducing strain between the substrate and GaN layer, and this would cause a high density of lattice defects. To avoid this, a nucleation layer (most likely AlN) is grown on top of the substrate.

AlGaN/GaN HEMT presents a unique feature: A 2DEG is formed a the heterojunction due to polarization effects and the conduction band offset between the barrier and channel layers. The barrier has a higher conduction band than the channel, and due to the conduction band discontinuity the electrons transfer from the larger band gap (AlGaN or AlInN) to the smaller band gap GaN.

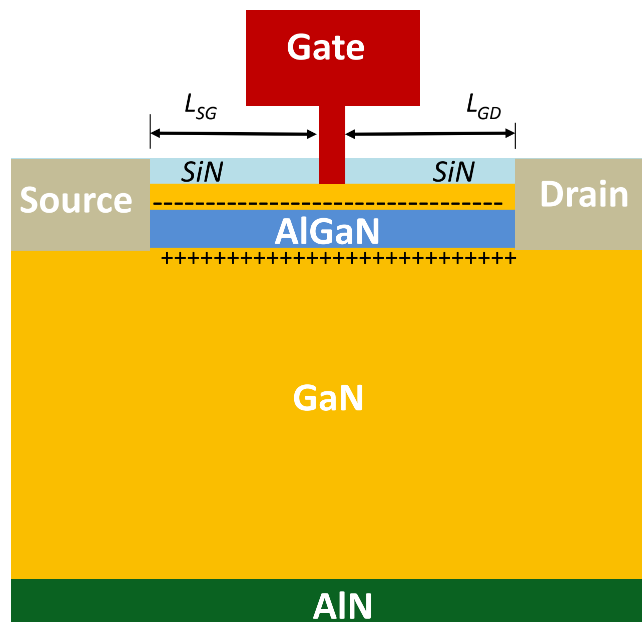

Figure 2.1: A schematic of the investigated planar GaN HEMT structure.

The high sheet carrier concentration at the AlGaN/GaN interface ($\approx$ 2x10^{13} cm^{-2}) induced by the piezoelectric and spontaneous polarization charges, along with the confinement of two dimensional electron gas (2DEG) results in band bendings at the heterojunction. Figure 2.2 illustrate the energy band diagram under the gate electrode. The large carrier density is mainly at the AlGaN/GaN interface due to spontaneous and piezoelectric polarization effects. The high sheet charge along with the conduction band offset between AlGaN/GaN leads to the formation of a quantum well having a triangular shape as depicted in Fig. 2.2. The mobility of confined electrons and the saturation velocity at the quantum well are to high compared to bulk material, which is a key feature of the GaN-based HEMTs. The 2DEG sheet charge can be controlled by applying an appropriate bias on the Schottky barrier gate place on the barrier layer.

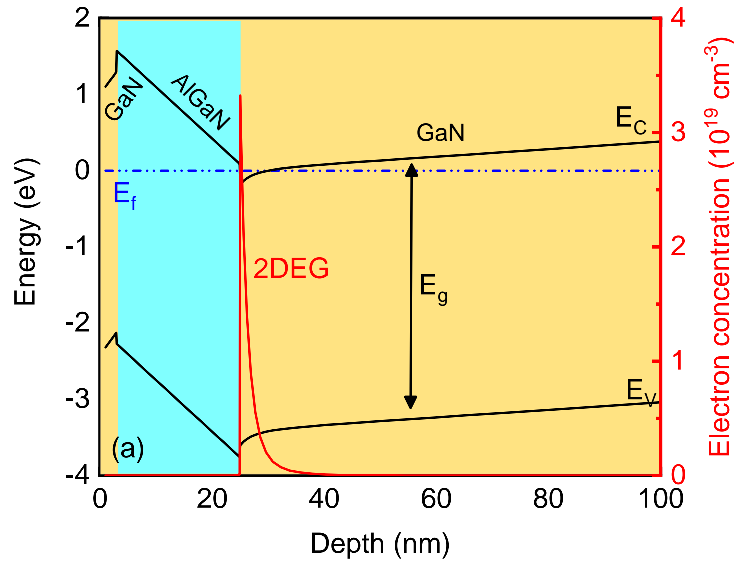

Figure 2.2: Simulated energy band diagrams and electron density underneath the gate region of an AlGaN/GaN heterojunction with 1 μm GaN buffer, 22 nm $Al_{0.22}Ga_{0.78}N$ barrier and a 2 nm cap thickness.

The drain current I_{DS} in the GaN HEMT flow from drain to source and is controlled by the applied gate voltage which is varies the 2DEG. The Schottky gate is a reverse biased and the electrons in the 2DEG will be depleted when applying a negative voltage to the gate. This is due to the normally-on nature of GaN HEMT, which required applying a negative gate voltage relative to drain and source contacts to switch the device OFF.

2.1.2 Polarization Effects in GaN HEMTs

Group-III nitride materials such as GaN, AlN and InN exist in wurzite and zinc-blende crystal structures. However, wurzite crystal structure is commonly used in electronic devices due to their large spontaneous polarization if no external electric field is applied (because of the noncentro symmetric nature of the wurzite crystal structure)[48],[49].

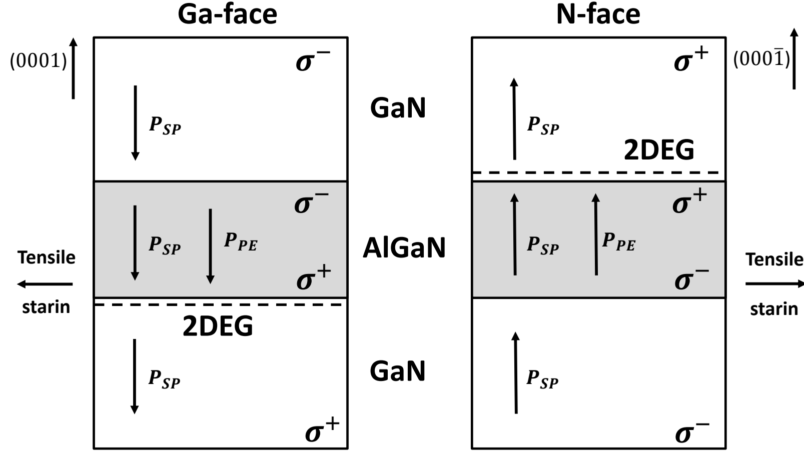

Figure 2.3: Spontaneous and piezoelectric polarization bound interface charges and 2DEGs in pseudomorphic GaN/$Al_xGa_{1-x}N$/GaN heterostructure with Ga-face (left) and N-face (right).

Furthermore, stressing the wurzite structure along the [0001] direction is found to form a nonzero piezoelectric modulus, which results in piezoelectric effects. Polarization charges are formed between the barrier (e.g., $Al_xGa_{1-x}N$ or $Al_xIn_{1-x}N$) and the GaN buffer due to these piezoelectric effects and the difference in spontaneous polarization between the barrier/channel of GaN FETs as shown in Fig. 2.3. As shown here, the spontaneous polarization in case of Ga-face is negative because all direction vectors point toward the substrate while in the N-face structure, the direction vector points away from substrate.

The spontaneous polarization charge for $Al_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ alloys as a function of x (in C m^{-2}) are give by [48],[49]:

$$P^{sp}_{AlGaN} = -0.090x - 0.034(1-x) + 0.021x(1-x) \tag{2.1}$$

$$P^{sp}_{AlInN} = -0.090x - 0.042(1-x) + 0.070x(1-x) \tag{2.2}$$

As shown in Fig. 2.4, the spontaneous polarization charge for both $Al_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ have nonlinear behavior as a function of the alloy composition x. This nonlinear dependence is caused by the third term in Eq. 2.1 and Eq. 2.2. It is

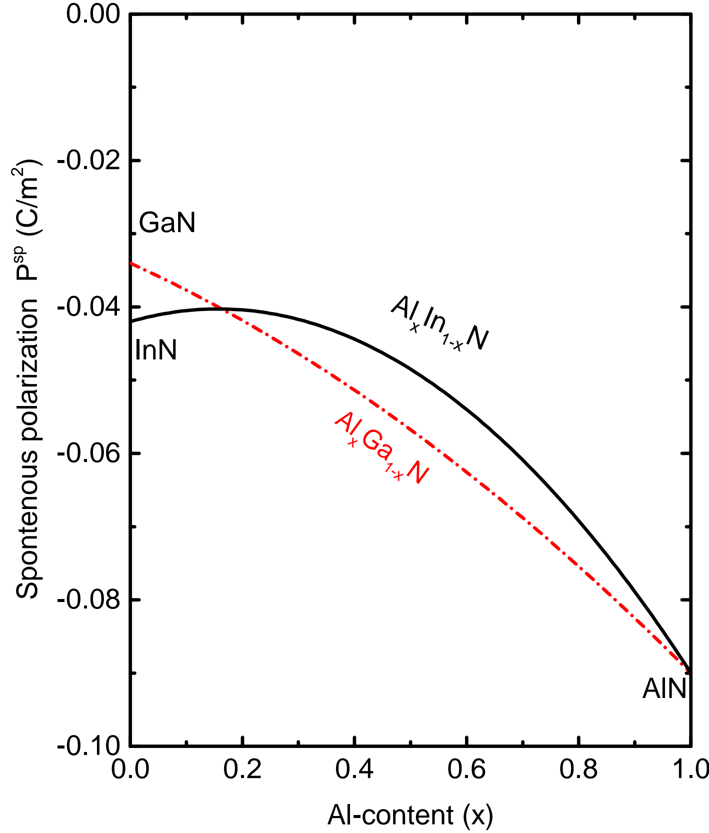

Figure 2.4: Spontaneous polarization of the $Al_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ alloys with wurzite crystals calculated from Eq. 2.1 and Eq. 2.2

not enough to know only the spontaneous polarization to predict the polarization interface charges between the GaN-based structures, because the GaN-based heterostructure are grown strained and pseudomorphically on buffer layers. Therefore, in order to ensure a better description of the polarization interface charges in GaN-based heterostructure, both spontaneous and piezoelectric have to be calculated. The piezoelectric polarization based on that can defined by the non-vanishing component of the piezoelectric polarization caused by the biaxial strain as [48]:

$$P^{pz}_3 = \varepsilon_1 e_{31} + \varepsilon_2 e_{32} + \varepsilon_3 e_{33} \tag{2.3}$$

The piezoelectric polarization pointing along the [0001] direction when a strained AlGaN layer is grown on a relaxed GaN bulk layer is calculated under the the

assumptions that e_{31}=e_{32} and $\varepsilon_3 = -2\frac{C_{13}}{C_{33}}\varepsilon_1$ to be

$$P_3^{pz} = 2\varepsilon_1(e_{31} - e_{33}\frac{C_{13}}{C_{33}}) \tag{2.4}$$

the strain is calculated as

$$\varepsilon_1 = \frac{a_0 - a(x)}{a(x)} \tag{2.5}$$

where a_0 represents the in-plane lattice constant for the relaxed GaN buffer and a is the in-plane lattice constant for the strained barrier (i.e., $Al_xGa_{1-x}N$ or $Al_xIn_{1-x}N$).

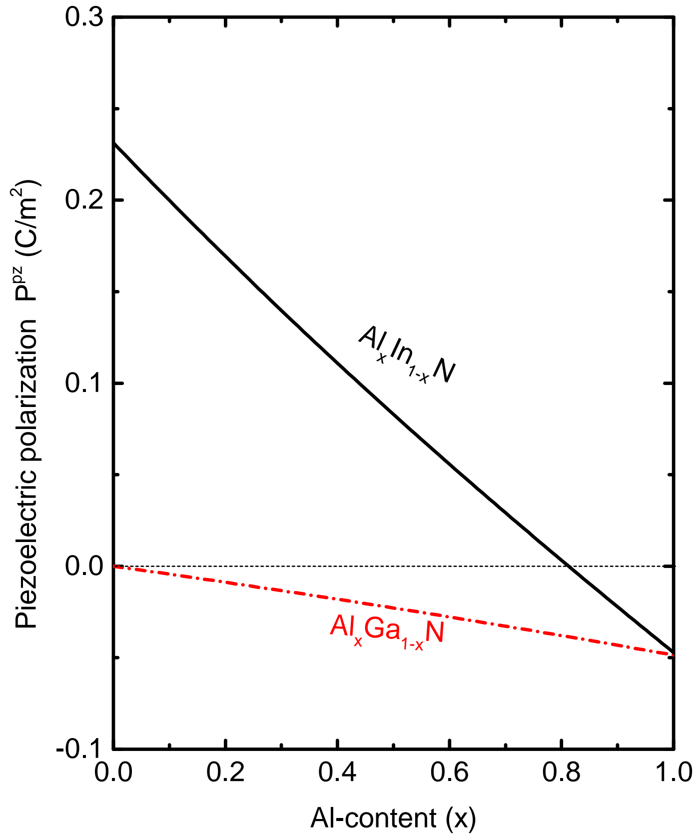

Figure 2.5: Piezoelectric polarization of the $Al_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ alloys with wurzite crystals calculated from Eq. 2.9 and 2.10

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Based on Equ. 2.5 and the linear interpolation of both the elastic and piezoelectric constants, the piezoelectric polarization charges (give in Cm^{-2}) for the $Al_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ barriers are found to be nonlinearly dependent on the

alloy composition as follow:

$$P^{pz}_{GaN} = -0.918\varepsilon + 9.541\varepsilon^2 \tag{2.6}$$

$$\begin{aligned} P^{pz}_{AlN} &= -1.808\varepsilon + 5.624\varepsilon^2 \text{ for } \varepsilon < 0 \\ P^{pz}_{AlN} &= -1.808\varepsilon - 7.888\varepsilon^2 \text{ for } \varepsilon > 0 \end{aligned} \tag{2.7}$$

$$P^{pz}_{InN} = -1.373\varepsilon + 7.559\varepsilon^2 \tag{2.8}$$

By applying Vergard's law to calculate strain $\varepsilon_1 = \varepsilon(x)$ and using Eq. 2.6, 2.7 and 2.8, the polarization charge for strained $Al_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ barriers grown on relaxed GaN buffer is calculated as follow:

$$P^{pz}_{AlGaN} = xP^{pz}_{AlN}(\varepsilon(x)) + (1-x)P^{pz}_{GaN}(\varepsilon(x)) \tag{2.9}$$

$$P^{pz}_{AlInN} = xP^{pz}_{AlN}(\varepsilon(x)) + (1-x)P^{pz}_{InN}(\varepsilon(x)) \tag{2.10}$$

In Fig. 2.5, the piezoelectric polarization for both $Al_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ heterostructures as a function of the alloy composition is shown. It is important to note that the $Al_{0.82}In_{0.18}N$ heterostructure is lattice matched (i.e., piezoelectric polarization is zero). It has been shown that increasing the polarization charge at the barrier/channel interface (i.e. increasing the electron density in the 2DEG) can results in a decreasing source resistance R_s, which correspondingly increases transconductance based on:

$$g_{m,ext} = \frac{g_{m,int}}{1 + R_s g_{m,int}} \tag{2.11}$$

where $g_{m,ext}$ is the extrinsic transconductance and $g_{m,int}$ is the intrinsic one . This can be done by either increasing the aluminum content of the $Al_xGa_{1-x}N$ barrier or by using another barrier material. However, if the Al-content exceeds 30%, partial relaxation becomes likely that in turn reduces the polarization and degrades the electron mobility in the 2DEG [50]. A good alternative is the use of lattice matched (i.e. unstrained) $Al_{0.83}In_{0.17}N$ barriers, where relaxation is not an issue (see Fig. 2.9).

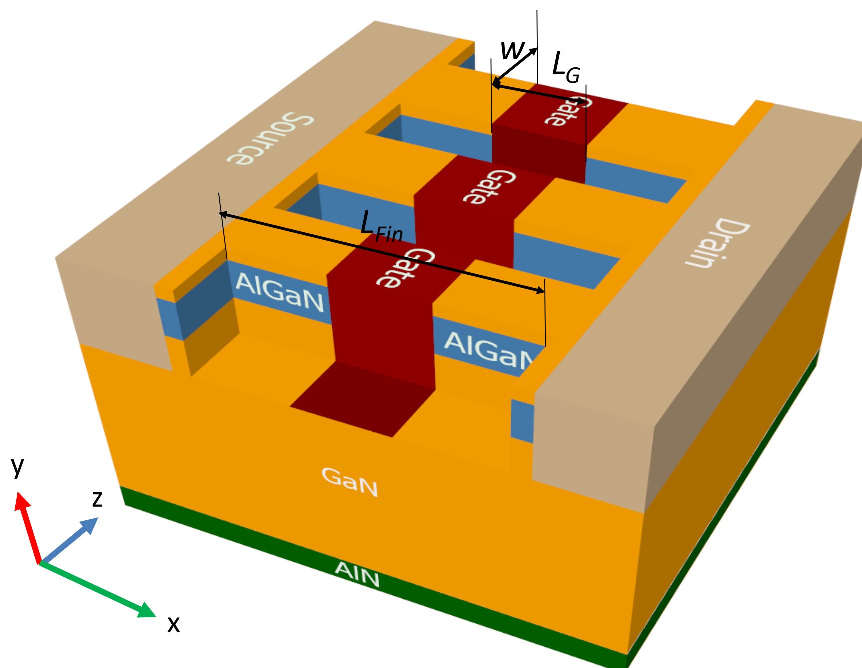

Figure 2.6: A 3D schematic illustration of the investigated GaN tri-gate HEMTs structure.

2.1.3 GaN tri-gate HEMT

Commonly, AlGaN/GaN HEMTs are normally-on transistors, i.e., they are in the on-state for zero applied gate voltage and have a negative threshold voltage. For various important applications such as fail-safe power switches and RF amplifiers with single-polarity power supply [51],[52], however, normally-off transistors having a positive threshold voltage are needed. Unfortunately, achieving a positive threshold voltage in AlGaN/GaN structures is more difficult compared to GaAs- and InP-based HEMTs due to the high density of the polarization-induced 2DEG (two-dimensional electron gas) at the AlGaN/GaN interface. A viable topology that has been recently used and found to provide a significant shift of threshold voltage V_{Th} toward positive is the GaN tri-gate HEMT [53],[16].

The tri-gate design is proposed as an alternative approach to improve gate controllability of GaN HEMTs which enhances the performance in the ON-state while improving the OFF-state at the same time. Periodic multiple 2DEG channels and trenches can be formed using dry etching processes. The tri-gate takes advantage of the 3D non-planar design where the gate is wrapped around narrow AlGaN/GaN bodies from three sides as shown in Fig 2.6. The x-axis horizontal layout between source and drain, y-axis points toward the vertical layout defin-

ing the distance from nucleation layer to the top of gate electrode and z-direction define the width of the structure.

Figure 2.7, depicts 2D (in x-y direction) electron distribution through a vertical cut at the mid of the gate electrode (in z-direction) of the layer sequence. Multiple tri-gate bodies are realized in Fig. 2.7a instead of one wide channel in the conventional planar GaN HEMT (Fig. 2.7b). Experimental GaN tri-gate HEMTs showing a significant shift of threshold voltage toward normally-off compared to conventional top-gate control transistors have been demonstrated [17] and shortly afterwards GaN tri-gate HEMTs with improved gate controllability for down-scaled gate lengths and positive threshold voltages have been reported [31],[32].

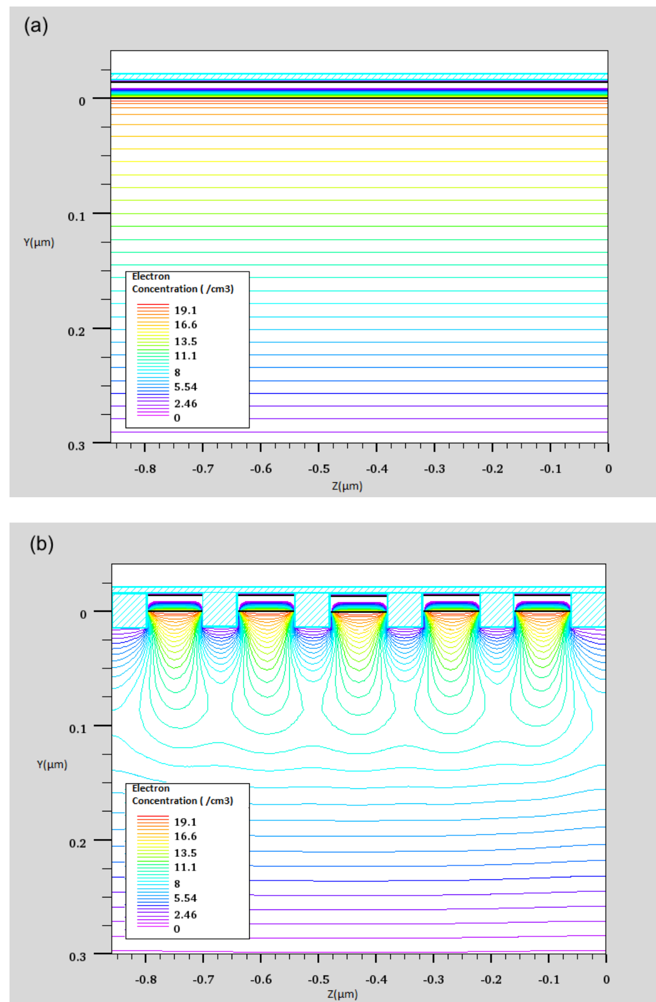

Figure 2.7: 2D contour plot of the electron distribution of two GaN HEMT device having the same total gate-width calculated at zero applied gate voltage for (a) Planar (b) tri-gate GaN HEMT structures with 100 nm body width.

The shift of threshold voltage in GaN tri-gate HEMTs with narrow AlGaN/-GaN bodies is caused by the combination of two effects, namely (i) the enhanced gate control due to the two gates at the body sidewalls in addition to the top-gate and (ii) partial strain relaxation in the AlGaN barrier of narrow bodies resulting in a reduced piezoelectric polarization [34],[30] and, consequently, a lower 2DEG sheet density for a given gate voltage.

An additional general advantage of the GaN tri-gate HEMTs design compared to conventional top-gate transistors (that has been demonstrated not only for GaN tri-gate HEMTs but for Si tri-gate MOSFETs as well) is the improved electrostatics leading to a better suppression of short channel effects [25],[28],[21],[22]. This improved suppression of short channel effects will allow for further channel down scaling of GaN HETMs.

In [54],[46] excellent RF improvement in terms of linearity for the AlInN/GaN tri-gate compared with the conventional planar is reported as a result of reducing access resistance in the source region. The improvement in linearity means flatter f_T (less bias dependent) which considered to be attractive for millimeter-wave applications. It should be noted that most GaN tri-gate HEMTs reported are so far long-channel devices and that only little is known on the behavior of short-channel GaN tri-gate devices.

The GaN tri-gate HEMT design considered here has the same layer sequence presented in previous subsections. Both conventional planar and tri-gate GaN HEMTs are fabricated with similar process steps on the same wafer for fair comparison. The layer sequence consists of a nucleation layer, a GaN buffer/channel layer, an $Al_xGa_{1-x}N$ barrier, a GaN cap, a Si_3N_4 passivation layer is deposited on the inactive (etched) area and a Ni/Au gate electrode with gate length L_G wrapped around the body from three sides (i.e., on top of the GaN cap and the sidewalls) is defined.

The source to gate distance L_{SG} and drain to gate distance L_{GD} are fixed at 0.7 μm. The GaN tri-gate HEMTs body width w, body height h (i.e., the body etching depth) and the separation between two adjacent bodies d, unless otherwise stated all are fixed to 100 nm. The entire structure is assumed to be undoped, however, acceptor-like traps in the bulk with activation energy of 0.64eV and density of 1.3 $\times 10^{16}$ cm^{-2} are assumed to reduce the bulk leakage in the off-state and to provide isolation by compensating the unintentional doping resulting from the metal organic vapor deposition (MOCVD)[39].

2.2 Simulation of GaN-Based Devices

Before we start the discussion on devices simulation and the models used for it, it worth to review some basic concepts of GaN-based HEMTs simulation and discuss fundamental semiconductor equations. This is important to understand the simplification and limitations inherent in such calculations. To this end, we provide an overview of device simulation, as well as the physical models and parameters used for simulating GaN-based devices. The polarization including spontaneous and piezoelectric charges are also introduced in addition of the channel formation in GaN HEMTs. Furthermore, carrier transport under low and high field conditions is described. The material parameters required for the simulation are provided in details.

Semiconductor device simulation has gained considerable attention during the last five decades, and it has helped so far the semiconductor industry by predicting, analyzing and improving devices performance and design. Devices are getting smaller and much more sophisticated, and this requires device simulation to still continue effectively predicting the physics and behavior of semiconductor devices. Most required semiconductor's properties to be investigated by research and industry are steady-state DC, noise, thermal, small and large-signal analysis.

Most device simulators utilizes a combination of mathematical models to describe the electrical characteristics of electron devices which are associated with specific physical operations and bias conditions. Approximating the operation of the electron device onto two or three dimensional grid (mesh). At every grid point several equations inside the simulated device are solved. These equations are derived from Maxwell's law and consist of Poisson equation, the continuity and the transport equations. The mathematical models used to solve these equations consist of, set of basic equations which describe and relate the carrier densities and electrostatic potential within the simulated structure.

Technology computer-aided design (TCAD) simulations are widely used for research purposes. These simulations capable of simulating large scales (e.g., micrometer scale) as well as deep sub-micron scales. TCAD simulations incorporate numerical methods and advanced physical models for simulating most semiconductor devices behaviors. Modeling and simulating the device physical characteristics is seen to be important in predicting devices performance. Moreover, they are shown to be much faster and cheaper than fabricating and measuring experimental devices, and they could provide information that is impossible to get from real devices. The simulations tools to be used are the device simulator:

- Nextnano[3] that allows both quantum-mechanical and classical 2D simulations [55].

- DEVICE3D Silvaco to perform 2D and 3D classical device simulations[56].

2.2.1 Transport Model

The transport of electrons and holes is described by Boltzmann equation (BTE)[57]. The BTE for electron gas in semiconductor is defined as:

$$\frac{\partial f}{\partial t} + u\nabla_x f + \frac{qE}{\hbar}\nabla_k f = C(f) \tag{2.12}$$

where f is the electron distribution in momentum space k and a physical space x. The vector u is the velocity coordinate in state ($u = \nabla_k \epsilon/\hbar$, $\epsilon = \epsilon(k)$ describes the conduction band energy), q the elementary charge, $\hbar$ the reduced Planck constant ($h/2\pi$), E is the electrical field and ∇_k the velocity gradient operator.

However, solving the BTE is typically very difficult due to its integro-differential nature with seven independent variables. To get a result through a direct solution of the BTE one has to make a drastic approximation to solve the basic equations (drift-diffusion and Poisson) governing the transport in semiconductors and devices containing them. Simplifying and approximating the BTE is used to obtain the current density equations or/and charge transport models. Different transport models, however can result from this approximation such as the kinetic models (quantum transport equations, hydrodynamic and semi- classical BTE) and Drift-diffusion model (known as balance equations). Although more advanced models are provided and included by many simulators, the drift-diffusion model (DDM) remains the simplest and useful transport model of constitutive equations.

$$J_n = qn\mu_n E + qD_n\nabla_n \tag{2.13}$$

$$J_p = qn\mu_p E + qD_p\nabla_p \tag{2.14}$$

where J_n, J_n are the electron and holes current densities, n the electron concentration, μ_n, μ_p are the electron and holes mobilities, D_n, D_p are the diffusion coefficient of the electrons and holes which can be obtained from the Einstein relationship as

$$D_n = \frac{K_B T_L}{q}\mu_n \tag{2.15}$$

$$D_p = \frac{K_B T_L}{q} \mu_p \tag{2.16}$$

The transport equations governing charge flow, and the fields driving charge flow are the main kernels which have to be solved self-consistently and simultaneously. The electrostatic potential is related to the space charge density using Poisson equation as follow:

$$div(\varepsilon \nabla \psi) = -\rho \tag{2.17}$$

where ε is the local permittivity, ψ is electrostatic potential, and ρ is the local space charge density which is the sum of contributions from all mobile and fixed charges (i.e., electrons, holes and ionized impurities). The electric field is calculated from the gradient of the potential as:

$$\overrightarrow{E} = -\nabla \psi \tag{2.18}$$

In this work, we consider the exact time saving (classical calculation) and the though time consuming quantum mechanical description (Poisson-Schrödinger). Well known drift diffusion model is also used for 2D and 3D simulations. We compare two approaches and see what effect is obtained by each approach. The goal is to conduct a systematic theoretical study, to obtain an encompassing picture of the physics of GaN planar and GaN tri-gate HEMTs. Therefore, several simulation setups and runs are conducted and this required model validation to calibrate the simulator.

Regardless of the transport models, there are also other issues to be considered such as the effect of quantum confinement in the channel perpendicular to the direction of current flow. This is normally done by simultaneous self-consistent solutions of the Schrödinger and Poisson equations using Nextnano^3 simulator [55]. As a solution, we obtain the sub-band energies, the corresponding wave functions and the spatial distribution of the associated electrons. This means a significant additional computational effort in the device simulations. Therefore, approximate solutions are often used.

Figure 2.8 shows a comparison between classically (2D Poisson) calculated electron sheet density for planar and tri-gate GaN HEMTs using Nextnano^3 and TCAD Silvaco. Both structures have the same layer sequence a 1 μm GaN buffer, a 14 nm $Al_{0.3}Ga_{0.7}N$ barrier and 2 nm GaN cap layer. The electron sheet density is calculated classically by solving of Poisson equation.

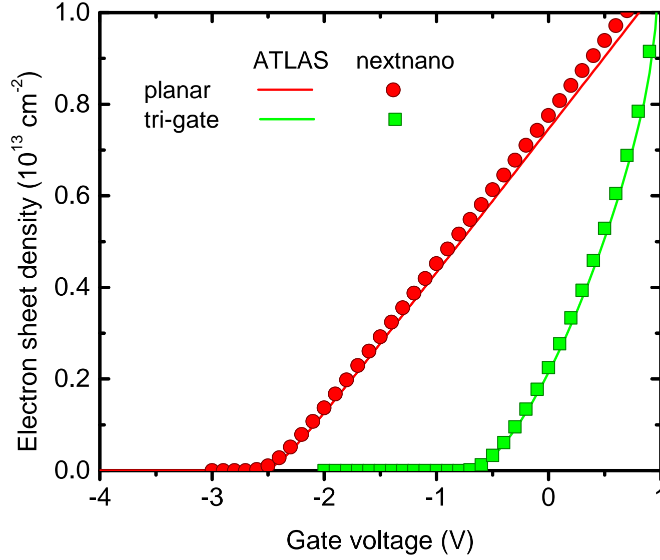

Figure 2.8: A comparison between classically (2D Poisson) calculated electron sheet density for planar and tri-gate GaN HEMTs using Nextnano^3 and TCAD Silvaco. Both structures have the same layer sequence: 1 μm GaN buffer, a 14 nm $Al_{0.3}Ga_{0.7}N$ barrier and 2 nm GaN cap. For GaN tri-gate HEMTs, the gate width w is 50 nm and h is 30 nm and depth d is 30 nm. The planar device has a gate width of 1 μm.

2.2.2 Traps

Since HEMT structures are consisting of several layers, defects are expected to be present within either individual layers and interfaces. Existence of crystal defects and impurities in semiconductor materials have been shown to be caused by the presence of impurities in the bulk or dangling bonds at the interface. This, however, affects the electrical characteristic of semiconductor devices by changing the density of space charge at the interface. Depending on where this defects are spatially or eclectically, some of these defects may acts as donor or acceptor type [39],[58], [59]. Such influence is considered in Poisson's equation.

$$\rho = q(p - n + {N_D}^+ - {N_A}^-) - Q_T \tag{2.19}$$

where n and p are the electron and holes concentrations, ${N_D}^+$ and ${N_A}^-$ are the ionized donor and acceptor impurity concentrations, Q_T is the charge caused by defects and traps.

$$Q_T = q({N_{tD}}^+ + {N_{tA}}^-) \tag{2.20}$$

where ${N_{tD}}^+$ and ${N_{tA}}^-$ are the ionized donor-like and acceptor-like traps.

2.2.3 Simulation of 2DEG in GaN-Based Devices

In the two investigated layer sequences, we assume that the AlGaN and AlInN barriers are grown on relaxed GaN buffer, thus both spontaneous and piezoelectric polarizations are pointing in the same direction. The total polarization charge in general is defined here as the sum of spontaneous and piezoelectric polarizations. It is shown that the bound charge density (σ) is associated with a gradient of polarization (P) in space which are calculated is given by:

$$\sigma = -\nabla . P \tag{2.21}$$

The difference in polarization charge at the interface between the AlGaN and GaN leads to a polarization sheet charge:

$$\begin{aligned} \sigma_{AlGaN/GaN} &= P_{GaN} - P_{AlGaN} \\ &= (P^{sp}_{GaN} + P^{pz}_{GaN}) - (P^{sp}_{AlGaN} + P^{pz}_{AlGaN}) \end{aligned} \tag{2.22}$$

and at the interface between the AlInN and GaN:

$$\begin{aligned} \sigma_{AlInN/GaN} &= P_{GaN} - P_{AlInN} \\ &= (P^{sp}_{GaN} + P^{pz}_{GaN}) - (P^{sp}_{AlInN} + P^{pz}_{AlInN}) \end{aligned} \tag{2.23}$$

Here, P^{pz}_{GaN} is assumed zero because bulk GaN buffer layers are assumed relaxed (no strain). An accumulation of free electrons at the GaN interface will compensate the induced sheet charge at the AlGaN interface, and the sheet electron concentration ($n_s(x)$) can be calculated as follow [48, 49]:

$$n_s(x) = \frac{\sigma(x)}{q} - \frac{\epsilon_0 \epsilon_r(x)}{q^2 d}[q\phi_b(x) + E_F(x) - \Delta E_c(x)] \tag{2.24}$$

where σ is the total polarization induced charge, q the electron charge, d the thickness of the AlGaN/AlInN barrier, $q\phi_b$ the Schottky barrier of the gate on top of the barrier, E_F the position of the Fermi level with respect to the edge of GaN conduction band energy, ϵ_0, ϵ_r are the vacuum and relative permittivities and ΔE_c is the offset of conduction band energy at the barrier/GaN interface. From Eq 2.24 it is clear that the sheet concentration charge strongly depends on the Al-content in the $Al_xGa_{1-x}N/Al_xIn_{1-x}N$ and/or on the barrier thickness. Figure 2.9

illustrate of the bound interface of GaN, AIN and InN, also the influence of varying the Al-content on total resulting interface charge.

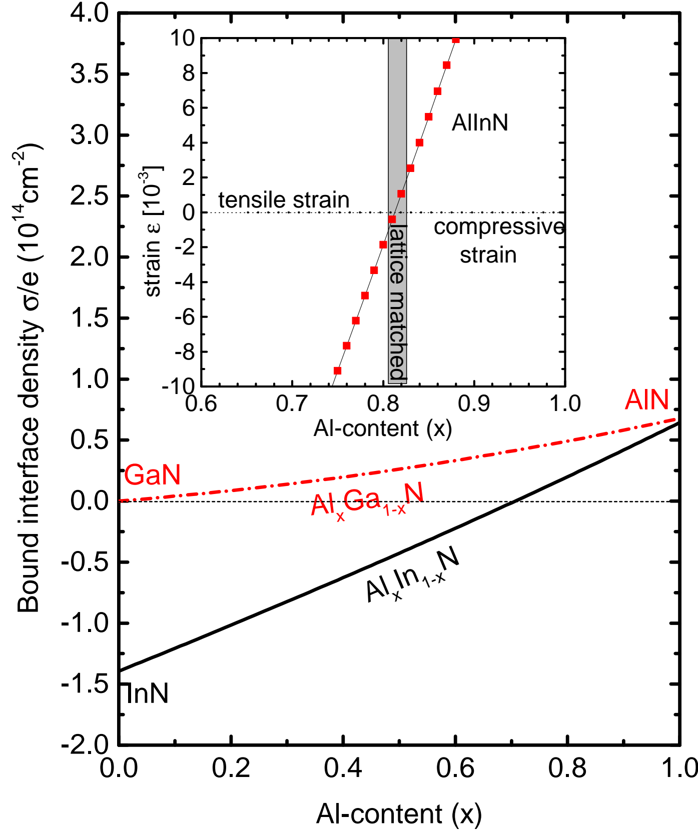

Figure 2.9: Bound interface density of GaN,AlN and InN crystals as a function of the alloys composition x where the dependence of biaxial strain is assumed in the basal plane [48]. Inset: show the tensile and comprehensive strains of the $Al_xIn_{1-x}N$ barrier as a function of the alloy composition. The $Al_xIn_{1-x}N$ barrier is lattice matched at $x = 0.82$ (strain is zero).

As a result of the spontaneous and piezoelectric polarization charges, even without a doping in the barrier a high density 2DEG is achieved at the interface between AlGaN/GaN. In the simulation, this is done by introducing a fixed sheet charge (e.g., positive at the AlGaN/GaN interface and negative at the cap/AlGaN interface).

The energy band diagram and sheet density for zero applied voltage ($V_{GS} = 0$, where V_{GS} is the gate-source voltage and V_{DS} is the drain-source voltage) for the two investigated planar and tri-gate structures are shown in Fig. 2.10. The layer sequence consists of a 120 nm AlN nucleation layer, a 2 μm GaN buffer/channel layer, a 22 nm $Al_xGa_{1-x}N$ barrier with Al content $x = 0.22$, and a 3 nm GaN

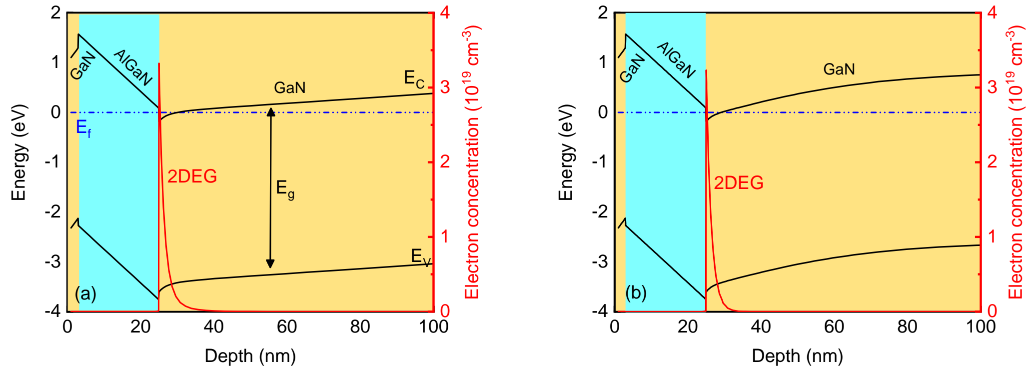

Figure 2.10: Simulated energy Band diagrams and electron densities underneath the gate region of AlGaN/GaN HEMT structure with 22 nm barrier and a 2 nm cap thickness (a) planar (b) in a vertical cut-plane through the channel of GaN tri-gate HEMT structure close to the side−gate Schottky contact.

cap. A passivation layer of 100 nm Si_3N_4 is deposited on the cap between the source/drain and gate electrodes, and a Ni/Au gate with length L_G of 100 nm is wrapped around the body from three sides (i.e., on top of the GaN cap and at the sidewalls). The source-gate and gate-drain distance L_{SG}, L_{GD} are 0.7 μm. The GaN tri-gate HEMTs device has 100 nm wide body, a 100 nm etch depth h, a 100 nm long fin (only underneath gate) and the separation between adjacent bodies is d = 100 nm.

2.2.4 Carriers Mobility and Saturation Velocity

The velocity of electron in the channel depends on the electric field and the mobility at low field based on the following relationship:

$$v = \mu_n E \tag{2.25}$$

where μ_n is the electron mobility and E is the applied electric field. Considering that velocity is increasing by increasing applied electric field based on Eq. 2.25, and that the mobility of electrons in AlGaN/GaN HEMT is affected by scattering in the semiconductor crystal, having a good mobility model in the simulation tool will lead to a better and accurate simulation.

The carrier mobility for III-nitride materials at low field presents a linear dependency on the field (ohmic). Hence, mobility is a constant and called low field mobility. However, at higher applied fields, it no longer linearly depends on the

field, but rather has a sub-linear field dependency. For calculating the mobility at the fields, the Farahmand Modified Caughey Thomas Model (FMCT model) is used. This model is a composition N and temperature T dependent model and a result of fitting like Caughey model to Monte Carlo data [60], [61]. The carrier mobility at a low field based on that model is described as follow:

$$\mu_0(T,N) = \mu_{min}\left(\frac{T}{300}\right)^{\beta} + \frac{(\mu_{max}-\mu_{min})\left(\frac{T}{300}\right)^{\delta}}{1+\left[\frac{N}{N_{Ref}\left(\frac{T}{300}\right)^{\gamma}}\right]^{\alpha(T/300)^{\varepsilon}}} \tag{2.26}$$

Here N is the doping level, T is the lattice temperature, μ_{min} and μ_{min} are the minimum and maximum expected mobility values, N_{Ref} is the total doping concentration, β, α, δ, γ, ε are parameters describing the shape of mobility characteristic. These parameters are determined by fitting measured mobility data, and it can be found in [61] for various nitride materials.

For high field mobility is same model is used within this work. This model is based also on a fit to Monte Carlo for bulk III-nitride and could be specified using the following dependence.

$$\mu_n(E) = \frac{\mu_0(T,N) + v_n^{sat}\left(\frac{E^{n_1-1}}{E_c^{n_1}}\right)}{1+a\left(\frac{E}{E_c}\right)^{n_2}+\left(\frac{E}{E_c}\right)^{n_1}} \tag{2.27}$$

where $\mu_0(T,N)$ is the low field mobility resulting from Eq. 2.26 and v_n^{sat} is the saturation velocity. The parameters in Eq. 2.27 are determined from Monte Carlo data for bulk III-nitride [60]. This model is used within this work for predicting current using 2D and 3D device simulation and is found to be in a good agreement with measurement. Figure 2.11 demonstrates the used specific III-nitride steady-state electron drift velocity compared to measured ones versus electric field for GaN material system.

2.2.5 Metal-Semiconductor Contacts

Contacts are important parts of HEMTs as they play a role in defining the carrier transport to/from the semiconductor and the metal contact of the HEMTs. The metal contacts here can be classified into two types, namely Schottky and ohmic contacts.

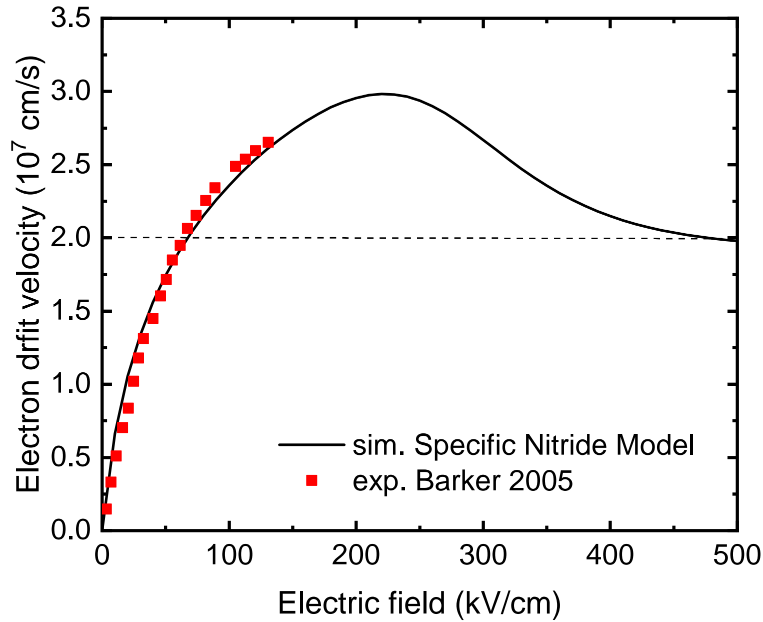

Figure 2.11: Electron velocity vs electric field in AlGaN/GaN where the carrier mobility is extracted using the FMCT model in comparison to measured data[62].

2.2.5.1 Schottky Contacts

Schottky contacts show rectifying current-voltage characterics like conventional pn diodes. If such contacts are reverse biased, only a small reverse current flows, while in the forward direction, large currents can flow. In GaN HEMTs, the gate is a Schottky contact. Since for proper HEMT operation the gate current should be as small as possible, the Schottky gate contact is either reversed biased or only a small forward bias is applied to keep the gate current low. The barrier height for Schottky contacts on wide bandgap materials like GaN strongly depends on the work function of the metal (e.g., Nickel, Platinum, Gold, etc.) as shown in Tab. 2.1. In general, Schottky contacts can be formed using both n-type and p-type semiconductors.

The surface potential of the Schottky contact is given by:

$$\psi_s = \chi + \frac{E_g}{2q} + \frac{kT_L}{2q} \ln \frac{N_C}{N_V} - \phi_c + V_{applied} \tag{2.28}$$

where χ is the electron affinity of the semiconductor material, E_g is the energy bandgap, N_C is the effective density of states in the conduction, N_V is the effective

Table 2.1: Metal contacts and their workfunctions

Metal	Workfunction (eV).
Galliumn (Ga)	4.20
Silver (Ag)	4.26
Aluminum (Al)	4.28
Titanium (Ti)	4.33
Silicon (Si)	4.52
Gold (Au)	5.10
Nickel (Ni)	5.15
Platinum (Pi)	5.65

density of states in valence band and T_L is the ambient temperature. The work function for the Schottky contact in Nextnano^3 is defined as:

$$\phi_c = \chi + \phi_B \tag{2.29}$$

where ϕ_B is the barrier height at the metal-semiconductor interface in eV which is defined as is the energy difference between the band edge with majority carriers and the Fermi energy of a metal. In GaN HEMTs, a voltage is applied to the gate electrode, modulates the 2DEG at the AlGaN/GaN interface and also modulates the drain to source current.

In TCAD Silvaco, If the thermionic emission model is enabled of the CONTACT statement then the quasi-Fermi levels, ϕ_n and ϕ_p, are no longer equal to $V_{applied}$. Instead, these parameters are defined by a current boundary conditions at the surface. In our investigation we enable a thermionic emission Schottky contact with tunneling and barrier lowering. In the simulations we consider the default values defined by the simulator for the used tunneling models and only m^* is modified to bring the simulated gate leakage current into an agreement with the experimental data. This value for effective electron mass m^* is found to be 1.45 for the conventional planar GaN HEMT.

2.2.5.2 Ohmic Contacts

Ohmic contacts represent the second type of metal-semiconductor contacts. In contrast to Schottky contacts, they show a low resistance regardless of the polarity of the applied voltage. In GaN HEMTs, source and drain are Ohmic contacts.

2.2.6 Material parameters

The simulation of GaN based HEMT using Nextnano[3] or TCAD Silvaco requires certain models and definitions to describe the material parameters of nitride compounds. It worth to mention here that Nextnano is used to calculate sheet densities, while TCAD is used to calculate current and RF characteristics for GaN HEMTs. Although TCAD Silvaco contains several built-in models and material properties, one has to consider the most appropriate values since a range of numbers already exist in the literature. The material parameters as used in the simulations are summarized in Tab. 2.2. The material parameters needed for the simulations are obtained as follows. The effective electron masses for GaN and AIN are taken from [48],[49] and the corresponding masses for $Al_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ are calculated by linear interpolation.

$$m^*_{\parallel}(AlGaN) = 0.322x + 0.186(1-x) \tag{2.30}$$
$$m^*_{\perp}(AlGaN) = 0.329x + 0.209(1-x) \tag{2.31}$$

$$m^*_{\parallel}(AlInN) = 0.322x + 0.186(1-x) \tag{2.32}$$
$$m^*_{\perp}(AlInN) = 0.329x + 0.209(1-x) \tag{2.33}$$

The bandgap E_G for the AlGaN and AlInN are obtained using the nonlinear interpolation scheme from [63].

$$E_G^{AlGaN}(x) = [6.13x + 3.42(1-x) - 1.0x(1-x)]e.V \tag{2.34}$$
$$E_G^{AlInN}(x) = [6.13x + 1.95(1-x) - 5.4x(1-x)]e.V \tag{2.35}$$

and the conduction band offset ΔE_C for the AlGaN and AlInN are obtained using the nonlinear interpolation scheme

$$\nabla E_C^{AlGaN}(x) = 0.63(E_G^{AlGaN} - 3.42) \tag{2.36}$$
$$\nabla E_C^{AlInN}(x) = 0.63(E_G^{AlInN} - 1.95) \tag{2.37}$$

the dielectric constant is calculated as follow:

$$\varepsilon_r^{AlGaN}(x) = 0.03x + 10.28 \tag{2.38}$$
$$\varepsilon_r^{AlInN}(x) = 4.33x + 10.28 \tag{2.39}$$

Table 2.2: Material parameters used for the simulation (effective masses in growth direction and perpendicular to the growth direction, relative dielectric constant, nonparabolicity of the Γ valley, band gap, conduction band offset, polarization bound charge).

Parameter	GaN	$Al_{0.22}Ga_{0.78}N$	$Al_{0.83}In_{0.17}N$	AlN	Ref.
$m^*_{\parallel}(m_0)$	0.186	0.216	0.278	0.322	[63]
$m^*_{\perp}(m_0)$	0.209	0.235	0.284	0.329	[63]
ε_r	10.28	10.29	11.04	10.31	[63]
$\alpha(eV^{-1})$	0.363	0.335	0.258	0.237	[63]
$E_G(eV)$	3.42	3.845	4.657	6.130	[63]
$\Delta E_C(eV)$	-	0.267	0.78	1.707	[63]
$\sigma(cm^{-2})$	-	9.63×10^{12}	2.38×10^{13}	-3.49×10^{13}	[48]

The Schottky barrier height ϕ_B of 1.0 eV is assumed for the gate metal on GaN and of 1eV + ΔE_C for the gate on AlGaN. Note that although a ϕ_B of 1eV is a typical value for Ni/Au contacts on n-type GaN [64]. The mobility model is calibrated to reproduce the same current for the reference planar device, and the value needed to bring simulated and measured data into an agreement is found to be 1000 cm^2/V.s when no extra contact resistances are applied to the source and drain.

2.3 Calibration of Simulation Tool

In order to accurately simulate the device performance, some assumptions/modifications to the simple GaN HEMT structure is made. The planar GaN HEMT layer sequence used for model calibration similar to [65] consists of a 120 nm AlN nucleation layer, a 2 μm GaN buffer/channel layer, a 22 nm $Al_xGa_{1-x}N$ barrier with Al content $x = 0.22$, and a 3 nm GaN cap. A passivation layer of 100 nm Si_3N_4 is deposited on the cap between the source/drain and gate electrodes. The source-gate and gate-drain distance L_{SG}, L_{GD} are 0.7μm.

- The FMCT model is used for the low field mobility while the nitride specific field dependent mobility models are used for high field which is shown to produce good results. The model is perfectly predict the low R_{on} and the I-V curves and the transfer characteristics of GaN HEMTs without modifying the parameters of the FMCT model for the GaN material.
- As Silvaco ATLAS recommends not to use the polarization statements for GaN-based FET devices but to use fixed interface charges, a fixed interface

charges between GaN/AlGaN and AlN/GaN layers is introduced in the simulation (as shown in Tab. 2.2. The polarization charges at the interfaces are shown to predict the device maximum drain current and the gate threshold voltage without any adjustment.

- In the two used simulators (i.e., Nextnano and TCAD) there is no default value for the Schottky gate work function, therefore, the value has to be manually inserted.

- To simulate the current characteristics of the GaN HEMT device using ATLAS Silvaco, the influence of traps in bulk was also considered by introducing acceptor-like traps in the bulk with activation energy of 0.64eV and a density of 1.3×10^{16} cm^{-3}. Normally, doping of the GaN buffer is compensated with Fe to suppress bulk leakage in the off-state, however deep traps due to process damage is not prevented. Therefore, in the investigated GaN HEMT structure a slight background doping effects is assumed to compensate this affect.

Shown in Fig. 2.12 are the measured and simulated transfer characteristics for the planar GaN HEMT structure (i.e., with and without traps in the bulk) . As can be seen, when assuming the above mentioned density of traps in the bulk, a good agreement between measured and simulated results are achieved.

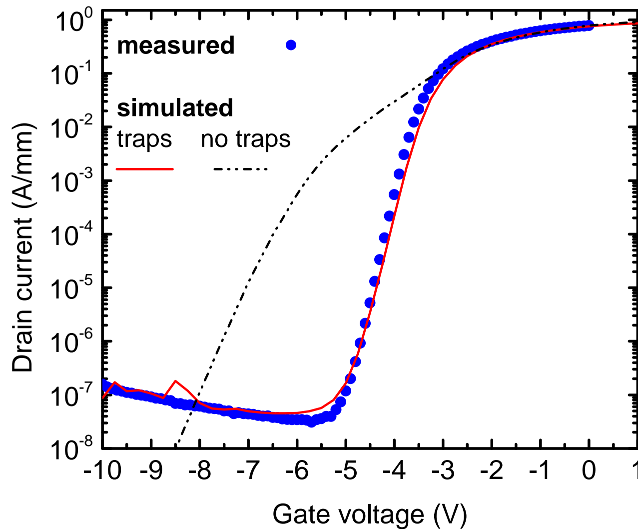

Figure 2.12: A comparison between simulated vs. measured (device is fabricated by IAF) transfer characteristics for planar GaN HEMT (V_{DS} =3V).

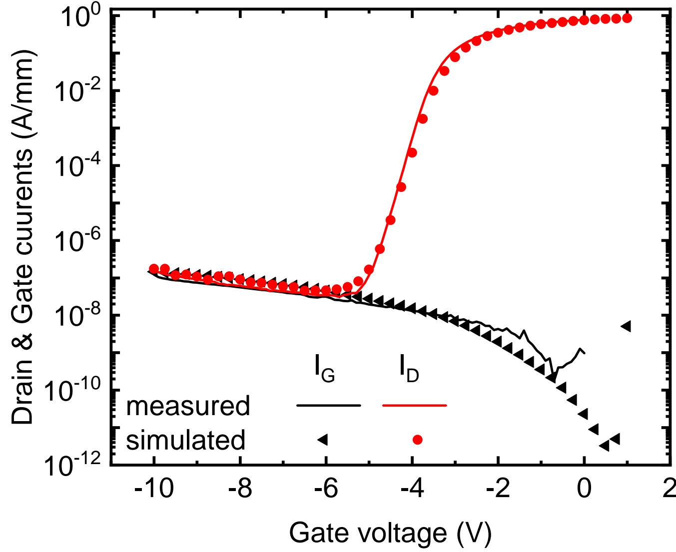

Figure 2.13: Simulated vs. measured (device is fabricated by IAF) transfer characteristics and gate leakage current (V_{DS} =3V).

Figure 2.13 shows that by using the universal tunneling model and the phonon-assisted tunneling model, we were able to predict the experimental leakage current.

2.4 GaN-based HEMTs Device Figure of Merits

2.4.1 DC Characterization

The DC characteristics (transfer and output) are good performance metrics. The transfer characteristic shows the drain current I_{DS} as a function of gate bias voltage (V_{GS}) at a fixed drain voltage (V_{DS}) and is shown in Fig. 2.14a. An important DC figure of merit is the threshold voltage V_{Th} and is depicted in Fig. 2.14a. It is defined as the minimum required voltage to switch on the conducting channel starts to form. The current at where $V_{Th} = V_{GS}$ is defined as the threshold current:

$$I_{Th} = \frac{w_{eff}}{L_G} 10^{-7} \qquad (A) \tag{2.40}$$

where w_{eff} is effective gate width and L_G is the gate width. On the logarithmic scale of Fig. 2.14a, it can ne seen that in the subthreshold region where $V_{GS} \leq V_{Th}$,

the drain current is very small.

Further information can be gained from the DC output characteristics, which show the drain current I_{DS} as a function of drain bias V_{DS} for several gate bias V_{GS} as depicted in Fig. 2.14b. Here, two regions are distinguished: the linear region ($V_{DS} < V_{GS} - V_{Th}$) and the saturation region (e.g., pinch off). In linear region, the current depends on the electric field, because the saturation velocity in the channel is proportional to electric field. In this case, current flowing from source to drain can be give by:

$$I_{DS} = qn_s v_{eff} W \qquad (A) \tag{2.41}$$

where n_s is the sheet charge concentration,v_{eff} is the effective electron velocity and W is the gate width.

For HEMT devices with large gate lengths, the drain current in the saturation region is almost independent of the drain voltage V_{DS} and mainly determined by the gate bias V_{GS}. However, the output characteristics shown in Fig. 2.14b, is that of a short gate transistor and one can observe that drain current has a prominent dependency on V_{DS} due to short channel effects. Some of the DC characteristics can be also an indicator for the AC performance of a transistor. A good example here is the extrinsic transconductance (g_m), which can be extracted from the DC-transfer characteristics by taking the first derivative of drain current (I_{DS}) with respect to the gate voltage V_{GS} at a fixed drain voltage.

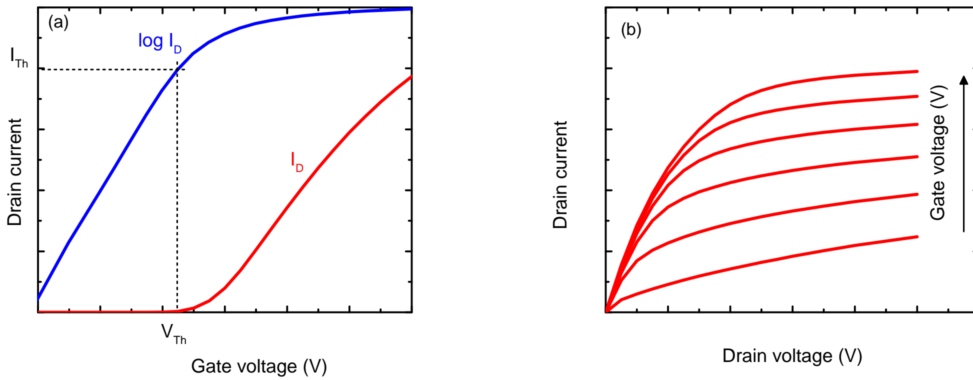

Figure 2.14: Typical (a) transfer (b) output characteristics for GaN HEMT structure.

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=const} \tag{2.42}$$

The drain conductance g_{ds} can also be extracted from the DC characteristics and provide a good indicator on the existence of short channel effects.It also affects RF performance, and should be as small as possible. The conductance g_{ds} quantifies the drain current variation caused by a variation of the drain source voltage at a fixed gate bias.

$$g_{ds} = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}=const} \tag{2.43}$$

On the other hand, the inverse slope of the logarithmic drain current in the subthreshold region as a function of gate bias is called subthreshold swing (SS) and is calculated as:

$$SS = \left(\frac{\partial(\log I_{DS})}{\partial V_{GS}}\right)^{-1} \tag{2.44}$$

Ideally, good transistors are supposed to switch off right after threshold voltage, but in reality this is not really feasible as short channel effects become severe.

Another quantity used as a metric of short channel effects is the so called drain-induced barrier lowering (DIBL). Normally, for long gate devices, the potential barrier between source and drain is mainly controlled by the gate bias. However, as the gate length is intensively reduced, the potential barrier will be also reduced by the positive drain source voltage as shown in Fig. 2.15. As a consequences, the DIBL effect is causing a reduction of the threshold voltage V_{Th} value with increasing V_{DS} as:

$$DIBL = \frac{\Delta V_{Th}}{\Delta V_{DS}} \tag{2.45}$$

2.4.2 RF Characterization

As one key application of GaN HEMTs is RF power applications, relevant RF figure of merits derived from AC small signal analysis are introduced in this section. The cutoff frequency f_{T} and the maximum frequency of oscillation $f_{\max}$ are considered as the most important figures of merit for characterizing RF devices.

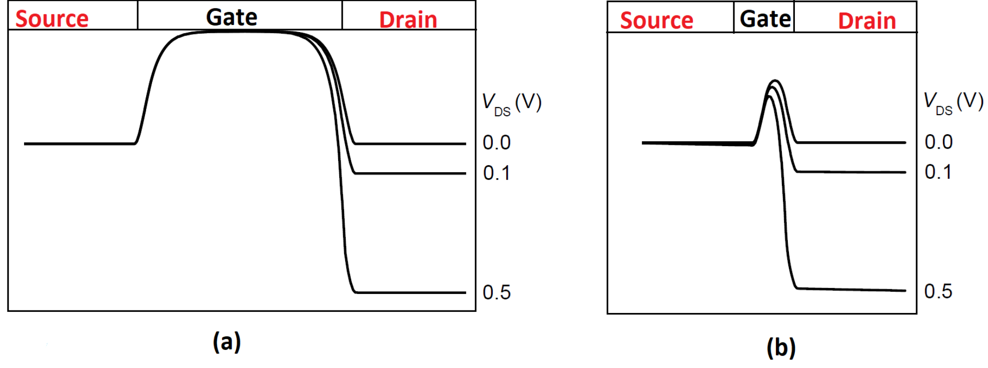

Figure 2.15: Conduction band energy in a (a) long channel (b) short channel n-type FETs.

The cutoff frequency f_T is defined as the frequency at which the short circuit current gain h_{21} is unity. Several FET small signal analysis models and equivalent circuits were reported in the literature [66],[67],[67].

In this work we only conduct a small signal analysis using DEVICE3D Silvaco, however, a practical way to estimate the both f_T and f_{max} is to use the small analysis equivalent circuit of FET shown in Fig. 2.16 with most important intrinsic (C_{GD},C_{DS},C_{GS},g_m, g_{ds} and τ) and extrinsic (R_G,R_S and R_D) elements. The intrinsic elements are bias dependent and the extrinsic ones are bias independent.

The current source in the shown equivalent circuit is defined/controlled by $g_m \times V_{GS}$ of the internal transistor. At very high frequencies, however, the drain current can no longer follow changes in gate voltage, which is taken into account by the exponential term ($e^{-j\omega_\tau}$), where $\omega = 2\pi f$ and τ is time required for electron to transport from source to drain through the channel. By analyzing the equivalent circuit in Fig. 2.16 and its elements, the following expression is used to describe the cutoff frequency f_T is given as:

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})(1 + g_{ds}(R_S + R_D)) + C_{GD}g_m(R_S + R_D)} \tag{2.46}$$

where C_{GS} is the gate-source capacitance, C_{GD} is the drain-source capacitance, R_S and R_D are the source and drain resistances. The previous formula can be simplified if we neglect the the effect of the parasitic resistances:

$$f_T \approx \frac{g_m}{2\pi C_{gg}} \tag{2.47}$$

where C_{gg} is the overall gate capacitance between the 2DEG channel and the gate (electrode and other parasitics). It is clear from Eq. 2.47, that increasing

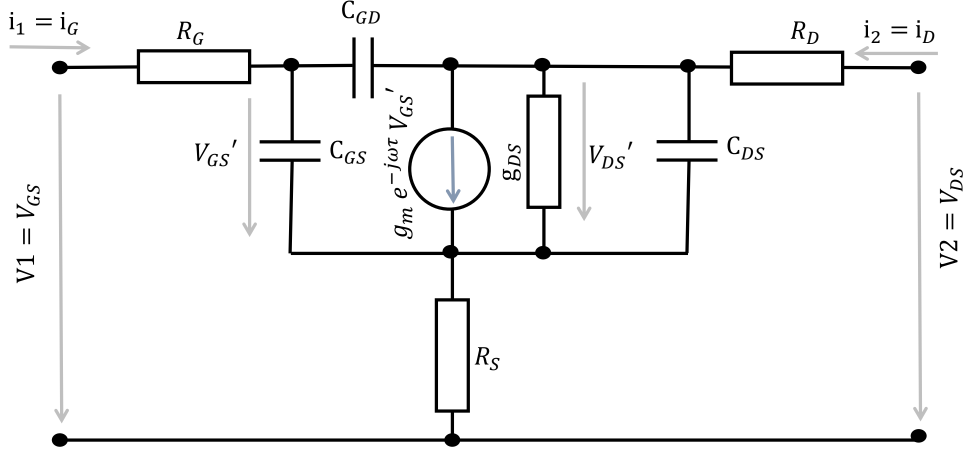

Figure 2.16: Small signal equivalent circuit diagram for FET with parasitic elements..

the transconductance g_m while keeping the gate capacitance C_{gg} fixed, will leads to an increase in the cutoff frequency f_T, and this is will be one of our research focus in addition to reducing the parasitic capacitance.

For some application such as power amplifiers (PA), maximum frequency of oscillation f_{max} is the most important figure of merits. The maximum frequency of oscillation is important figure of merit, in which it is preferred to maximize f_{max} value in order to deliver large signal gain and ensure that the maximum frequency of oscillation is several times higher than operating frequency as this will define the gain and efficiency. Here, f_{max} is defined as the frequency at which the unilateral power gain (G_p) is unity. In relation to cutoff frequency f_T, maximum frequency of oscillation f_{max} can be written as:

$$f_{max} = \frac{f_T}{4\sqrt{g_{ds}(R_G + R_D + R_S) + \frac{(2R_G + R_D + R_S)}{C_{gd} f_T}}} \tag{2.48}$$

where R_G denote the gate resistance, C_{GD} is the gate-drain capacitance. Although, increasing cutoff frequency f_T will as a result lead to an increase of f_{max}, reducing other parasitics (capacitances and resistances) are also seen to improve the value of f_{max}. Previous equation can be simplified by omitting the parasitic

resistances:

$$f_{max} \approx \sqrt{\frac{\pi f_T}{8C_{GD}R_G}} \tag{2.49}$$

In the last equation, R_G could play a key role in defining the f_{max} value based on the gate electrode design.

2.5 Summary

In this chapter, we have provided basics of GaN HEMTs, presented a brief history on GaN as a material for semiconductor technology and the advantages of such material in the RF electronics. Further, the structures, operations and the important characteristics of the conventional GaN HEMT structures are provided. A systematic calibration of GaN-based HEMTs experimental measurements to physically based simulation programs is done. Most accurate yet simple physical models were chosen for better reproducing the GaN-based HEMTs.

Special attention was given to the calibration and comparison with the experimental data in terms of subthreshold characteristics for the analysis of the device leakage currents. These prior to simulation steps guarantee that the GaN-based device simulation will be useful and helpful for the design and physical insight analysis which also help through development of semiconductor devices.

Chapter 3

DC performance of GaN Tri-gate HEMTs

In the present chapter, we perform a systematic theoretical study to get insights in the physics of AlGaN/GaN tri-gate HEMT structures, to investigate the effect of different design parameters on the threshold voltage, current density, electron density, short channel effects, electric field and breakdown voltage. Furthermore, we provide design guidelines for normally-off tri-gate HEMTs.

The fabrication of the tow main investigated structures in this work was performed by using plasma-assisted molecular beam epitaxy (PA-MBE) on 4H-SiC [65] and Metal-organic chemical vapor deposition (MOCVD) on sapphire substrates [31]. The epitaxial structure in [65] consists of a 120 nm AlN nucleation layer, a 1.8 μm GaN buffer/channel layer, an $Al_xGa_{1-x}N$ barrier with Al content x (two Al-concentration are used 22 and 32%), and a 3 nm GaN cap. Initial mesa isolation, deposition and annealing process are followed to form Ti/Al-based metal stacks ohmic contacts on the source and drain. Electron-beam lithography and plasma-enhanced chemical vapor deposition (PECVD) are used then to form a 100 nm long fin-shaped tri-gate bodies. A passivation layer of Si_3N_4 is deposited on the cap between the source/drain and gate electrodes Ni/Pt/Au-based Schottky gate electrode wrapped around the body from three sides (i.e., on top of the GaN cap and at the sidewalls) with a gate length of 100 nm is defined after removing the passivation layer from the gate area.

In [31], the epitaxial structure consists of a 1.5 μm un-intentionally doped GaN buffer layer, a 1 nm thick spacer AlN layer, a 13 nm $Al_xGa_{1-x}N$ barrier with Al content x = 30 %, and a 2 nm GaN cap. Initial mesa isolation, deposition and annealing process are followed to form Ti/Al/Ni/Al-based metal stacks ohmic

contacts on the source and drain. Multi tri-gate bodies were then patterned using electron-beam lithography, and transfer this pattern into AlGaN/GaN heterostructure using chlorine-based low-rate etching process. The GaN tri-gate HEMT has a fin length of 1 μm and gate length of 2 μm. The source-gate and gate-drain distance L_{SG}, L_{GD} are varied. In the experimental structures, the

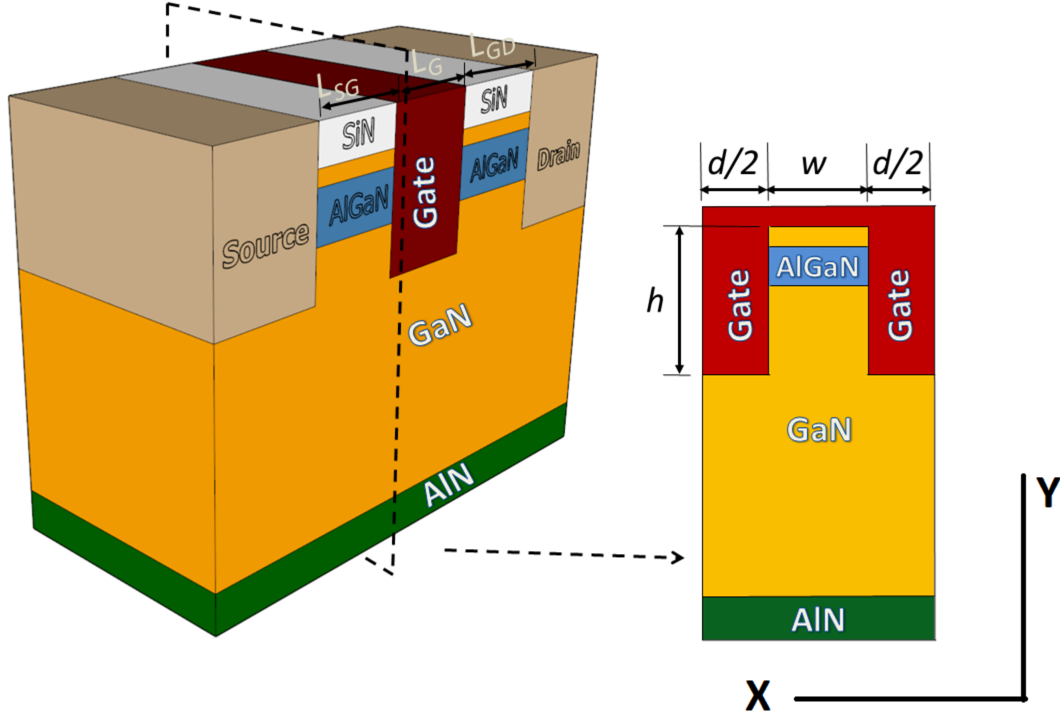

Figure 3.1: Schematic view of the investigated AlGaN/GaN tri-gate HEMTs structure

unintentional n-type doping of the GaN buffer has been compensated with Fe to suppress bulk leakage in the OFF-state. This is taken into account in the simulation, by acceptor-like traps with activation energy of 0.64 eV and a density of 1.3×10^{16} cm^{-3}. All other layers are assumed undoped. Figure 3.1 presents a schematic view of tri-gate GaN HEMTs structure.

3.1 Electron Distribution

In this part, we calculate the two-dimensional carrier distribution in the body either quantum-mechanically (self-consistent solution of the Schödinger and Poisson equations) or classically (solution of the Poisson equation) using the 2D Poisson-Schödinger solver (Nextnano[3]). For accounting the 2DEG in the simulation, fixed

polarization charges (positive) at the AlGaN/GaN and (negative) at the cap/AlGaN are introduced.

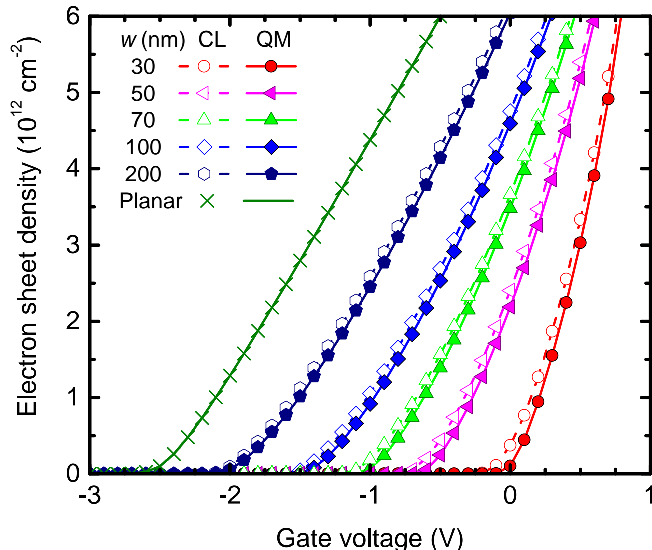

Figure 3.2: Average 2DEG sheet density vs. gate voltage for the GaN tri-gate HEMT structure from Fig. 3.1 (fully strained $Al_{0.3}Ga_{0.7}N$ barrier) for different body widths obtained by classical (CL) and quantum-mechanical (QM) simulation.

The structure investigated in this section is shown in Fig. 3.1. It corresponds to the design of the experimental normally-off tri-gate AlGaN/GaN HEMTs from [31] and consists of a 1μm GaN buffer/channel layer, an $Al_{0.3}Ga_{0.7}N$ barrier, a 2 nm GaN cap, and a Ni/Au gate. The body width w is varied in our study, the body height h (i.e., the body etching depth) is 30 nm, and the separation between two adjacent bodies is $2\times d = 60$ nm. Unless otherwise stated, the barrier thickness is 14 nm, and the Al content x of the barrier is 0.3. For $Al_{0.3}Ga_{0.7}N$/GaN, an overall bound polarization charge density σ at the AlGaN/GaN interface of 1.38×10^{13} cm^{-2} is obtained assuming no relaxation (i.e., full strain). The material parameters needed for the simulations are summarized in Tab. 2.2.

First the average 2DEG sheet density n_{sh-av} of the structure from Fig. 3.1 is calculated for different body widths ranging from 30 to 200 nm and for a planar structure (without side-gates) as a function of gate voltage V_G. It is given by eq. 3.1 and takes the depleting effect of the sidewall-gates into account.

$$n_{sh-av} = \frac{1}{w}\int_0^w n_{sh}(x)dx \tag{3.1}$$

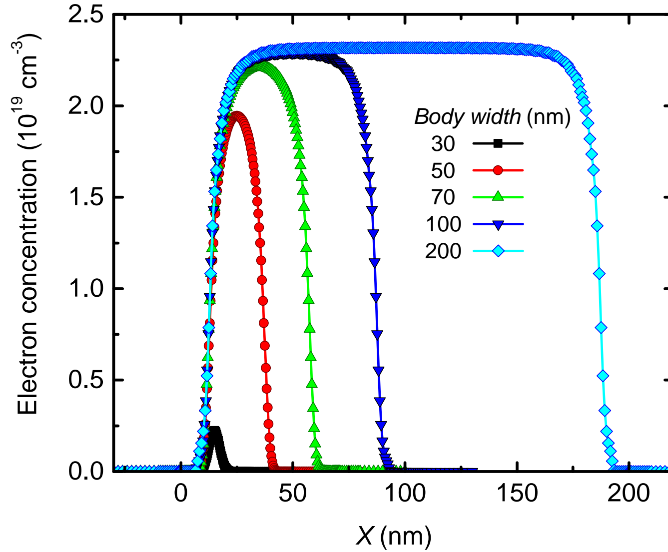

Figure 3.3: The effect of body width reduction on electron distribution in the 2DEG of the structure from Fig 3.1 for zero applied gate voltage assuming zero relaxation. Shown are the electron concentrations in the depth y where for each structure the maximum electron concentration occurs, i.e., the position of the peak in Fig. 3.4, upper right.

The results depicted in Fig. 3.2 clearly show that for a given gate voltage the sheet density rapidly decreases for shrinking body widths and that the threshold voltage increases from -2.4V for the planar structure to above zero (i.e., normally-off) for the 30 nm wide body. Moreover, the slope of the n_{sh}-V_G curves increases for decreasing body widths. This means, in other words, that due to the side-gate effect both the transconductance and the gate capacitance (normalized by the body width w) increase in GaN tri-gate HEMTs structures with narrow bodies. A comparison of classical and quantum-mechanical results reveals that for the planar structure the results are quite similar while for the GaN tri-gate HEMT structures, as expected, the quantum-mechanical simulation predicts a lower sheet density and a more positive threshold voltage than the classical simulation.

In Fig. 3.3 the effect of a body width reduction on the carrier distribution is shown. While in the wide structures (w = 100 and 200 nm) the electron concentration in the body center is not affected by the sidewall-gates but controlled only by the top-gate, in the more narrow structures the peak concentration at the body center decreases rapidly with decreasing body width. The 2DEG in the most narrow structure (w = 30 nm) is almost entirely depleted by the sidewall-gates.

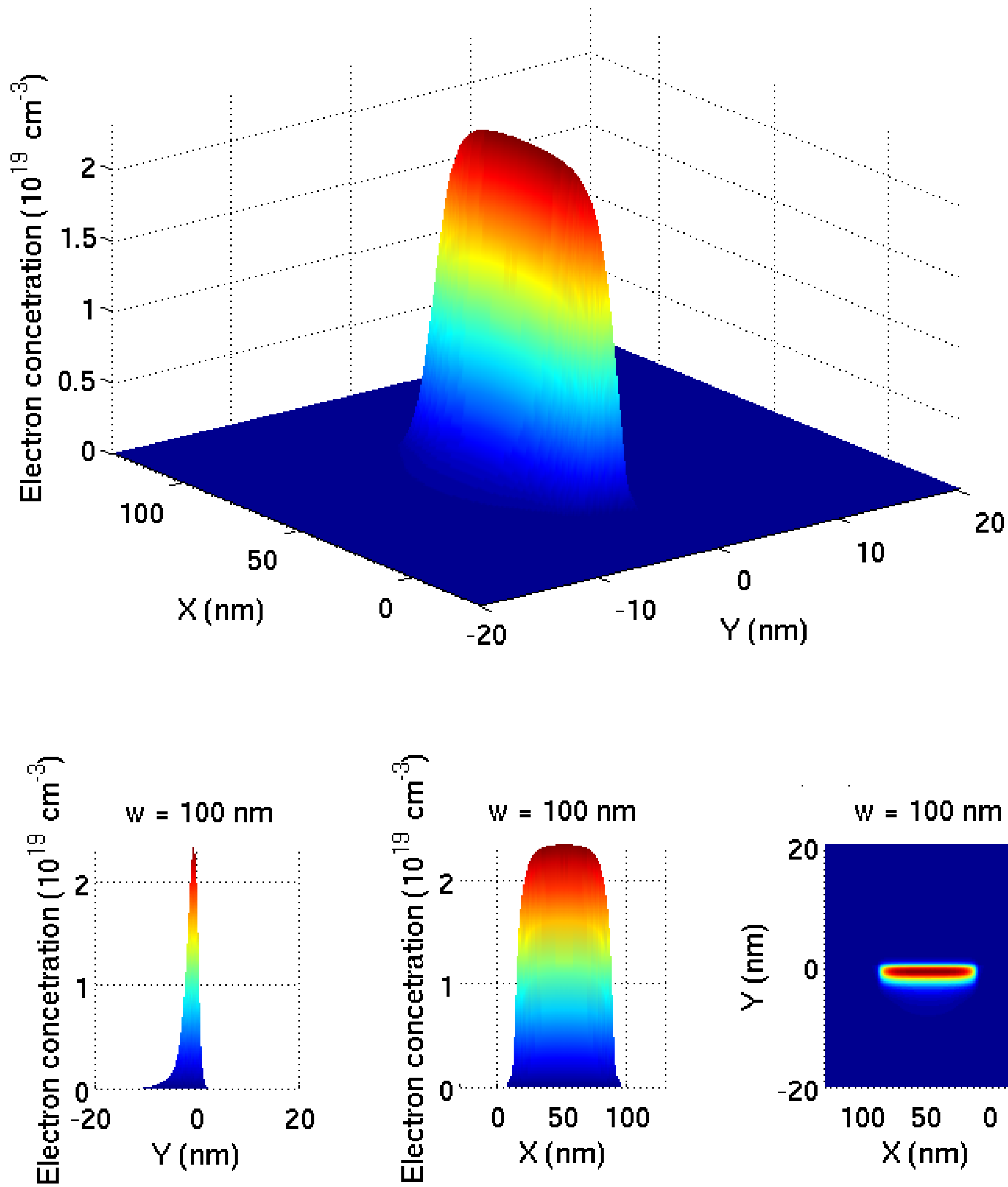

Figure 3.4: Electron distribution in the body of a 100 nm wide GaN tri-gate HEMT structure (compare Fig. 3.1). Upper left: 2D view. Upper right: 1D side view. Lower left: 1D front view. Lower right: 2D top view. In all plots, the AlGaN/GaN channel interface is located at y = 0 between x = 0 and x =100 nm. The top gate contact is located at y = 16 nm.

Figure 3.4 shows the quantum-mechanically calculated electron distribution in the GaN tri-gate HEMT structure from Fig 3.1 with 100 nm wide body for zero applied gate voltage. The depletion zones at both sidewalls can clearly be identified.

3.2 I-V characteristics

In this section we calculate I-V characteristics of the GaN HEMTs by conducting 3D simulations considering full device structure using ATLAS simulator from Silvaco. The investigated device has a similar layer sequence as shown in Fig 3.1. The layer sequence consists of a 120 nm AlN nucleation layer, a 2 μm GaN buffer/channel layer, a 22 nm $Al_xGa_{1-x}N$ barrier with Al content $x = 0.22$, and a 3 nm GaN cap. A passivation layer of 100 nm Si_3N_4 is deposited on the cap between the source/drain and gate electrodes, and a Ni/Au gate with length L_G of 100 nm is wrapped around the body from three sides (i.e., on top of the GaN cap and at the sidewalls). The source-gate and gate-drain distance L_{SG}, L_{GD} are 0.7 μm.

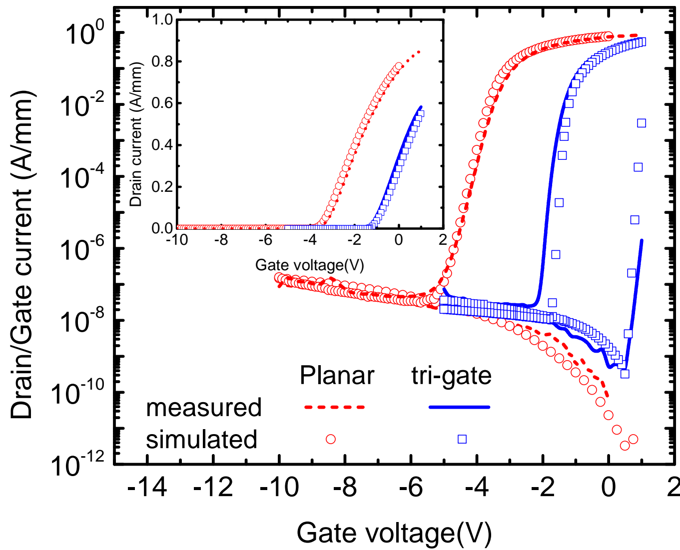

Figure 3.5: A comparison between simulated vs. measured transfer characteristics and gate leakage currents for planar and tri-gate GaN HEMTs (V_{DS}=3V). Inset: transfer characteristics comparison on linear scale.

In the experimental structures, the unintentional n-type doping of the GaN buffer has been compensated with Fe to suppress bulk leakage in the OFF-state. This is taken into account in the simulation, by acceptor-like traps with activation energy of 0.64 eV [39] and a density of 1.3×10^{16} cm^{-3}. All other layers are assumed undoped. For $Al_{0.3}Ga_{0.7}N$/GaN heterojunctions, an overall polarization bound charge density at the interface of 9.63×10^{12} cm^{-2} has been obtained when no relaxation is assumed (i.e. fully strained AlGaN barrier). A Schottky

barrier height ϕ_B of 1.0 eV is assumed for the gate metal on GaN. An electron low-field mobility of 1020 cm^2/Vs is chosen to reproduce the measured transfer characteristics of experimental devices, which is in good agreement with Hall measurements.

First, a planar GaN HEMT with a layer sequence as in Fig. 3.1 is simulated to calibrate the simulator. The drain and gate currents as functions of gate bias are calculated. The I-V characteristics of the planar and tri-gate devices are calculated and compared to experimental results calculated at $V_{DS} = 3$V as shown in Fig. 3.5. From Fig. 3.5, it can be seen, that the measured and simulated transfer characteristics and gate leakage currents are in good agreement. It is noted here that GaN tri-gate HEMT design have shown similar leakage currents at a reverse bias. However, the tri-gate tends to higher leakage currents (about two orders of magnitude at $V_{GS} = 0$) at forward bias. The GaN tri-gate HEMT leakage trend at forward bias is quite complex due to the 3D Schottky contact compared to the planar counter part which has more positive onset Schottky-gate voltage.

The drain current-voltage (I_{DS}-V_{DS}) characteristics are of the planar and tri-gate GaN HEMTs with similar layer sequences as in this section are shown in Fig. 3.6. The GaN GaN tri-gate HEMT is show pronounced saturation region in its output curves compared to planar counterpart, which show an increase of drain current with increasing drain voltage which is slight short channel effects (gate length = 100 nm). It is clear also, that GaN tri-gate HEMT structure is giving smaller output conductance because of less DIBL effect.

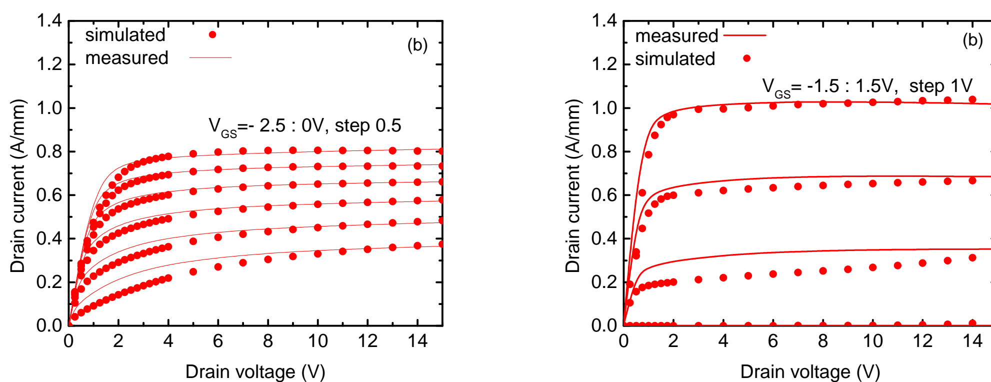

Figure 3.6: Simulated vs. measured output characteristics of the GaN (a) planar (b) tri-gate GaN HEMT.

Figure 3.7a shows a comparison between measured and simulated results for the planar and tri-gate GaN HEMTs. The GaN tri-gate HEMTs design with

different widths (w = 100 and 500 nm). The GaN tri-gate HEMT device with the 500 nm wide body has a 1μm long fin which is almost the entire distance between source and drain and the separation between adjacent bodies is $d = 500$ nm. In the narrower body device (w = 100 nm and d = 100 nm) the fin is only 500 nm long. The etch depth h is fixed to 200 nm in both devices.

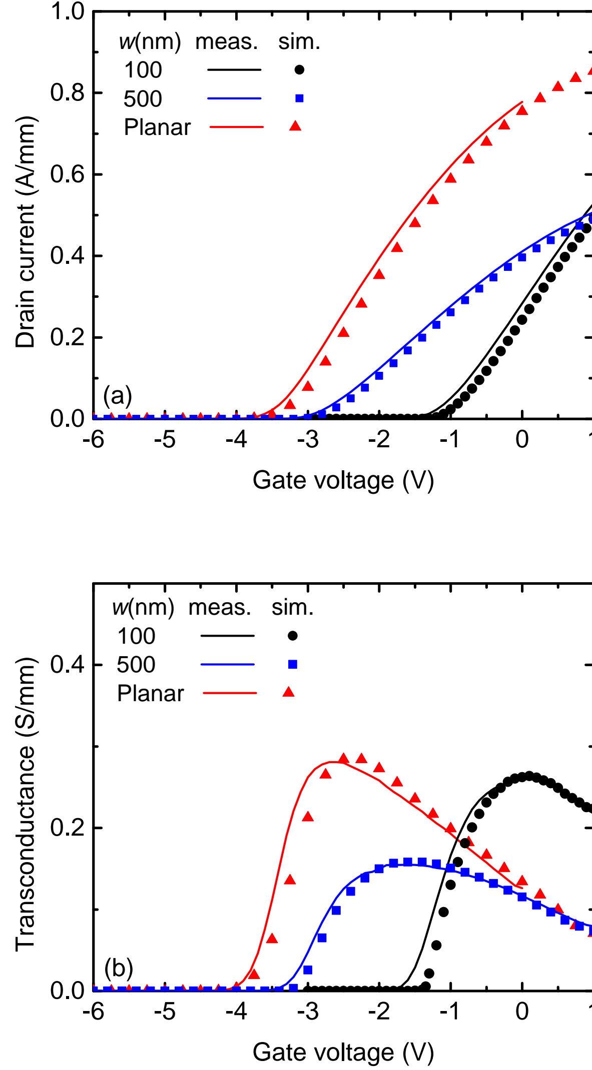

Figure 3.7: Simulated vs. measured (a) transfer characteristics (at $V_{DS} = 3V$) of planar and tri-gate GaN HEMTs with body widths of 100 and 500 nm. (b) corresponding transconductance as function of gate voltage. I_D and g_m are normalized on the total device width. For the simulated GaN tri-gate HEMT structures $w_{total} = w + d$ (compare Fig. 3.1).

The simulated I-V characteristics of the planar and tri-gate GaN HEMT devices are in good agreement with the experimental results as shown in Fig. 3.7b. As

can be seen, the GaN tri-gate HEMT with body width of 100 nm has slightly lower transconductance g_m compared to the planar counterpart, while the GaN tri-gate HEMTs with wider body (w = 500 nm) exhibits a considerably smaller g_m due to its large access resistances caused by the long fin. Moreover, Fig. 3.7b demonstrates that the simulation accurately reproduces the measured threshold voltage (V_{Th}) trend, i.e., reducing the GaN tri-gate HEMT body width leads to an increase in threshold voltage (i.e., V_{Th} becomes more positive).

3.3 Threshold voltage

Next, the effect of the body width reduction on the threshold voltage is investigated. Since in narrow bodies partial strain relaxation in the AlGaN barrier is likely to happen [34], we consider full relaxation and zero relaxation (full strain) as the two possible extreme cases. It should be noted, however, that full relaxation is not expected to occur in a wide AlGaN/GaN body and that the planar structure with full relaxation is included just for the sake of completeness.

Figure 3.8 shows the threshold voltage as a function of body width for these cases calculated both quantum-mechanically and classically. In a fully relaxed AlGaN layer only spontaneous polarization occurs and the bound polarization charge density σ at the channel GaN/AlGaN interface is 7.73×10^{12} cm^{-2}. The same bound charge but with opposite sign is found at the AlGaN/GaN-cap interface, if the cap layer is fully relaxed. If, on the other hand, the relaxation of the AlGaN layer induces strain in the cap, the absolute value of σ at the upper heterojunction would be higher and σ could reach a value of -1.29×10^{13} cm^{-2}.

As already expected from the results of Fig. 3.2, the classically and quantum-mechanically calculated threshold voltages V_{Th-CL} and V_{Th-QM} are essentially the same for the structures with wide body, while for the narrow structures V_{Th-QM} is larger (i.e., more positive) than V_{Th-CL}. For the 30 nm wide structure (no relaxation) the difference is almost 100 mV. Relaxation has a strong effect on V_{Th}. For the planar structure, the threshold voltage for zero relaxation is -2.3V compared to -0.87V for fully relaxed AlGaN and cap layers and -0.69V assuming strain in the cap induced by the relaxed AlGaN layer.

For decreasing body width the difference becomes smaller but is still about 0.45V (0.49V) for the structure with 30 nm wide body. As can be seen, normally-off operation is achieved for $w \leq 30$ nm for zero relaxation and for $w < 75$ nm assuming full relaxation. Since the impact of strain in the cap is rather small, especially in narrow tri-gate designs where partial relaxation is likely to occur,

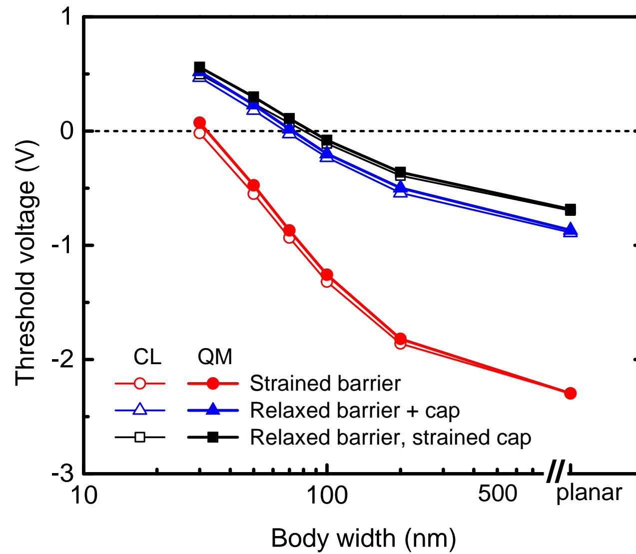

Figure 3.8: Threshold voltage of the structure from Fig. 3.1 as a function of body width assuming the extreme cases of unrelaxed (strained) and fully relaxed AlGaN barrier obtained by classical and quantum mechanical simulations. Two possible cases are considered for fully relaxed AlGaN layers: relaxed GaN cap (blue triangles) and strained cap (black squares).

we solely consider relaxed cap layers in the remainder of the work. At this place, a remark on our definition of the threshold voltage is advisable. The threshold voltage is obtained at a normalized sheet density n_{sh-Th} =3×10^{13} cm^{-2}.

3.3.1 GaN Tri-gate HEMT's Geometry Scaling

We now turn back to the two extreme cases of full relaxation and full strain (zero relaxation) and investigate the effect of the AlGaN barrier design on the threshold voltage of tri-gate AlGaN/GaN HEMTs. Figure 3.9(a) shows the threshold voltage as a function of body width for two Al contents, namely 25% and 30%. As expected, a decreasing Al content leads to a smaller polarization charge and thus to a higher (i.e., less negative) threshold voltage. However, it can be seen that in narrow-body structures the Al content has a much weaker effect on V_{Th} compared to GaN tri-gate HEMT structures with wide bodies. A similar trend can be observed, when the AlGaN barrier thickness is reduced [Fig. 3.9(b)].

In general, the threshold voltage becomes more positive, and again, the effect off the barrier design rapidly decreases for narrow body bodies. For the narrowest

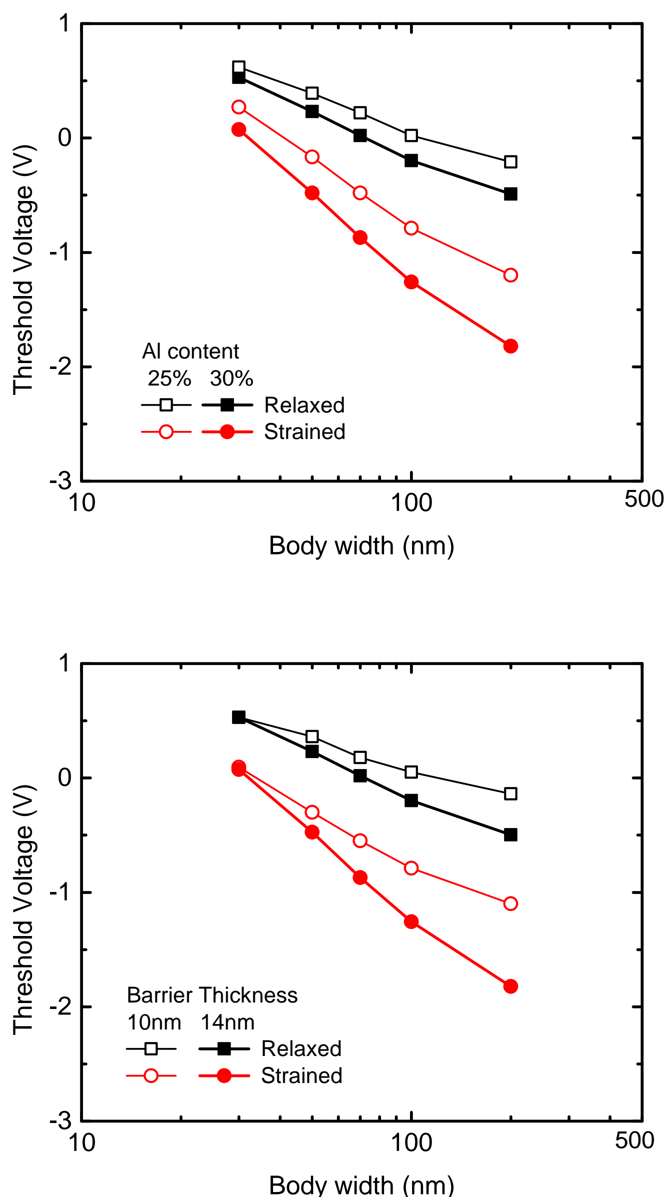

Figure 3.9: Threshold voltage of AlGaN/GaN tri-gate HEMT structures versus body width for (a) two different Al contents (25% and 30%) in the barrier and (b) two different AlGaN barrier thicknesses (10 and 14 nm).

body investigated (30 nm) the AlGaN thickness has only a negligible impact on the threshold voltage. Influence of decreasing the vertical layer design for narrow bodies is an inherent feature of the AlGaN/GaN tri-gate concept as shown in Fig. 3.9. The reason is the increasing influence of the depletion zones from the body sidewalls on the overall electrostatics, when the body width is reduced. In

narrow tri-gate bodies ($w < 70$ nm), the 2DEG density is governed by the sidewall gates (see Fig. 3.3), for which the vertical design is less important. However, the planar counter part as shown in Fig. 3.10 is dramatically affected by the barrier thickness. Threshold voltage is shifted by 7V toward negative as barrier thickness is reduced from 26 to 4 nm. It is recommended how ever to keep the channel aspect ratio $L_G/t_B \geq 5$ (t_B is the barrier thickness) to prevent sever threshold voltage shift.

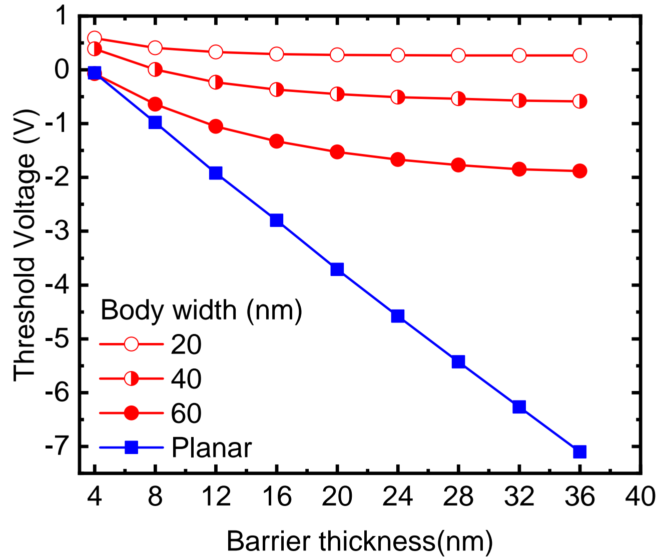

Figure 3.10: Barrier thickness scaling effect on threshold voltage of $Al_{0.3}G_{0.7}aN/GaN$ planar and tri-gate structures.

Figure 3.11 shows the threshold voltage as a function of body width where both Al content (20 and 22%) and the barrier thickness are varied (20 and 22 nm) compared to experimental results from IAF- Frauenhofer [65]. As expected, a decreasing Al content or and barrier thickness leads to a smaller polarization charge and thus to a higher (i.e., less negative) threshold voltage. However, it can be seen that in narrow-body structures the Al content has a much weaker effect on V_{Th} compared to tri-gate HEMT structures with wide bodies. The increasing influence of the depletion zones from the body sidewalls on the overall electrostatics becomes clear, when the body width is reduced.

Next, we investigate the threshold voltage dependency on the body width by varying the body width from 25 to 500 nm and compare it with the measured planar and tri-gate GaN HEMTs (w = 100 and 500 nm) results. As can be seen from Fig. 3.11, the simulation accurately reproduces the measured V_{Th} trend i.e.,

reducing the GaN tri-gate HEMT body width leads to an increase in threshold voltage (i.e., V_{Th} becomes more positive). Normally-off operation is achieved for body widths below 38 nm. Here, the threshold voltage V_{Th} is defined as the gate voltage at which the drain current decreases to 10^{-7} A$\times w_{total}/L_G$, where w_{total} is the total gate width and L_G is the gate length. Note that for tri-gate HEMT devices, the total width is defined by $w_{total} = w + d$.

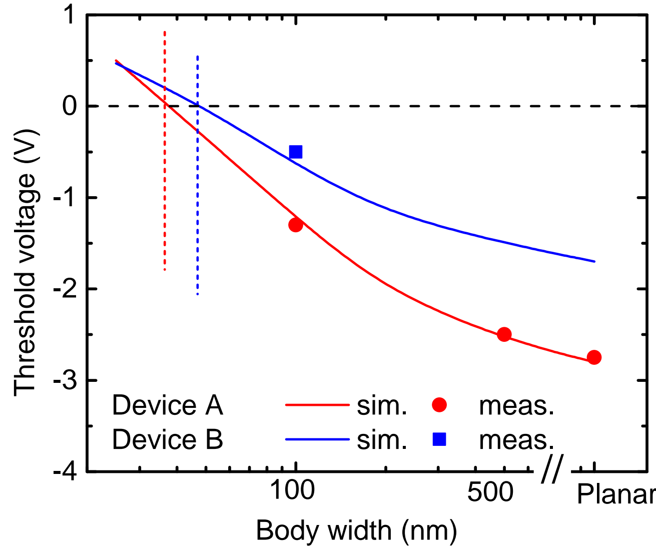

Figure 3.11: Comparison between simulated and measured threshold voltage of AlGaN/GaN tri-gate HEMT structures versus body width for two different Al contents (20% and 22%) in the barrier and two different AlGaN barrier thicknesses (20 and 22 nm).

Next the effect of the etching depth is investigated by varying the body height h for different body widths. Figure 3.12 shows the extracted threshold voltage V_{Th} vs. tri-gate body width for etching depths of 20, 30 and 50 nm. It turns out that the etching depth has a much weaker effect on the threshold voltage than the body width. The inset in Fig. 3.12 shows the threshold voltage shift ΔV_{Th} caused by an increase of the etching depth by either 10 or 30 nm from the reference value of 20 nm as function of the body width.

Obviously, there is a maximum etching depth effect on V_{Th} around a body width of 100 nm. This can be explained as follows. For narrow bodies, a small etching depth is already sufficient to guaranty full ΔV_{Th} control by the side gates. In wide bodies (i.e., in almost planar devices), on the other hand, V_{Th} is fully controlled by the top gate and the effect of the side gates is negligible. Hence,

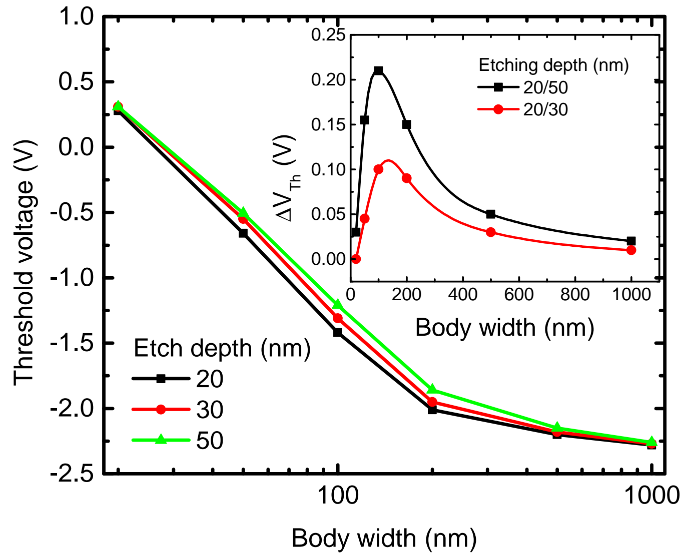

Figure 3.12: Threshold voltage of GaN tri-gate HEMT vs. body width for different etching depths. Inset: V_{Th}-shift due to an etch depth increase vs. body width.

in wide body devices the etching depth does not affect the device electrostatics. In GaN tri-gate HEMT structures with intermediate body widths, however, the 2DEG is controlled by both top gate and side gates and the electrostatics does necessarily depend to some extent on the ratio between top-gate and side-gate areas, i.e., on the etching depth.

Next the etching depth has been varied from 20 nm down to 200 nm for a GaN tri-gate HEMT with a body width of 100 nm (i.e., the body width at which the transistor is most sensitive to the etching depth). Figure 3.13 demonstrates that by increasing the etching depth V_{Th} also increases, and later starts to saturate as we reach a depth of 100 nm. Finally, for etching depths beyond 100 nm no significant change of V_{Th} can be observed. It can also be seen from Fig. 3.13 that the drain current curves for increasing etching depths become steeper, which means higher transconductance and intrinsic gate capacitance. This effect, however, saturates beyond an etching depth of 50 nm.

In Fig. 3.14, we investigate the effect of the etching depth in GaN tri-gate HEMT with gate lengths varying between 2μm and 50 nm. Our intention is to find out whether the same trend can be observed for short channel devices or not. It is clear from Fig. 3.14 that the effect of the etching depth becomes more important as the gate length is reduced. This is also confirmed by the inset in

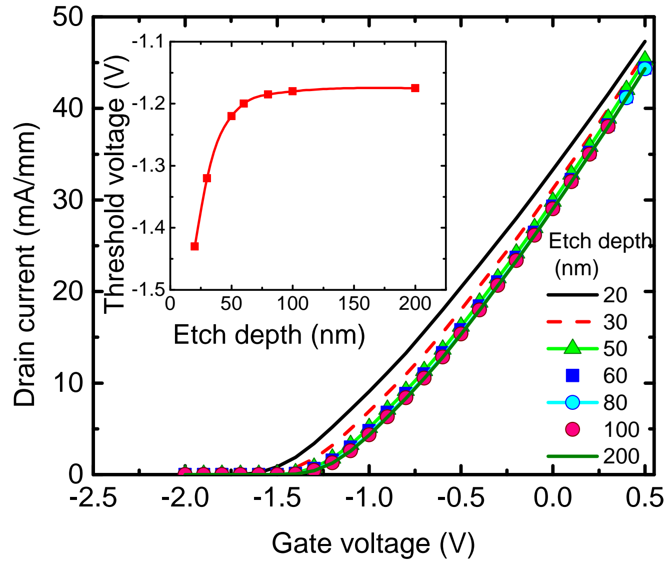

Figure 3.13: Transfer characteristics of GaN tri-gate HEMT with 100 nm wide body and different body heights. Inset: threshold voltage vs. etching depth.

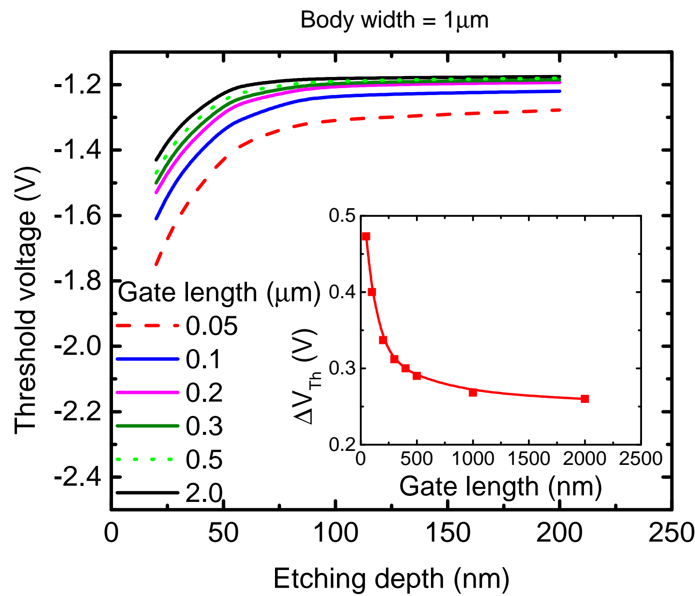

Figure 3.14: Threshold voltage of 100 nm wide GaN tri-gate HEMT with different gate lengths as function of the etching depth. Inset: maximum V_{Th}-shift due to an etch depth increase vs. gate length.

Fig. 3.14 where the threshold voltage shift ΔV_{Th} caused by an increase of the etching depth from 20 nm to 200 nm is shown as a function of the gate length.

In Fig. 3.15, the gap/separation d between two adjacent tri-gate bodies have been varied from 200 nm down to 10 nm. It is clear from the result that the separation has only small impact on threshold voltage. The gate still has a good controllability over the channel and can still deplete the channel on the side-walls.

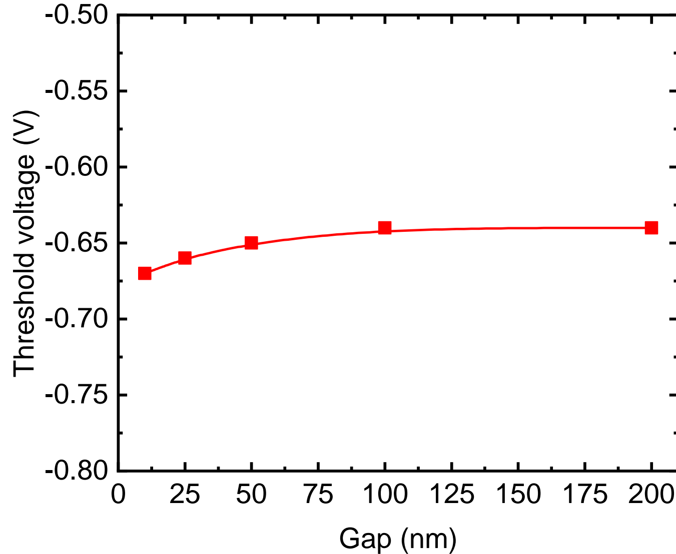

Figure 3.15: Threshold voltage of 100 nm wide GaN tri-gate HEMT as function of the separation gap g.

3.3.2 Effect of process-induced damage on side-walls

The etching process and the plasma treatment in fabricating GaN tri-gate HEMT devices is a challenge, and require very sophisticated technologies and processes. Etching induced-damage for instance is hard to completely prevent even with this sophisticated technology, examples of such variations are inconsistency in the etching depth, separation between neighboring tri-gate bodies and the body width. Such variations are shown to produce some discrepancy when simulated and experimental data are compared. Moreover, the geometry of the body is affected due to the etching damage and many experimental tri-gate FETs do not possess an ideal rectangular body but instead a trapezoidal shape is produced as shown in Fig. 3.16.

we conduct several simulations to investigate the possible impacts of the process-induced variations on the GaN tri-gate HEMTs design and performance. The

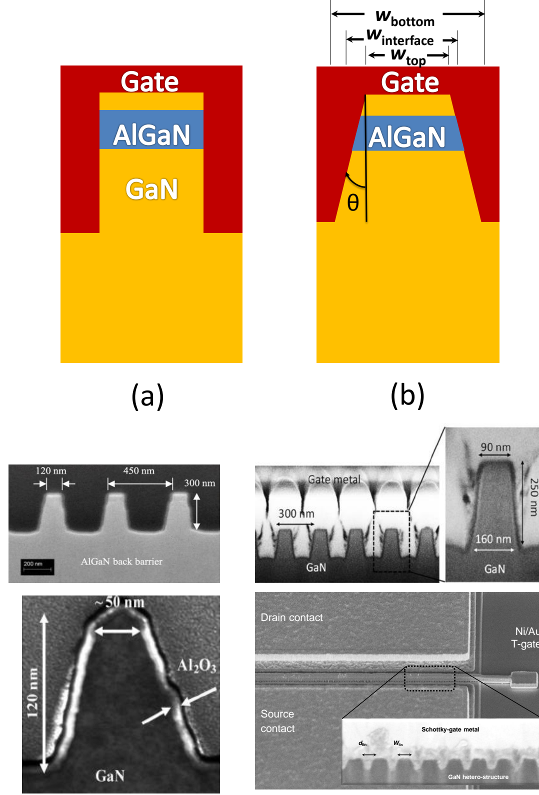

Figure 3.16: (a) Schematic view of the idle rectangular AlGaN/GaN tri-gate structure (b) schematic view of the trapezoidal shape AlGaN/GaN tri-gate structure (c) sketch of experimental non-idle (with trapezoidal shapes) tri-gate structures [65],[31],[68]

investigated scenarios as shown in Fig. 3.16. We consider the idle case (rectangular shape) as shown in Fig. 3.16a and the non-idle shape (trapezoidal) resulting from a damage on the side-walls as shown in Fig. 3.16b. For the non-idle shape we want to discover to which extend measuring the width at the top is valid although a damage is occurred . Therefore, we study three cases as shown in Fig. 3.16b , where the width is measured at top, interface(2DEG) and bottom of the side-walls.

First, we assume that the three simulated structures have in common that the width at the top, interface and bottom is the same as of the idle shape (i.e., $w_{top} = w_{interface} = w_{bottom} = 64$ nm). Figure 3.17a, shows the electron line density of the three structures along with the reference stricture (i.e., idle rectangular shape). It is clear here that only the case where the width is measured at the interface agrees with the reference case. For the other two cases, the electron density is either underestimated (i.e., width is measured at the top) or overestimated(i.e., width is measured at the bottom). The inset in Fig. 3.17a shows the electron

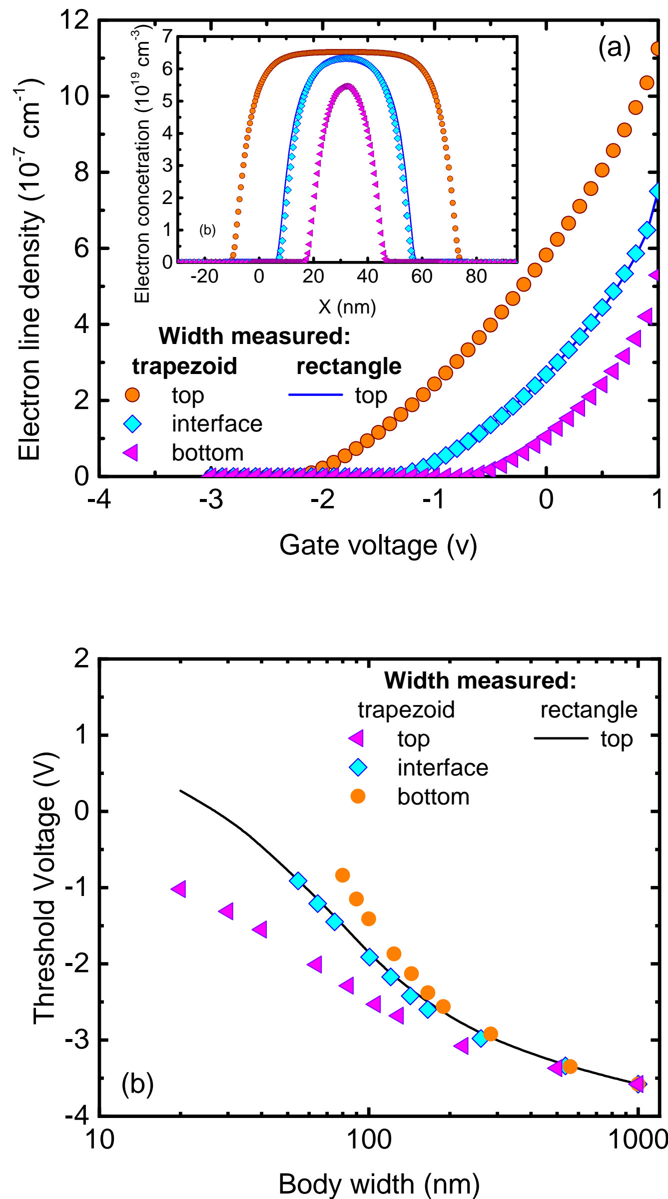

Figure 3.17: Simulated rectangular and trapezoidal shapes GaN tri-gate HEMT (a) electron line densities with varied body widths as a function of gate voltage.Inset: The corresponding electron concentrations for the simulated GaN tri-gate HEMT structures at V_G=0. (b) threshold voltage as a function of width of normalization.

distribution of the three investigated structures along with the reference device. The results show again that the distribution of the idle case and trapezoidal case (width at interface) are identical.

Next, we vary the top width of the trapezoidal shape device with keeping the

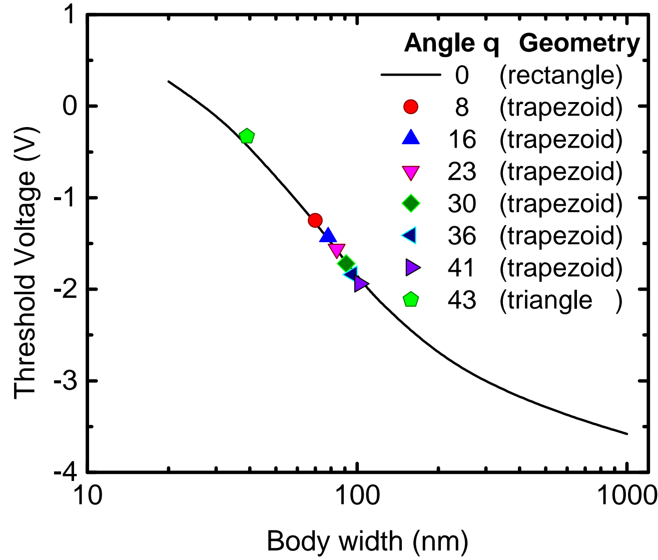

Figure 3.18: Simulated rectangular and trapezoidal shapes GaN tri-gate HEMT (a) electron line densities with varied body widths as a function of gate voltage.Inset: The corresponding electron concentrations for the simulated GaN tri-gate HEMT structures at V_G=0. (b) threshold voltage as a function of width of normalization.

angle θ fixed ($\theta = 45^o$ and the interface and bottom widths are varied accordingly). The threshold voltage as a function of the body width for the three investigated scenarios is shown in Fig. 3.17. The normalization is done in order to extract threshold voltage according to the width at each location. The results show that only if the width is measured at interface for the trapezoidal shape, we end up with the same extracted quantities as for the rectangular shape GaN tri-gate HEMT. Moreover, since the damage on side-walls is undesirable and unavoidable, because of the process complexity, it is hard to predict the width before fabrication since the idle shape is not produced. We try now to consider how bad is the damage could be on the side-wall and what effect could have on the threshold voltage if the normalization is done every time on the interface width. Figure 3.18 shows the threshold voltage of the trapezoidal shape GaN tri-gate HEMT as a function of gate voltage. This means channel width is a good reference for normalization.

3.3.3 Strain Relaxation Effects

In Fig. 3.19 the effect of a larger dielectric constant on the V_{Th-w} characteristics is shown. Assuming $\epsilon_r = 12.2$ for both GaN and AlGaN, the simulated V_{Th} for

the strained planar structure is only 0.26V more negative than the experimental value. Hence, a top gate Schottky barrier of 1.26eV brings the simulated threshold voltage of the planar device into perfect agreement with the experimental value. However, to consider the same ϕ_B value for the sidewall gates is not enough to bring the simulated V_{Th-w} curve for fully relaxed barriers, i.e. the upper limit of expected V_{Th} values, above the entire experimental V_{Th-w} characteristics. The reason is the weaker effect of the higher ϵ_r in structures with less negative

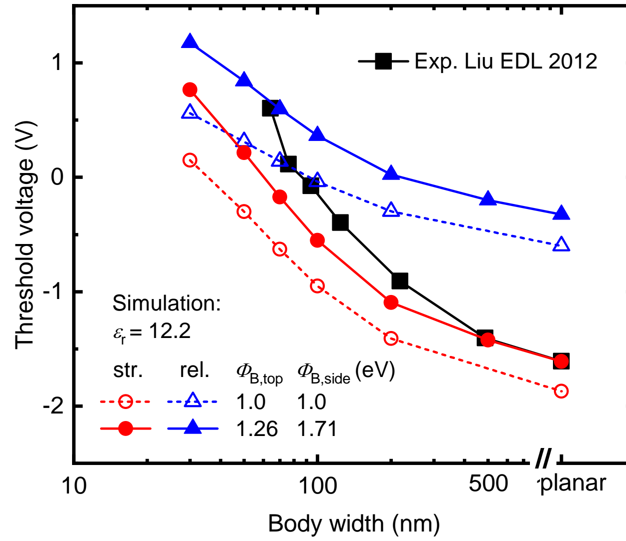

Figure 3.19: Simulated threshold voltage vs. body width assuming a relative dielectric constant of 12.2 for both GaN and AlGaN, together with experimental V_{Th} data from [31]. Two scenarios of top gate and sidewall gate Schottky barriers are considered in the simulations.

threshold voltage than that of the strained planar structure. In other words, the more positive the threshold voltage of a certain structure is (relaxed barrier, small w), the less effective is a relative increase of its gate capacitance due to a higher ϵ_r. Thus, we have to do further assumptions to push the simulated upper limit above the measured V_{Th-w} curve. A realistic assumption could be a larger Schottky barrier at the sidewalls since the surface state density at the etched sidewalls might be considerably larger than that at the protected top surface. As can be seen from Fig. 3.19, assuming a sidewall Schottky barrier of 1.71eV, i.e. the surface Fermi level is pinned exactly in the middle of the GaN band gap, the experimental V_{Th-w} characteristics is located between the simulated upper and lower limits for V_{Th}. It can be seen from Fig 3.19 that for wide bodies

the simulated curve for full strain (i.e. the lower limit: full red circles) is close to the experimental one while for more narrow bodies the experimental curve rapidly approaches the simulated V_{Th-w} characteristics assuming full relaxation (upper limit: full blue triangles). This behavior suggests that in narrow bodies partial strain relaxation plays an important role. Therefore, in a next step we investigate the degree of relaxation required to provide a better agreement with the experimental data. The degree of relaxation r can be obtained by varying the strain in the AlGaN barrier according to

$$\epsilon_{pr} = \epsilon(1 - r) \tag{3.2}$$

until the simulated threshold voltage equals the experimental one. Here ϵ_{pr} is the strain in the partially relaxed AlGaN barrier and ϵ the strain in a fully strained barrier.

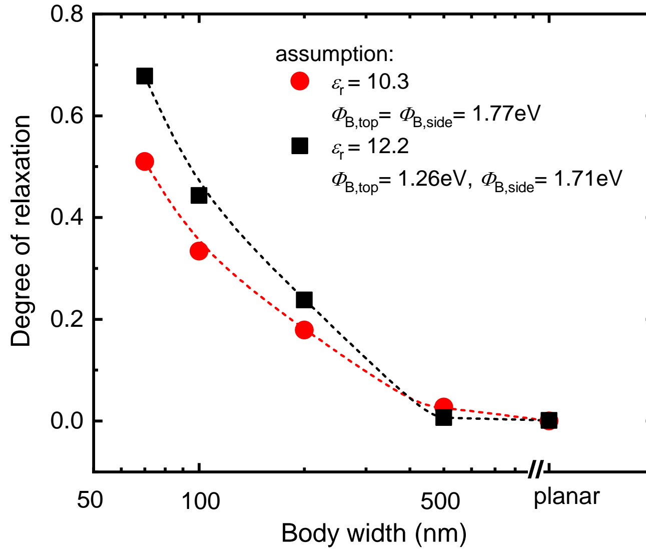

Figure 3.20: Degree of relaxation required to achieve perfect agreement between the calculated V_{Th} and the experimental data from [31]. Two different cases are considered in the simulations.

Figure 3.20 shows the degree of relaxation needed to achieve perfect agreement between the simulated and measured threshold voltages assuming (i) $\epsilon_r = 10.3$ and $\phi_{B,top} = \phi_{B,side} = 1.77$ eV and (ii) ϵ_r= 12.2 and $\phi_{B,top} = 1.26$ eV, $\phi_{B,side} = 1.71$ eV. As can be seen, in both cases partial relaxation starts to become relevant for body widths below 500 nm and for decreasing body width, r increases rapidly. This result is in good agreement with the experimental findings from [34], where

for body widths below 400 nm a decreasing strain, i.e., an increasing relaxation of the barriers in $Al_{0.26}Ga_{0.74}N$/GaN structures has been observed.

3.4 Electric Field Distribution

In the previous section, we have seen that at 100 nm etching depth the transfer characteristics as well as the V_{Th} are not sensitive regarding the etching depth. In this part we investigate the electric field distribution in an AlGaN/GaN tri-gate HEMT structure with body width of 100 nm, body height of 100 nm, and 1 μm gate. The 2D contours of the electric field in our GaN tri-gate HEMT biased at V_{GS} = 0V and V_{DS} = 3V are shown in Fig. 3.21. Also, the 2D contours of the electric field in our investigated GaN tri-gate HEMT biased at V_{GS} = -1.5V and V_{DS} = 100V are shown in Fig. 3.22. As expected, the highest field values are found at the drain end of the side gate.

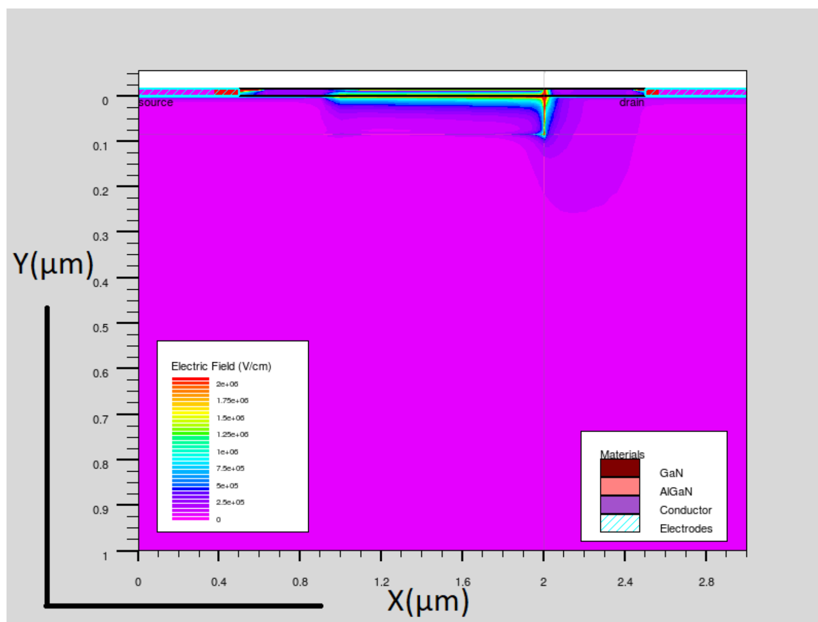

Figure 3.21: 2D contour plot of the field distribution in a vertical cut-plane through the channel of the tri-gate GaN HEMT structure close to the side−gate Schottky-contact calculated V_{DS}=3V.

In Fig. 3.23 the investigated GaN tri-gate HEMT structure is shown together with the field directions, mainly x- field (horizontal) in the direction of the channel from source to drain, y- field (vertical) from top to bottom of the device and finally z- field from sidewall toward the channel direction.

Figure 3.24 shows the components of the electric field in x, y and z directions together with the absolute value of the field in a cut-line from source to drain along

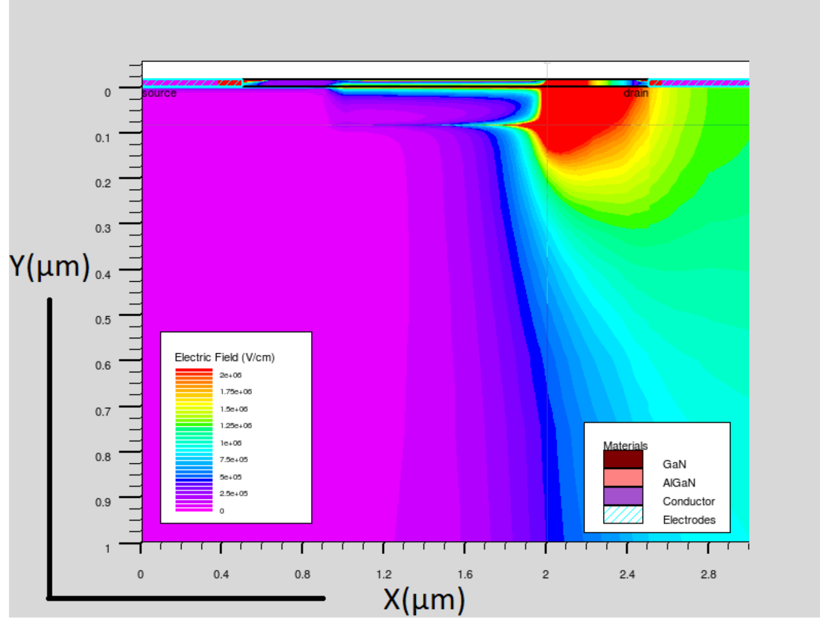

Figure 3.22: 2D contour plot of the field distribution in a vertical cut-plane through the channel of the tri-gate GaN HEMT structure close to the side-gate Schottky-contact calculated V_{DS}=100V.

the AlGaN/GaN interface close to the side gate contact. As can be seen from Fig. 3.24, a pronounced field-peak is located at the gate-edge near the drain side with an absolute value of about 2.5 MV/cm at $V_{DS} = 3$V. This is no surprise since at a sharp 90deg metal edge a singularity of the electric field must be expected. Note that such singularities are not per se a problem.

Regarding device breakdown, the ionization integral over the whole high field region is the critical quantity (i.e., the generation rate must be high in a sufficiently large volume and not only in a single spot). In the high-field region, the horizontal field components in the x- and z-directions (i.e., in length- and width- directions) are higher compared to the vertical field (i.e., in y-direction). This can be understood as follows. The vertical field is mainly caused by both the positive polarization charge at the AlGaN/GaN interface and the negative charge of the 2DEG, i.e. a positive y-field component corresponds to a quantum well containing a certain 2DEG charge, whereas a negative field denotes a fully depleted channel.

The x- and z-field components, on the other hand, do not directly depend on the polarization charge. Instead, these components are defined by the electron density distribution in the 2DEG, by the potential difference between the side-gate and drain contacts, and most importantly, by the singularity caused by the 90deg metal edge of the side gate contact.

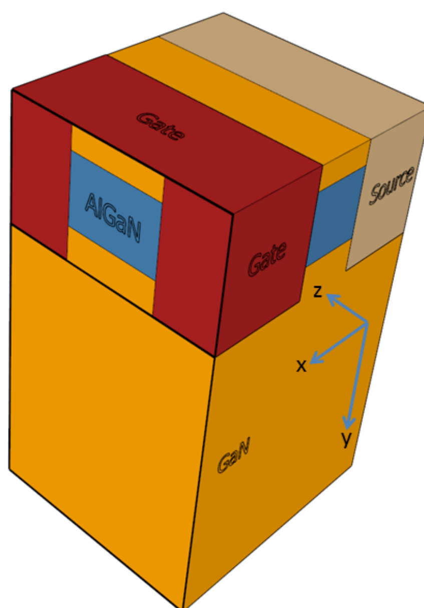

Figure 3.23: A schematic of the investigated GaN tri-gate HEMT structure.

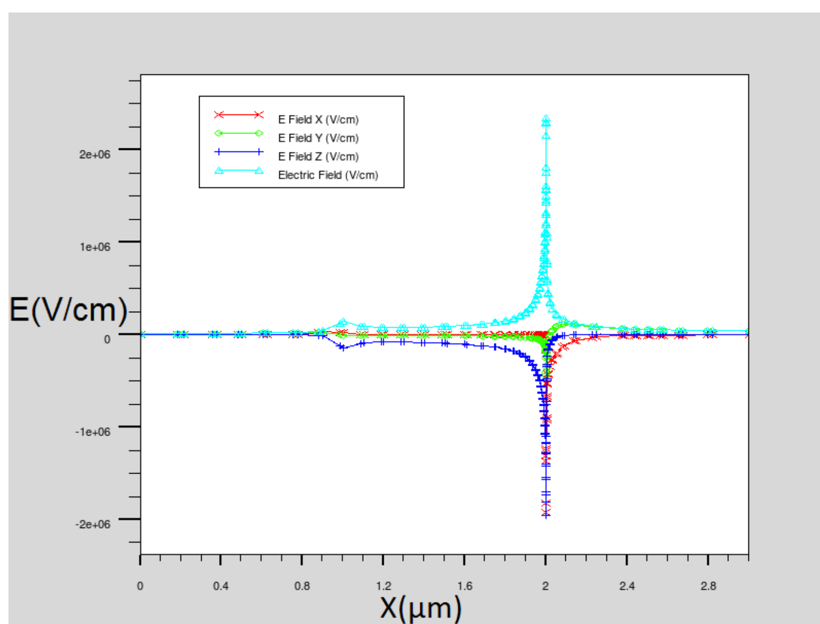

Figure 3.24: The field's components at a horizontal cut-line from source to drain at the AlGaN/GaN interface for the 2D contour plot.

Figure 3.25 shows the field components along a vertical cut-line from top to bottom along the side gate edge close to drain. Two field peaks are visible, one exactly at the AlGaN/GaN interface, and a second one at the side-gate corner. The first peak could be critical (i.e.,≈5 MV/cm) even at V_{DS} = 3V and at high

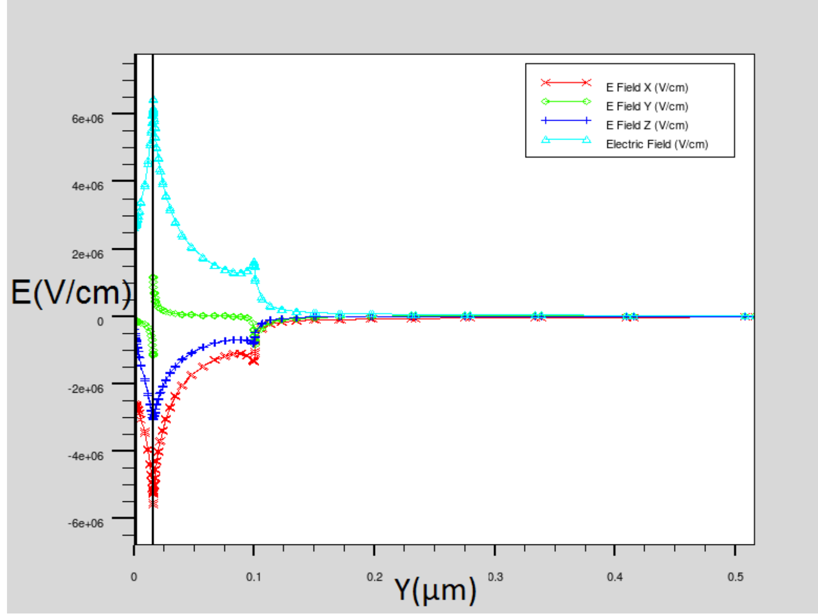

Figure 3.25: The field's components at a vertical cut-line from top to bottom along the side gate edge near the drain−side for the 2D Contour plot.

drain voltage the second peak at the corner edge also becomes significant (i.e., 20 MV/cm at V_{DS} = 100V).

In order to check whether theses calculated fields are critical or not, we first defined the critical field or breakdown field for the GaN HEMT. For the breakdown field, we chose a value of 4 MV/cm which is in the range of values found in the literature (i.e.,≈3-5 MV/cm) [64]. Based on the above discussion we defined three critical points within the structure where the bias dependence of the electric field is investigated in more detail. As can be seen in Fig. 3.26, the three points are defined at the drain-end of the gated active device region (in the GaN), point 1 close to the side-gate corner, point 2 at the contact between side-gate and AlGaN/GaN interface, and 3) at the middle of the AlGaN/GaN interface.

In Fig. 3.27, the total electric field in the three investigated points is shown as function of the drain bias in both on-state (V_{GS} = 0V) and off-state (V_{GS} = -1.5V). Also shown for comparison is the predefined critical breakdown field E_{BR} (i.e., 4 MV/cm). As can be seen from Fig. 3.27, the electric field E_3 at point 3 (i.e., mid of the channel) approaches the critical field only at higher drain voltages above 80V. At point 1 the field E_1 starts to be critical already at V_{DS} > 20V, whereas at point 2, the field E_2 is already high even at no applied drain voltage. Thus, the electric field at the side-gate contact (point 1 and 2) may be high enough to cause a tunneling current from the gate metal to the semiconductor. It can also

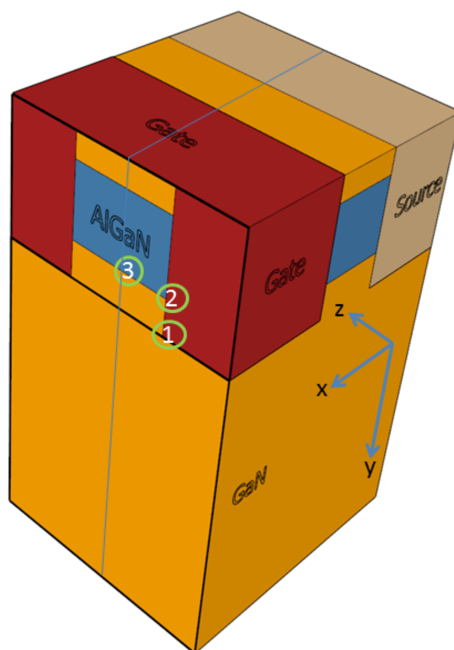

Figure 3.26: Schematic view of the investigated critical points.

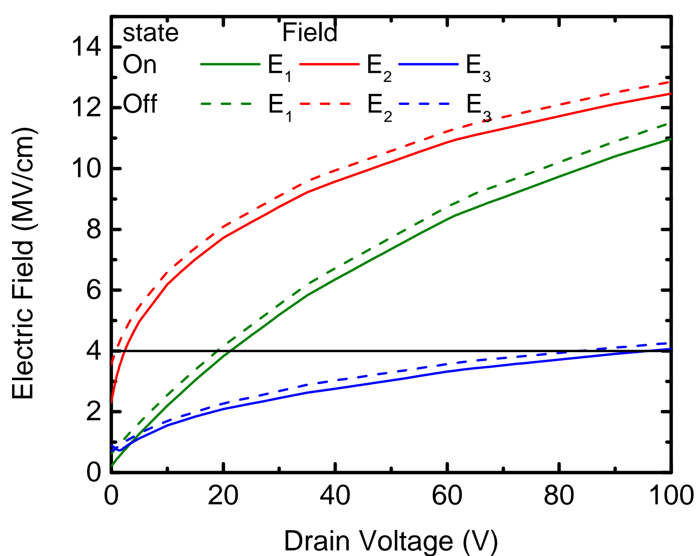

Figure 3.27: The total electric field at the investigated points the on/off states.

be observed that in general the total electric field is slightly higher at lower gate voltage (i.e., in the off state).

In Fig. 3.28a, we show the electric field components in the x, y and z directions at the three investigated points. At all three points, E_x is always the largest

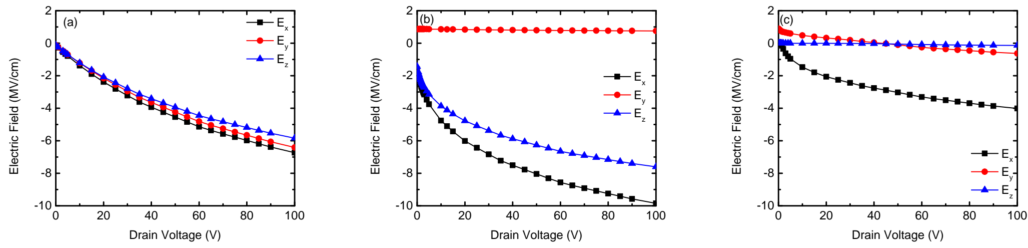

Figure 3.28: Simulated components of the electric field in the GaN tri-gate HEMT in the on-state at (a) point 1, (b) point (2), and (c) point 3.

component. In Fig. 3.23a, however, all three electric field components at point 1 (i.e., E_x , E_y and E_z) are comparable and show a similar V_{DS} dependence, i.e., all field components are zero at no applied drain voltage and increase together by applying higher drain voltage. As mentioned earlier, at higher drain voltage all three components can be considered critical. Figure 3.28b shows that E_y at point 2 remains almost constant, while both E_y and E_z fields are of high and rapidly increasing value. At point 3 (Fig. 3.28c) only E_x component can become critical at high V_{DS}. The z-field is zero due to the device symmetry and E_y remains uncritical in the entire drain voltage range. Note that although point 3 seems to be less critical when comparing the field values with those in the other two points, avalanche breakdown may be more severe in point 1 since the majority of the electron current from source to drain flows in the middle of the channel. In points 1 and 2, on the other hand, only few electrons coming from the source do exist that could cause impact ionization. However, here the electrons could tunnel from the side gate into the GaN due to the high field at the Schottky contact and then be multiplied by avalanche processes. This of course could effectively be prohibited by an oxide between the side gate and the GaN, i.e., by a MIS structure.

3.5 Short Channel Effects

Commonly, for a good transistor short channel lengths and fast carriers in the channel are mandatory. However, reducing the channel length leads to undesirable short channel effects due to the degraded control of gate over the channel and the increased effect of the drain field in the ON- and OFF-states [40],[41]. Short channel effects in the OFF-state are known to be responsible for shifting threshold voltage, increasing subthreshold swing (SS) and drain induced barrier lowering (DIBL). Moreover, short channel effect is also responsible for increasing

the output conductance (g_{ds}) in the ON-state which the end affect the device DC performance.

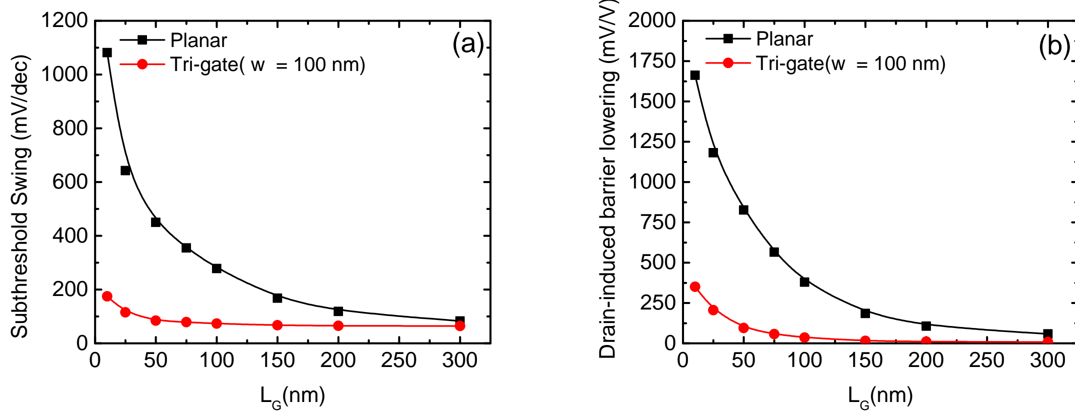

Figure 3.29: A Comparison of the scaling behavior of planar and GaN tri-gate HEMT in terms of (a) subthreshold swing and (b) drain-induced barrier lowering.

In the following, effect of gate length scaling on the DC performance in both the ON- and OFF-state is investigated. To this end, the gate lengths L_G of the planar and tri-gate GaN HEMT devices have been varied between 10 and 300 nm, while the ratios L_{SG}/L_G and L_{GD}/L_G are held fixed for fair comparison. For the GaN tri-gate HEMT design, a fixed body width is assumed (i.e., $w = 100$ nm as in the experimental device). The etch depth h as well as the gap d between adjacent GaN tri-gate HEMT bodies are kept fixed at $h = d = 100$ nm.

Figure 3.29 compares the scaling behavior of planar and GaN tri-gate HEMTs. Shown are SS and DIBL as a function of the gate length. The SS is extracted at a drain bias $V_{DS} = 3$V, while DIBL is calculated for $V_{DS} = 0.1$ and 3V. It can be seen from Figs. 3.29a 3.29b that for the GaN tri-gate HEMT device, both SS and DIBL are considerably smaller than for planar HEMTs due to the better electrostatic control in the GaN tri-gate HEMT structures. The improved channel confinement of the GaN tri-gate HEMT is shown to be effective and improves with reducing body width. On the other hand, the planar GaN structure with the same layer sequence suffers from short channel effects such as degraded SS and increased DIBL with higher applied drain voltage.

The scaling behavior of planar and tri-gate GaN HEMTs in terms of threshold voltage are shown in Fig. 3.30. The threshold voltage is extracted at a drain bias $V_{DS} = 3$V. As shown in Fig. 3.30, threshold voltage for the planar device is dramatically shifted toward negative values when the gate length is scaled below

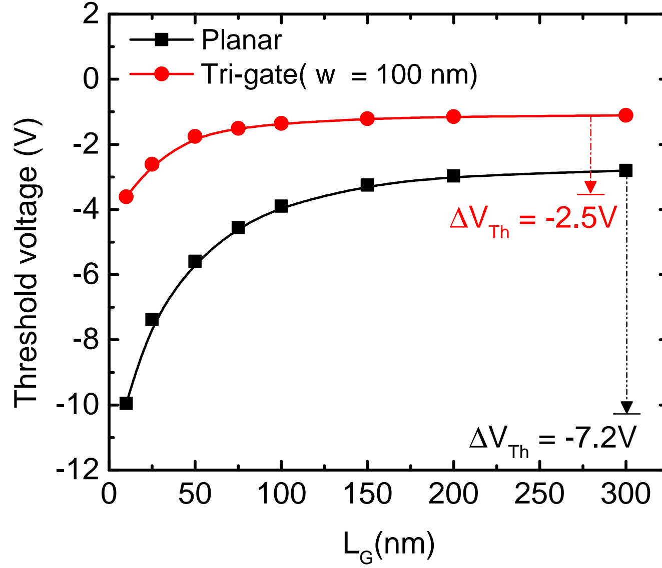

Figure 3.30: A Comparison of the scaling behavior of planar and tri-gate GaN HEMTs in terms of threshold voltage roll-off

150 nm, while this roll-off is considerably less pronounced in the GaN tri-gate HEMT design ($\triangle V_{Th}$ = -2.5V) with a fixed body width of 100 nm. Moreover, the short channel effect is also responsible for increasing the output conductance as shown in Fig. 3.31. Shrinking the gate length for planar device for 300 to 10 nm has resulted in 0.28 S/mm increase in the output conductance. The GaN tri-gate HEMT with a body width of 100 nm on the other hand has shown a smaller value for g_{ds} (0.13 S/mm) while keeping the shift in threshold voltage as small as possible due to the better electrostatic control of the side gates.

3.6 Breakdown Voltage

Next, the breakdown voltage BV of planar and tri-gate GaN HEMTs with L_G = 100 nm are simulated and the specific on resistances $R_{on,sp}$ are extracted. Here, $R_{on,sp}$ is defined as the inverse of the maximum slope of the output characteristics at $V_{GS} = V_{Th}$ +1 normalized on the device active area for fair comparison (see Inset of Fig. 3.32). As can be seen from Fig. 3.32, the GaN tri-gate HEMT exhibits a higher breakdown voltage (BV = 92V) than the planar device (BV = 72V). Within the tr-gate bodies, the 2DEG channel is depleted especially for normally-off devices at the selected operating point (i.e., $V_{GS} = V_{Th}$ +1). Such improvement that tr-gate deign provide even for such small gate-drain distance

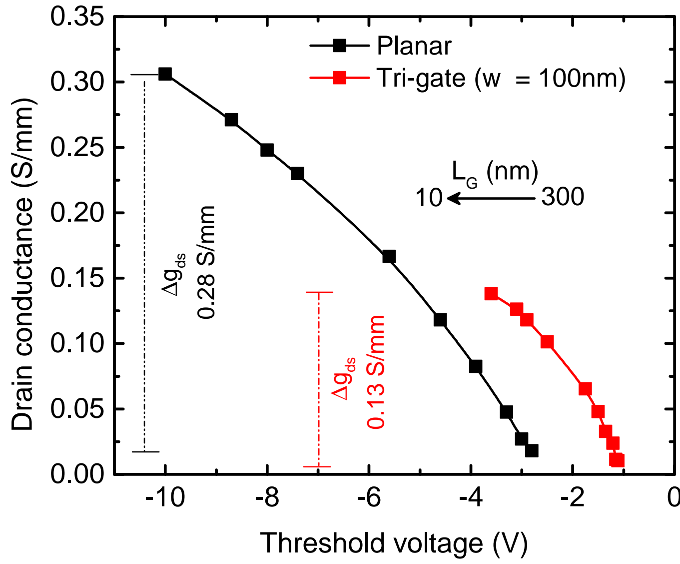

Figure 3.31: Lateral scaling of planar and tri-gate GaN HEMTs and the effect on the drain conductance.

(i.e., in this work 700n m) give it a superior to its planar counterparts.

It is also clear from Fig. 3.32 that planar GaN HEMT suffers from short channel effects and this is clear from the increase in drain current with increasing the drain voltage, while on the other hand, the tr-gate GaN HEMT device maintain the change in drain current as a function of drain voltage as small as possible before breakdown voltage. The increase of breakdown voltage is on the expense of only half the expected increase of $R_{on,sp}$ as proposed by the theoretical limit for GaN devices shown in Fig. 3.33. In other words, the GaN tri-gate HEMT operates closer to the theoretical limit than its planar counterpart.

Further, we investigate the effect of body width w on the BV-$R_{on,sp}$ curve as shown in Fig. 3.33b.The results depict that (1) with reducing body width of GaN tri-gate HEMT structure, an increase in breakdown voltage is realized with less increase in $R_{on,sp}$ (almost 17% lower) compared to GaN limits. (2) for wider body widths, however, GaN tr-gate can observe almost the same BV with the same $R_{on,sp}$ value. This is suggest that GaN tri-gate HEMT structure suggests a different limit line compared to conventional GaN counterparts.

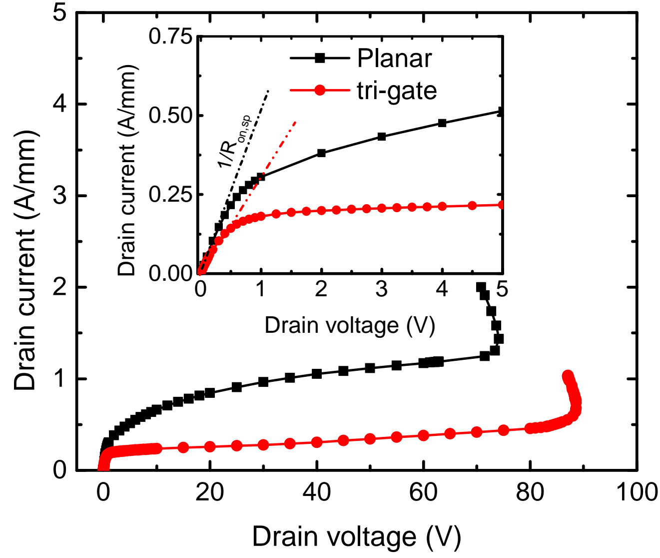

Figure 3.32: Calculated drain current as a function of drain voltage for GaN tri-gate HEMT ($w = h = d = 100$nm) and planar GaN-HEMTs at $V_{GS} = V_{Th} + 1$. Inset: Extracting specific on resistance from calculated output characteristic.

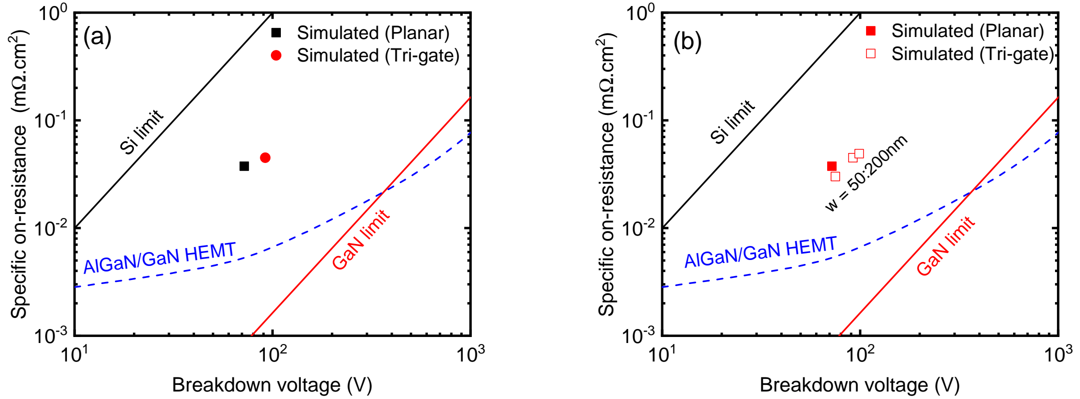

Figure 3.33: (a) specific on resistance vs breakdown voltages for simulated planar and tri-gate GaN HEMTs with $L_G = 100$ nm compared to theoretical limits for Si, GaN devices (b) Breakdown voltages for GaN tri-gate HEMT with varied bod width 50 to 200 nm compared with planar counterpart.

3.7 Summary

AlGaN/GaN tri-gate HEMT structures have been studied using the 2D Schrödinger-Poisson and 3D ATLAS Silvaco simulators. It has turned out that the threshold

voltage strongly depends on the body width and to a lesser extent on the etching depth. We found that GaN tri-gate HEMT structures with body widths around 100 nm are most sensitive to the etch depth. However, the beneficial effect of an increasing side gate area becomes weaker with going deeper in depth and saturates at a depth of about 100 nm. Hence, an etch depth of 150nm should be more than sufficient for most GaN tri-gate HEMT designs.

Moreover, the simulation results have shown that due to its excellent electrostatic integrity, the tri-gate GaN HEMT structure can be scaled down to gate lengths of the order of 10 nm while short-channel effects are effectively suppressed. The GaN tri-gate HEMT threshold voltage is not only controlled by the top gate as in standard planar devices but also by the side gates. Therefore, normally-off behavior can be achieved by reducing the body width below 40 nm for the studied layer sequence.

Additionally we have investigated the electric field distribution in the device. It has turned out that two major hot spots are found at the drain-side edge of the side-gate/GaN contact, one at the AlGaN/GaN interface and another one at the 3D corner of the side gate. The electric field particularly at these points has been found to be critical when compared to the breakdown field in GaN (i.e.,$\approx$4 MV/cm) already at drain voltages below 20V. The GaN tri-gate HEMTs have also show to exhibit higher breakdown voltage on the price of less increase in specific on resistance as suggested by GaN theoretical limits.

Chapter 4

RF performance of GaN Tri-gate HEMTs

In this chapter we perform a systematic theoretical study to get insights in the GaN tri-gate HEMT structure for the RF application, investigate the impact of design variations on the device RF performance and investigate the origin of the degradation in RF performance and propose some design guidelines to reduce the parasitic elements. We use the 3D ATLAS device simulator from Silvaco to conduct the simulations and compare it with the measured data provided by Frauenhofer IAF for validations and calibrations [65].

4.1 Surface Passivation and Gate Geometry

The investigated device has a similar layer sequence as shown in Fig 4.1. The layer sequence consists of a 120 nm AlN nucleation layer, a 2 μm GaN buffer/channel layer, a 22 nm $Al_xGa_{1-x}N$ barrier with Al content $x = 0.22$, and a 3 nm GaN cap. A passivation layer of 100 nm Si_3N_4 is deposited on the cap between the source/drain and gate electrodes, and a Ni/Au gate with length L_G of 100 nm is wrapped around the body from three sides (i.e., on top of the GaN cap and at the sidewalls). The source-gate and gate-drain distance L_{SG}, L_{GD} are 0.7μm.

A T-shaped gate cross-section as in the experimental devices as shown in Fig. 4.1 is considered in the simulations to account for the capacitive coupling between the gate head and source/drain access-region/electrodes [65],[45]. Note that the relative impact of the gate head is stronger in planar devices compared to GaN tri-gate HEMT designs due to the additional contribution of the gate at the sidewalls of the GaN tri-gate HEMT body. The T-gate cross section is used

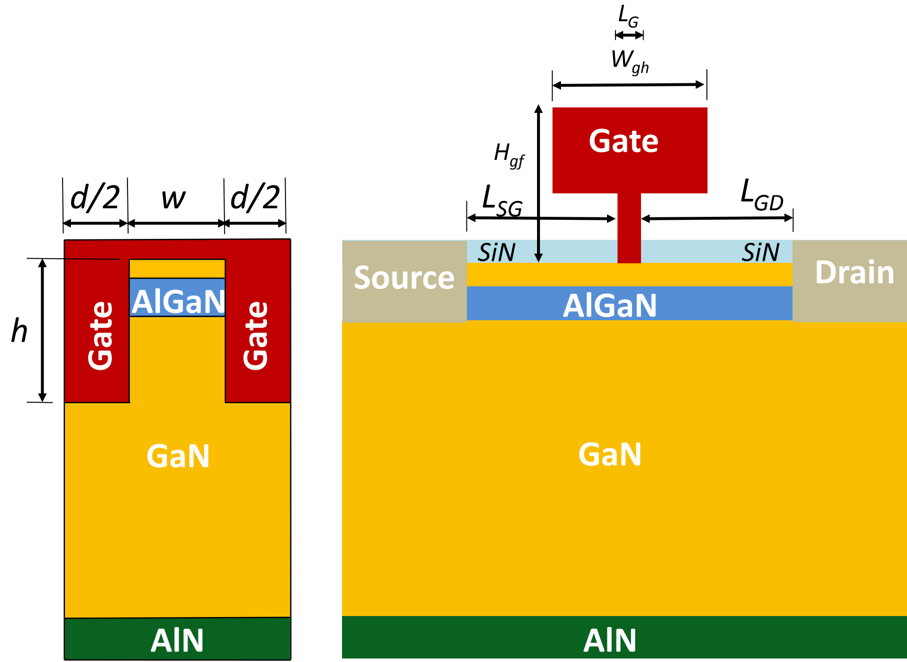

Figure 4.1: A schematic of the investigated GaN tri-gate HEMT structure.

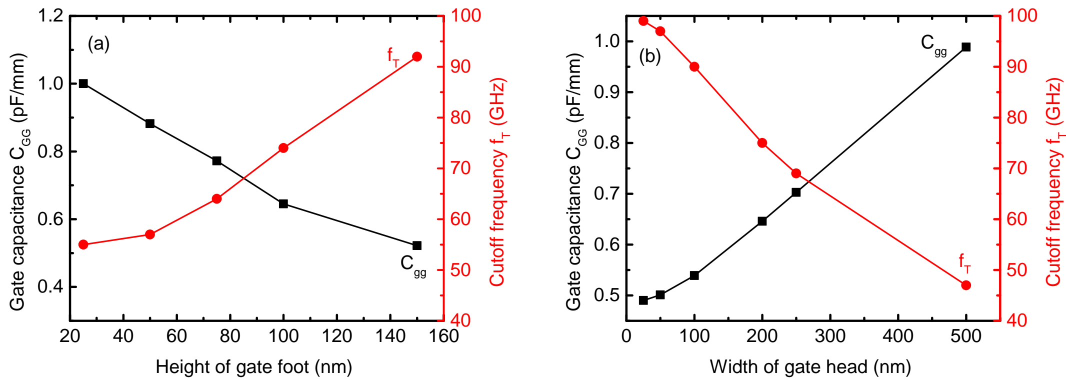

Figure 4.2: Simulated cutoff frequency and gate capacitance of planar GaN HEMT with (L_G=100 nm) as a function of (a) height of gate foot H_{gf} (b) width of gate head W_{gh} calculated at V_{DS} = 5V

to improve the device characteristics by reducing the gate resistance R_G effect when the gate length is shrinked, however, this on the other hand leads to an increase in the gate capacitance C_{gg}. The T-gate geometry has to be optimized so that a smaller value for R_G is ensured even for small gate lengths. Therefore, the width the gate head W_{gh} and and height of gate foot H_{gf} have to be chosen carefully.

Shown in Fig. 4.2 the effect of varying the gate-head width and height of gate-

foot on C_{gg} and f_T. It is clear that the gate capacitance is reduced by increasing the height of the gate-foot because the capacitive coupling between the gate-head, source and drain contacts will be reduced which can be also done by reducing the width of gate-head. This means that a trade-off between R_G and C_{gg} has to be made.

In the investigated structure in Fig. 4.1, we studied also the surface passivation (SiN) affect on the RF performance. Surface passivation influence on planar and nanoribbon AlGaN/GaN HEMTs has been shown to cause degradation in DC performances.Due to the increased tensile stress in the AlGaN layer, overall charge density increases [68]. Moreover, RF performance has been show to be improved by almost 50% when using surface passivation [69]. We varied the gate length L_G of the conventional planar structure from 10 to 300 nm to understand their influence on gate capacitance C_{gg} and cutoff frequency f_T. It turned out that for the planar structure without passivation, by reducing gate length frequency f_T increases as depicted from Fig. 4.3.

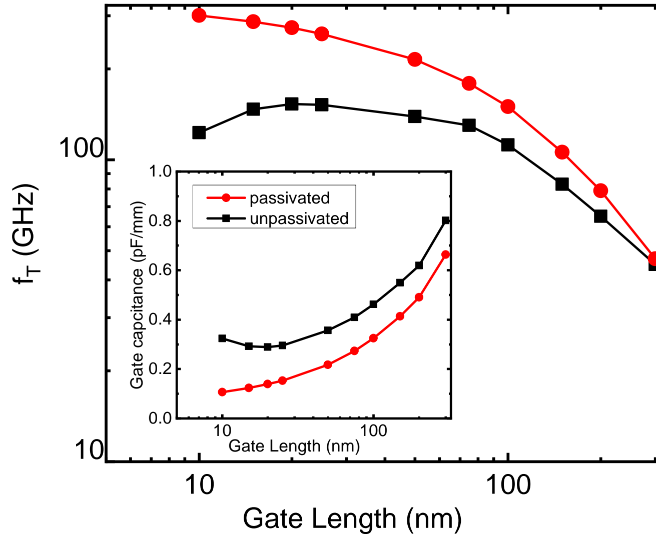

Figure 4.3: Simulated cutoff frequency f_T for passivated and unpassivated planar GaN HEMT vs. gate length calculated at V_{DS} = 5V

However, as gate length is reduced beyond after 100 nm, we see almost a saturation followed by drop down in f_T. The inset in Fig. 4.3, shows that as gate length is reduced, gate capacitance C_{gg} decreases, but at very small gate lengths ($L_G \leq$30 nm), C_{gg} starts to increase again causing f_T to drop down. Nevertheless, with surface passivation, a clear trend as expected for both C_{gg} and f_T are shown.

4.2 RF characteristics

After having established our simulation approach, the RF performance of the planar and GaN tri-gate HEMT($w = d = 100$ nm, $L_{Fin} = 500$ nm and $h = 200$ nm) GaN HEMT structures from Fig. 4.2. To this end, the gate length for both devices remain the same ($L_G = 100$ nm) in the simulations. In this section we calculate RF characteristics of the GaN HEMTs by conducting 3D simulations considering full device structure using ATLAS simulator from Silvaco.

The investigated device has a similar layer sequence as in [65],[37]. The layer sequence consists of a 120 nm AlN nucleation layer, a 2 μm GaN buffer/channel layer, a 22 nm $Al_xGa_{1-x}N$ barrier with Al content $x = 0.22$, and a 3 nm GaN cap. A passivation layer of 100 nm Si_3N_4 is deposited on the cap between the source/drain and gate electrodes, and a Ni/Au gate with length L_G of 100 nm is wrapped around the body from three sides (i.e., on top of the GaN cap and at the sidewalls). The source-gate and gate-drain distance L_{SG}, L_{GD} are 0.7μm.

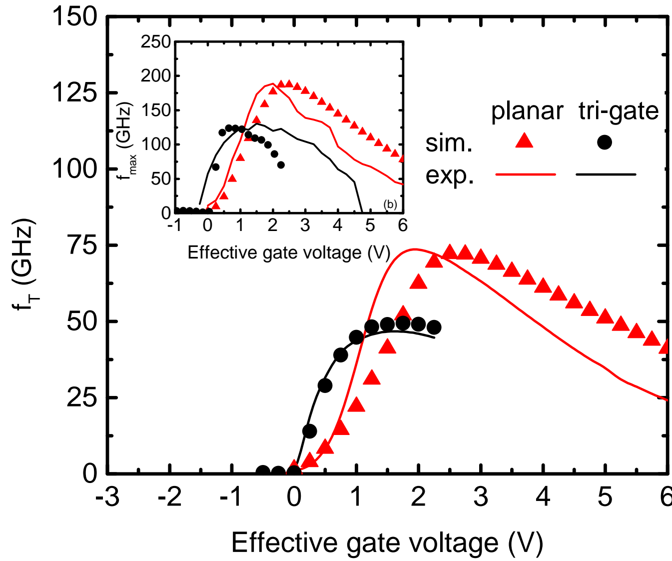

Figure 4.4: Simulated vs. measured (a) cutoff frequency and (b) maximum frequency of oscillation f_T and f_{max} of planar and tri-gate GaN HEMTs as a function the effective gate voltage (V_{GS}- V_{Th}) calculated at V_{DS} = 5V

The simulated and measured cutoff frequencies for both devices are shown in Fig. 4.4 as a function of the effective gate voltage. The comparison reveals that a good agreement between measured and simulated f_T for both planar and tri-gate

GaN HEMTs is achieved. As can be seen, the peak f_T value of the GaN tri-gate HEMT device is about 35 % lower than that of the planar counterpart (planar f_T = 75 GHz, tri-gate f_T = 49 GHz). However, the $f_T - V_{GS,eff}$ curve of the GaN tri-gate HEMT device is considerably more flat than that of the planar HEMT.

Furthermore, the peak f_T of the GaN tri-gate HEMT is more rapidly achieved compared to the planar device. The lower f_T peak of the GaN tri-gate HEMT can be attributed to its considerably larger gate capacitance compared to that of the planar device. From small-signal analysis, an overall gate capacitance C_{gg} of 0.84 pF/mm (normalized on w_{total}) for the GaN tri-gate HEMT structure is found. This value is 33% larger than the C_{gg} of the planar HEMT (0.56 pF/mm).

Contrary, the transconductance of the GaN tri-gate HEMT (g_m = 261 mS/mm) is slightly smaller than that of the planar device (282 mS/mm), which further contributes to the smaller peak f_T of the GaN tri-gate HEMT. Note that for a GaN tri-gate HEMT structure, the stated value of g_m strongly depends on the normalization scheme. In this study, we normalize all quantities on the total width, $w_{total} = w + d$, but normalization on the body width w is also common. In the latter case, the g_m of our GaN tri-gate HEMT structure would be twice as large, i.e. much larger than that of the planar device. However, this would have no effect on f_T as the capacitance value would increase by the same factor.

As an advantage of the GaN tri-gate HEMT structure, we find an extremely small output conductance g_{ds} of 30 mS/mm compared to 70 mS/mm for the planar device, a sign for effectively suppressed short-channel effects. Considering a gate resistance R_G value as in the experimental devices (i.e. 3Ω in 100 μm wide devices), our simulations result in peak f_{max} of 180 and 123 GHz for the planar and GaN tri-gate HEMT devices, respectively, which are in a good agreement with the measured f_{max} (189 GHz for the planar and 130 GHz for the GaN tri-gate HEMT device).

Figure. 4.5 demonstrates a 2D contour of f_T of planar and tri-gate AlGaN/GaN HEMTs as a function of gate and drain voltages. the dependency of f_T on the applied gate and drain bias for both planar and tri-gate GaN HEMTs. The conventional planar design here has shown a maximum peak f_T at V_{GS} = -2.5V but then by either varying drain or gate voltage, the value of f_T drops down. On the other hand, the GaN tri-gate HEMT structure is shown to have weak dependency on the applied drain voltage because the peak f_T achieved (at V_{GS} = 0V) remains almost unchanged. Similar behavior have been also studied and confirmed by other groups [54].

To elaborate more on the dependency of the planar and tri-gate GaN HEMT

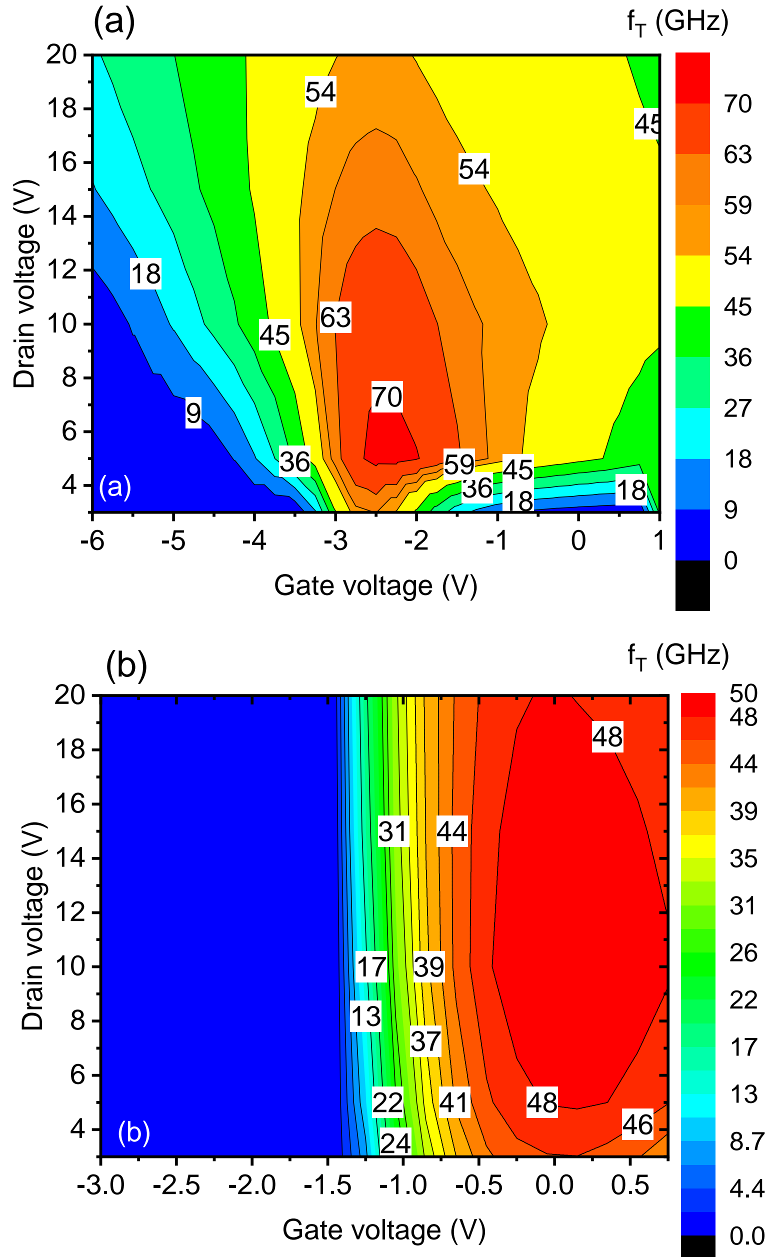

Figure 4.5: 2D contour of the simulated cutoff frequency f_T for planar (a) and tri-gate (b) GaN HEMTs as a function of the gate and drain voltages.

structure on bias, the corresponding transconductance and gate capacitance for the previous result as functions of drain voltage are shown in Fig. 4.6. It is clear that the reason for observed flatness in f_T for the GaN tri-gate HEMT structure is related to the flatness in g_m (i.e., less dependence on the bias). The planar GaN HEMT however has shown a strong dependency for g_m on the bias which might a limitation. It has been found to be the relatively unchanged source access resistance compared to the rapidly increasing one in conventional

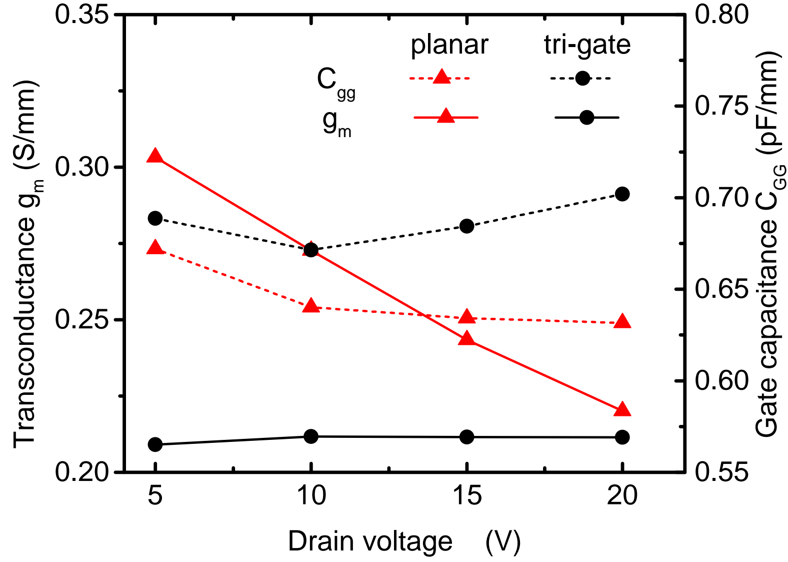

Figure 4.6: Simulated vs. measured Peak values of the cutoff frequency (f_T) simulated for planar and tri-gate GaN HEMTs as a function of the drain voltage V_{DS}. Inset: simulated source access resistance for GaN planar and tri-gate HEMTs as a function of the drain current.

planar structures as shown in Fig. 4.7 is the main reason for the flatness in f_T and g_m. This is due to its larger current drivability of its source access region as it has similarly been observed by other groups for the GaN tri-gate FETs [46],[54],[70],[17]. The source access resistance R_s is extracted from simulation data by ; 1) source contact is grounded and gate is forward biased with respect to the channel. 2) Constant gate currents I_{GS} is applied into the AlGaN/GaN channel, 3) varying drain current from 0 to 2 A/mm to obtain different levels. 4) extract R_s by taking derivative of gate voltage V_{GS} with respect to the drain current I_{DS}.

In the planar device as shown in the inset in Fig. 4.7, as a consequence of increasing the gate bias, the source resistance as a function of current is also increases. This exponential behavior of the source resistance of planar HEMTs causes a drop down in transconductance g_m. The access resistance of planar GaN HEMT is 5 times higher than GaN tri-gate HEMT at drain current = 2 A/mm, while for its GaN tri-gate HEMT counterpart remains almost unchanged. It has been shown in [54] that for conventional planar HEMT structures, the increase in source access resistance limits the effective gate overdrive ($V_{OV,eff}$ so that $V_{OV,eff} = V_{GS} - V_{Th} - I_{DS} \times R_S$) and therefore, channel charge increase will

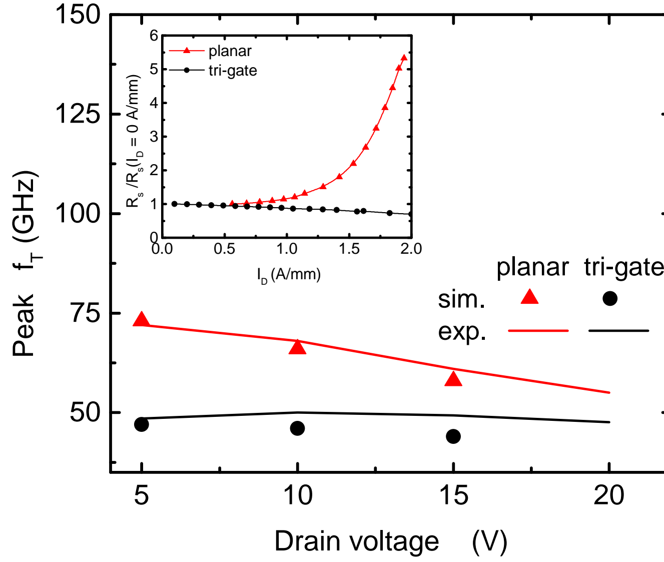

Figure 4.7: Simulated vs. measured Peak values of the cutoff frequency (f_T) simulated for planar and tri-gate GaN HEMTs as a function of the drain voltage V_{DS}. Inset: simulated source access resistance for GaN planar and tri-gate HEMTs as a function of the drain current.

be affected.

4.3 RF Scaling Potential of GaN HEMTs

The RF scaling potential of the conventional planar and GaN tri-gate HEMT structures is investigated by varying the gate length between 10 nm and 300 nm. For the GaN tri-gate HEMT structure, two cases are considered, namely, GaN tri-gate HEMT with fixed width (i.e.,w = 100 nm) and with body width also scales with the gate length (i.e., $w = L_G$). In both cases, the etch depth and gap for GaN tri-gate HEMT is held fixed e.g., $d = h = 100$ nm. A reasonable measured gate resistance is used for fair comparison (i.e., 300 $\Omega\mu$m). We use the same layer sequence as of the previous section for both planar and tri-gate, but we consider un-passivated surface here to isolate parasitics affect on the RF performance.

Figure 4.8 shows both f_T and f_{max} of the conventional planar and the tri-gate GaN HEMT designs. Even at very short gate lengths, the conventional planar device outperforms the GaN tri-gate HEMT in terms of f_T. However, a saturation followed by degradation in conventional planar RF performance is

noticed, while GaN tri-gate HEMT devices with fixed body widths have shown continuous increase in f_T and f_{max} with reducing the gate length. In the second case, where $w = L_G$, similar trend is observed for both f_T and f_{max} for body widths larger than 25 nm. Both f_T and f_{max} drops for GaN tri-gate HEMT devices below 25 nm body width.

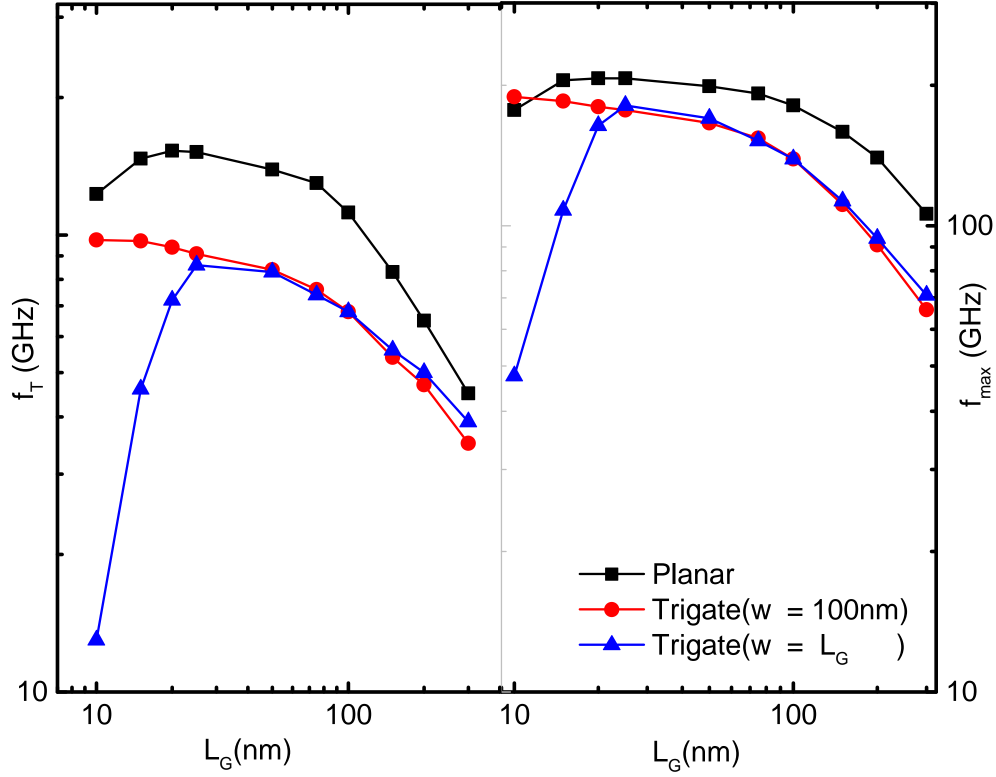

Figure 4.8: Peak values of the (a) cutoff frequency (f_T) and (b) maximum frequency of oscillation (f_{max}) simulated for planar and tri-gate GaN HEMTs at $V_{DS} = 3V$ as a function of the gate length L_G

4.4 Performance Degradation Analysis

To understand the possible reasons responsible for the drop down in the GaN tri-gate HEMT f_T and f_{max}, transconductance g_m, output conductance g_{ds} and overall gate capacitance C_{gg} for the results shown in Fig. 4.8 normalized by the total width are extracted and shown in Fig. 4.9. In Fig. 4.9a, the extrinsic transconductance of the planar device increases for devices with $L_G > 75$ nm and a saturation is noticed at $L_G = 50$ nm possibly because the saturation electron velocity value is already reached. The saturation in g_m is later followed by slight dropdown at

$L_G \leq 20$ nm because some of the parasitic components do not scale with the gate length.

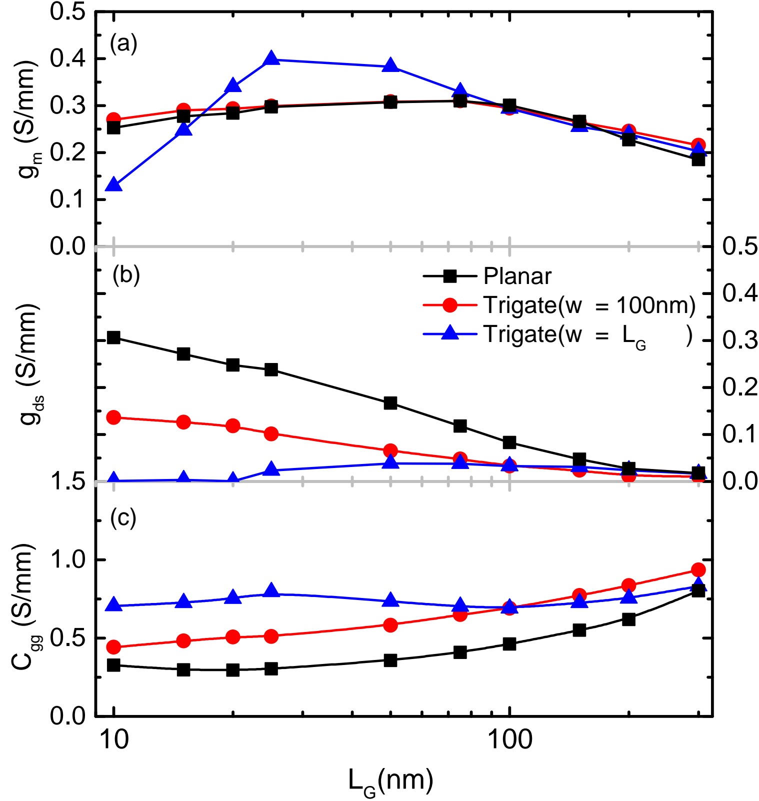

Figure 4.9: Impact of lateral scaling on (a) transconductance (b) output conductance (c) overall gate capacitance of planar and tri-gate GaN HEMTs. All values are normalized on the total gate width w_{total}

.

For the GaN tri-gate HEMT devices, it turns out that scaling the body width (i.e., the case where $w = L_G$) has much stronger effect on g_m and by shrinking the body width the extrinsic transconductance increases. Later, a remarkable degradation in g_m is seen, and the reason is that the value of g_m is at the maximum peak f_T which for $L_G < 25$ nm is limited because of the dominant Schottky-gate leakage current. Moreover, no more improvement can be achieved in g_m compared to the planar device if the body width is fixed $w = 100$ nm. Note that, total gate width normalization (i.e., body width + separation) is used.

In Fig. 4.9b, the GaN tri-gate HEMT devices in both cases have shown smaller g_{ds} compared to the planar device, and the value of g_{ds} becomes even smaller

Table 4.1: Figures of merit of AlGaN/GaN tri-gate HEMTs with a gate length of 25 nm and various body widths, etch depths and separation widths. Also, the parameters for the planar HEMT with the same gate length are shown for comparison.

Device	w nm	h nm	d nm	g_m S/mm	g_{ds} S/mm	C_{gg} pF/mm	f_T GHz	f_{max} Ghz
Tri-gate	100	100	50	0.32	0.085	0.483	106	199
	100	100	100	0.28	0.079	0.494	91	177
	100	100	200	0.23	0.071	0.511	73	150
	100	50	100	0.25	0.090	0.405	100	193
	100	100	100	0.28	0.079	0.494	91	177
	100	200	100	0.29	0.079	0.591	80	156
	50	100	100	0.37	0.057	0.632	95	182
	100	100	100	0.28	0.079	0.494	91	177
	200	100	100	0.24	0.095	0.399	97	184
Optimized tri-gate	50	50	50	0.40	0.068	0.500	127	231
Planar	-	-	-	0.30	0.238	0.302	152	207

when the body width is reduced because of excellent suppression of short channel effects. However, the GaN tri-gate HEMT devices have also shown higher C_{gg} compared to the conventional planar device as it is shown in Fig. 4.9c, which is the main reason for the degradation in the RF GaN tri-gate HEMT performance compared to the planar device. This effect becomes even stronger when the body width is reduced.

In order to understand the origin of the higher parasitic C_{gg} in the GaN tri-gate HEMT devices, the extracted device parameters for a GaN tri-gate HEMT with body width $w = 50$ nm, gate length $L_G = 25$ nm and both the gap d and etch h are varied are shown in Tab. 4.1. The gate length is chosen to be the same where the conventional planar device has shown the maximum RF performance to see if the GaN tri-gate HEMT can achieve similar or even better performance at the same gate length. Either etching depth or gap is varied at once with keeping the other parameters fixed. As it is shown in Tab. 4.1, both etch depth and gap has an impact on the RF performance of the GaN tri-gate HEMT device (i.e., on both f_T and f_{max}). The results show that by decreasing the gap between adjacent GaN tri-gate HEMT bodies from 200 nm to 50 nm both f_T and f_{max} are improved by 45% and 33% respectively.

The realized improvement achieved by reducing the gap d is mainly due to the reduction in the overall gate capacitance C_{gg} and also an increase in the transconductance g_m (i.e., number of channels per total width increases). The

increase in f_{max} is slightly lower than f_T because the output conductance g_{ds} value increases with reducing the gap d. Second, the etch depth h is reduced from 200 nm to 50 nm with fixing the gap d to 100 nm, and this provides 25% and 24% improvement in f_T and f_{max} respectively. Reducing the etch depth helps to reduce the side gate capacitance although this will also leads to slight reduction in g_m and increase in g_{ds}. However, a compromise has always to be reached in order to optimize the device RF performance. In order to achieve such improvement three different ways are proposed.

4.5 Optimization of GaN Tri-gate HEMTs

In general, the RF performance of a transistor can be improved by minimizing the parasitic capacitance components, by reducing the access and contact resistances and by increasing the transconductance. In the following, three approaches to improve the RF behavior of the GaN tri-gate HEMTs are investigated, namely (a) the optimization of geometrical design parameters, (b) the isolation of the body sidewalls with silicon nitride layers and (c) the increase of the polarization charge by using a lattice matched AlInN barrier.

The three investigated designs are shown in Fig. 4.10 and the layer sequence and design are summarized in Tab. 4.2. A fundamental disadvantage of the GaN tri-gate HEMT architecture is the additional capacitive coupling between the gate metal in between the tri-gate bodies and the source/drain regions, which does not exist in planar HEMT structures.

This parasitic capacitance component strongly depends on two parameters of the GaN tri-gate HEMT design, the gap width d and the etch depth h. Table 4.1 shows the simulated figures of merit for a GaN tri-gate HEMT with a gate length of 25 nm and various gap widths d, etch depths h and body widths w. Also shown for comparison are the parameters for the planar HEMT with $L_G = 25$ nm, i.e. the device with the best RF performance so far. As can be seen from Tab. 4.1, both etch depth h and gap d has a considerable impact on the RF performance. By decreasing the gap between adjacent tri-gate bodies from 200 nm to 50 nm, f_T and f_{max} are improved by 45% and 33% respectively. This is mainly due to the reduction of the overall gate capacitance C_{gg} since parasitic capacitance components are reduced. Furthermore, the transconductance g_m increases as the ratio of channel width per total width (w/w_{total}) becomes larger. For the same reason the output conductance g_{ds} increases as well. Thus, the relative increase of f_{max} is slightly smaller than that of f_T.

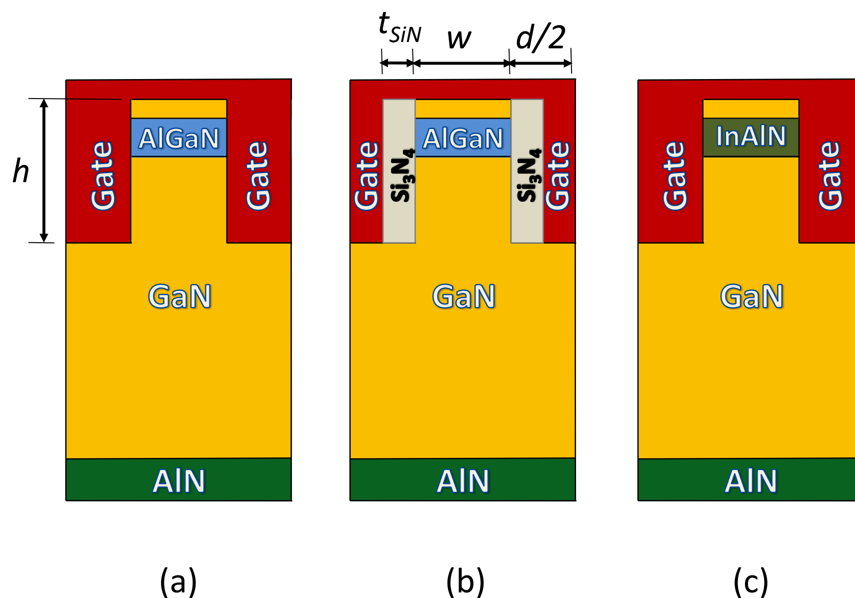

Figure 4.10: Cross section of the investigated GaN tri-gate HEMTs designs (L_G = w = 10 nm) (a) AlGaN/GaN tri-gate as in Fig. 1 (b) AlGaN/-GaN tri-gate with nitride on the sidewalls (c) AlInN/GaN tri-gate HEMTs.

By reducing the etch depth h from 200 nm to 50 nm (while the gap is fixed to d = 100 nm), both f_T and f_{max} can be improved by about 25%. Both g_m and C_{gg} are reduced by decreasing h as the etch depth defines the area of the sidewall gates and hence the intrinsic gate capacitance. However, C_{gg} decreases more rapidly than g_m since the parasitic capacitive coupling between the gate and the source/drain regions is also reduced. The drawback of a reduced etch depth is a larger output conductance g_{ds}, due to the weaker electrostatic control of the channel by the sidewall gates.

As shown in Tab. 4.1 , g_{ds} can be minimized by reducing the body width, whereas both g_m and C_{gg} increase at the same time since the intrinsic gate capacitance becomes larger. Hence, a body width variation only weakly affects f_T and f_{max} as the ratio g_m/C_{gg} remains almost unchanged. However, the minimum f_T (f_{max}) is found at w = 100 nm, i.e., by reducing the width, the RF performance can be slightly improved.

For optimum RF performance, the parameters d, h and w should be reduced simultaneously. As seen from Tab. 4.1, a GaN tri-gate HEMT with $d = h = w$ = 50 nm exhibits a considerably improved RF behavior with f_T = 127 GHz and

Table 4.2: The three proposed approaches to improve the RF behavior of the GaN tri-gate HEMTs are investigated, namely design (a) the optimization of geometrical design parameters, (b) the isolation of the body sidewalls with silicon nitride layers and (c) the increase of the polarization charge by using a lattice matched AlInN barrier

Device	Design A	Design B	Design C
Barrier type	$Al_{0.22}Ga_{0.78}N$	$Al_{0.22}Ga_{0.78}N$	$Al_{0.83}In_{0.17}N$
Barrier thickness (nm)	22	22	22
Body width w (nm)	50	10	10
Body height h (nm)	50	100	100
Body separation d (nm)	50	30	100
SiN on sidewalls (nm)	-	10	-

f_{max} = 231 GHz. Compared to the device with $d = h = w = 100$ nm, f_T and f_{max} are increased by 40% and 30%, respectively. The improved GaN tri-gate HEMT design even outperforms the conventional planar device in terms of f_{max} (f_{max} = 207 GHz for the planar HEMT) mainly due to its much smaller output conductance. However, the GaN tri-gate HEMT f_T is still smaller than that of the planar device (152 GHz) because of the larger gate capacitance of the GaN tri-gate HEMT structure.

Figure 4.11 compares the simulated f_T and f_{max} (maximum frequency of oscillation) of GaN tri-gate HEMT and planar GaN HEMTs with gate lengths between 300 and 10 nm. The best RF performance is obtained at $L_G = 25$ nm for planar devices and at $L_G = 10$ nm for GaN tri-gate HEMT designs with $w = d = h =$ 100 nm (our standard design). As can be seen, our standard GaN tri-gate HEMT design is outperformed by the planar HEMT in terms of f_T and f_{max} in the entire gate length range. However, the RF performance of the GaN tri-gate HEMT can considerably be improved by reducing the dimensions w, h and d of the GaN tri-gate HEMT structure by which the parasitic gate capacitance components are diminished. Such an optimized GaN tri-gate HEMT design can outperform the planar HEMT in terms of f_{max}. The main reason is the very small output

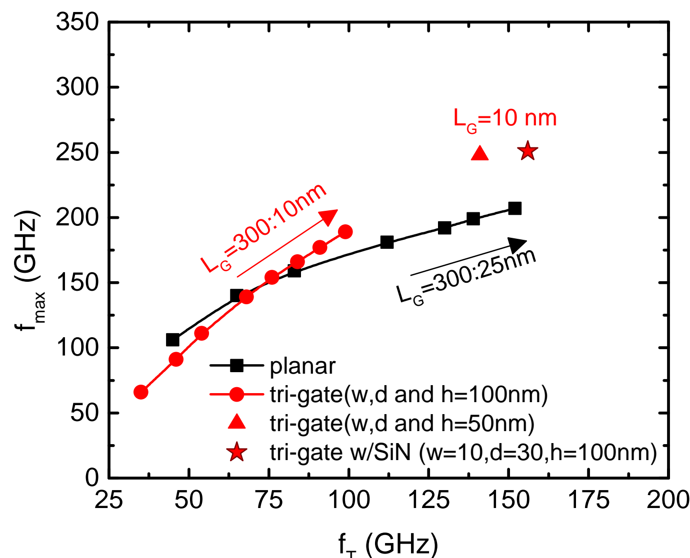

Figure 4.11: f_{max} vs. f_T with various gate lengths for planar HEMTs and different GaN tri-gate HEMT designs; 1) GaN tri-gate HEMT devices with a body width w, body height h and body separation d of 100 nm (red circles). 2) GaN tri-gate HEMT with optimized body width w, body height h and body separation d of 50 nm (red triangle). 3) GaN tri-gate HEMT device with 10 nm SiN layers at the body sidewalls are shown (red star).

conductance of the GaN tri-gate HEMT design due to its excellent electrostatic integrity.

Further improvements can be achieved by covering the body sidewalls with SiN layers 10 nm SiN on each side (i.e., separation $d = 30$ nm which is the red star in Fig. 4.11) and further reducing the body width to increase the transconductance and to minimize parasitic capacitance components. Such a GaN tri-gate HEMT design exhibits higher f_T and f_{max} than the best planar HEMT in this study.

Let us now consider the GaN tri-gate HEMT design with $w = L_G = 10$ nm that has shown the weakest RF performance among all structures investigated so far (compare Fig. 4.8). Figure. 4.12a shows that by reducing the body separation (gap) from $d = 100$ nm to 10 nm, both f_T and f_{max} can strongly be improved. However, this design is still outperformed by the planar HEMT with the same gate length. As illustrated by the dashed line in Fig. 4.12a, the performance of the planar device can be seen as the upper limit for this optimization approach.

However, the etch effect is shown to has a stronger impact on the RF performance. In Fig. 4.12b the effect of varying the etch height h on both f_T and

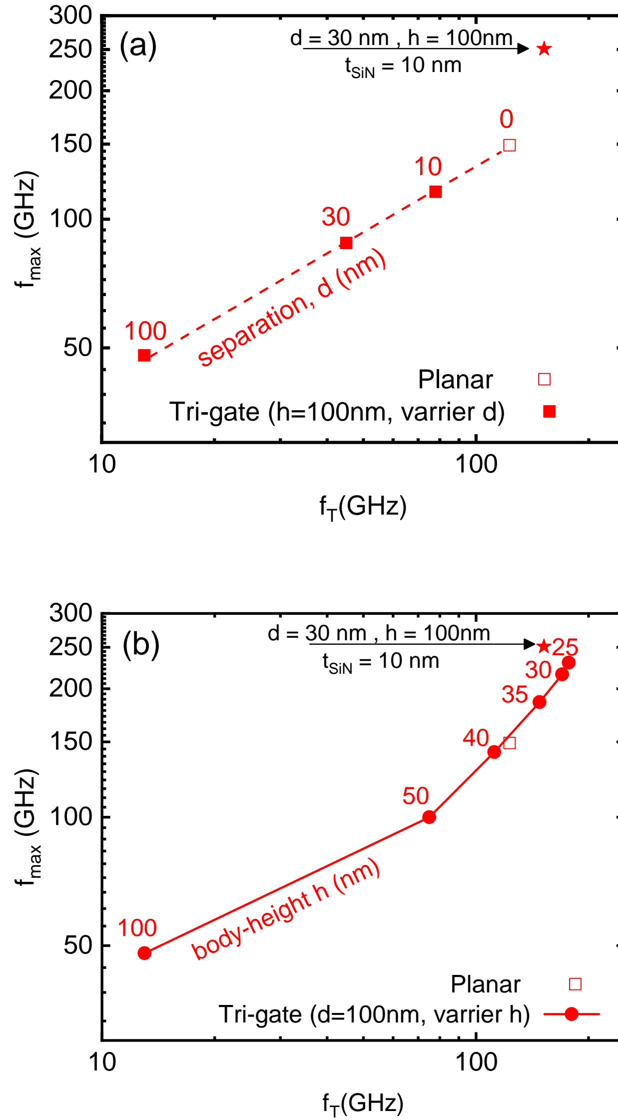

Figure 4.12: Comparison of planar and tri-gate GaN HEMTs with a gate length of 10 nm in terms of f_T and f_{max} calculated at $V_{DS} = 3$V. The GaN tri-gate HEMT devices possess a body width w of 10 nm and (a) a body height (etch depth) h of 100 nm, whereas the body separation (gap width) d is varied (b) a body separation (gap width) d of 100 nm, whereas the body height (etch depth) h is varied. Furthermore, the results for a GaN tri-gate HEMT device with 10 nm SiN layers at the body sidewalls are shown

f_{max} of the investigated GaN tri-gate HEMT is shown. The result show clearly that by reducing the body etch height an improvement in the RF performance can be achieved. Because the tri-gate design suffers from the additional parasitic coupling between the sidewalls and source/drain electrodes, reducing the body

height will leads to a reduction in the overall gate capacitance which results in improvement in RF performance.

Another option to reduce the overall gate capacitance and to improve the RF performance is to cover the sidewalls of the GaN tri-gate HEMT channel with dielectric layers (e.g. SiN). As a result, the fringing capacitance components are reduced since the gap that can be filled with gate metal is narrower than without the nitride. The intrinsic gate capacitance is also reduced as the distance between gate electrode and the body sidewalls is increased. Considering a body separation of d = 30 nm, the overall gate capacitance can be reduced by 25% when the sidewalls are covered with 10 nm SiN. Furthermore, due to the smaller intrinsic gate capacitance, the threshold voltage shifts to a negative value (V_{Th} = -0.5V compared to 0.64V without the nitride) and hence the operating point for peak g_m, i.e. the optimum gate voltage for a high f_T, is reached before the onset of gate leakage. Thus, the transconductance is more than twice as high at peak f_T compared to that in the structure without the nitrite layers. This results in an increase of f_T and f_{max} by a factor of 3 (see Fig. 4.13) and the GaN tri-gate HEMT structure with SiN layers (f_T = 152 GHz, f_{max} = 251 GHz) outperforms the planar HEMT with the same gate length (f_T = 123 GHz, f_{max} = 149 GHz), particularly in terms of fmax. This is mainly due to the much smaller output conductance (g_{ds} = 81 mS/mm compared to 306 mS/mm for the planar HEMT).

A third option to improve the RF performance is to increase the polarization charge at the barrier/channel interface (i.e. increasing the electron density in the 2DEG). This can be done by either increasing the aluminum content of the AlGaN barrier or by using another barrier material. However, if the Al-content exceeds 30%, partial relaxation becomes likely that in turn reduces the polarization and degrades the electron mobility in the 2DEG [50]. A good alternative is the use of lattice matched (i.e. unstrained) $In_{0.17}Al_{0.83}N$ barriers, where relaxation is not an issue. Compared to the $Al_{0.22}Ga_{0.78}N$ barrier used so far, the polarization charge at the $In_{0.17}Al_{0.83}N$/GaN interface is 2.5 times larger.

Due to the larger 2DEG density, the resistance of the source/drain access regions is reduced. Moreover, the threshold voltage is reduced (though still positive: V_{Th} = 0.25V) and hence a larger effective gate voltage V_{GS} - V_{Th} can be applied before the onset of gate leakage. Thus, a larger transconductance (i.e., closer to peak g_m) can be achieved before h_{21} is compromised by the forward gate current. This leads to a rigorous improvement of the RF performance of the GaN tri-gate HEMT (f_T = 266 GHz, f_{max} = 313 GHz) as can be seen from Fig. 4.13. Contrary,

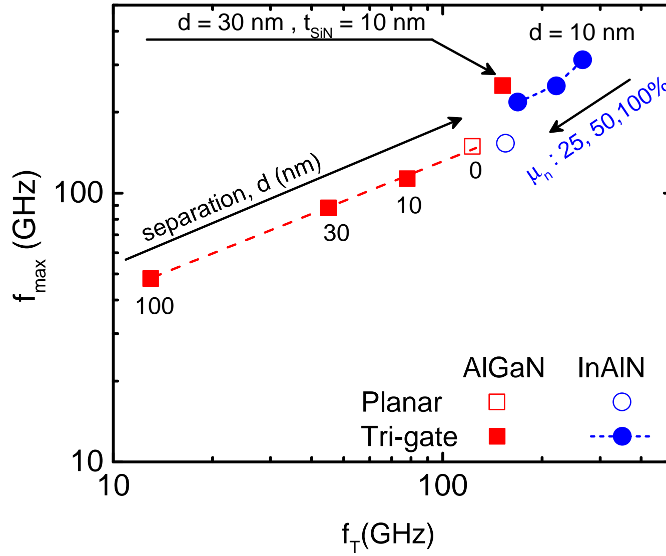

Figure 4.13: Comparison of planar and tri-gate GaN HEMTs with a gate length of 10 nm in terms of f_T and f_{max} calculated at V_{DS} = 3V. The GaN tri-gate HEMT devices possess a body width w of 10 nm and a body height (etch depth) h of 100 nm, whereas the body separation (gap width) d is varied. Furthermore, the results for a GaN tri-gate HEMT device with 10 nm SiN layers at the body sidewalls are shown as well as results for GaN tri-gate HEMT and planar HEMTs with a lattice-matched AlInN barrier.

the RF performance of the planar HEMT only slightly improves when changing the barrier material due to the reduced access resistances. The shift of V_{Th} does not affect the RF performance as the planar device operates at the optimum V_{GS} (peak g_m) for both barrier materials.

An effect that has not been considered so far is the possible degradation of the electron mobility in narrow GaN tri-gate HEMT channels [53],[68]. We have studied the impact of this effect on the RF performance of the $In_{0.17}Al_{0.83}N/GaN$ tri-gate HEMT by reducing the low-field mobility to 50% and 25% of our default value (1020 cm^2/Vs). As can be seen from Fig. 4.13, the effect on the RF performance is less than the mobility value may suggest. A mobility reduction by 50% results in a 17% (20%) decrease in f_T (f_{max}) and for mobility degradation by 75%, f_T (f_{max}) is reduced by only 37% (30%). Moreover, even with only 25% of the mobility in planar heterostructure, the GaN tri-gate HEMT (f_T = 169 GHz and f_{max} = 218 GHz) is faster than the planar device (f_T = 155 GHz and f_{max} = 153 GHz). Figure 4.14a summarizes the three optimized designs in com-

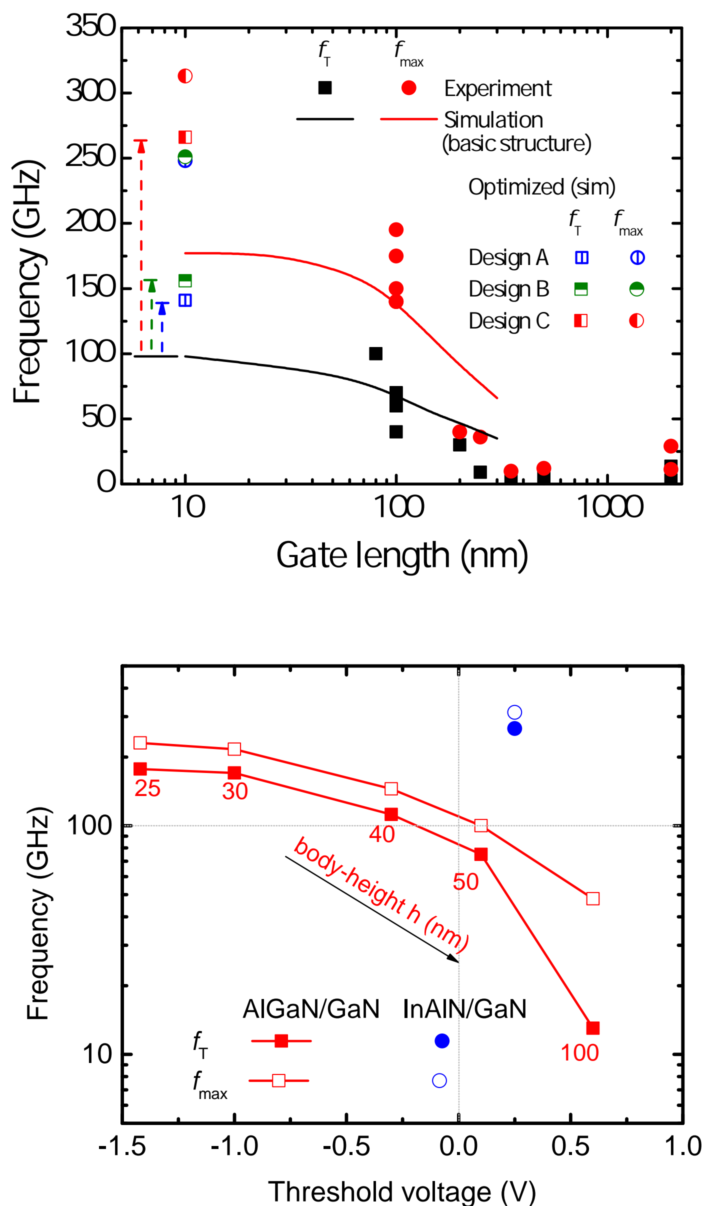

Figure 4.14: (a) state of research and simulated peak values of the cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) for tri-gate GaN FETs as a function of the gate length L_G. (b) Impact of varying the body height h on the cutoff frequency and maximum frequency of oscillation f_T and f_{max} of GaN tri-gate HEMT as a function of threshold voltage.

parison to the state of art of conventional HEMTs. The achieved improvement in the RF performance of the GaN tri-gate HEMTs is sometimes on the price of a negative shift in threshold voltage because it has been found that threshold

voltage is shifted positively if the body width is reduced and/or the body height is increased. This is at the same time leads to an increase in the overall gate capacitance. Figure. 4.14b shows that both f_T and f_{max} are improved by reducing the body etch height, but the price is a negative shift in threshold voltage.

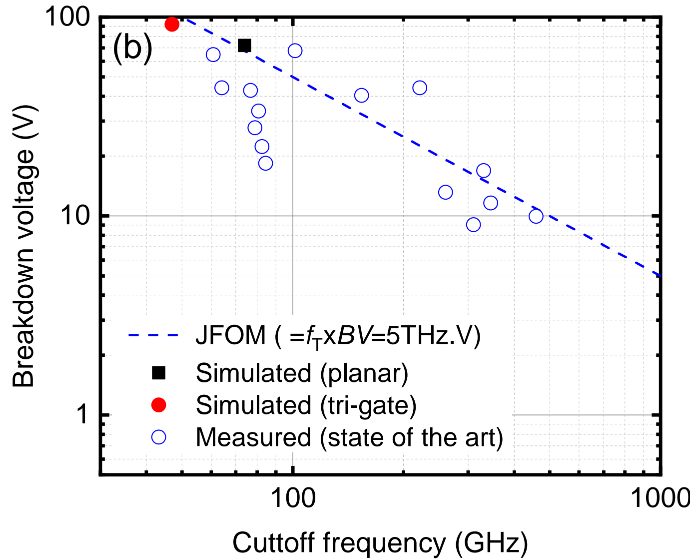

Figure 4.15: Breakdown voltage vs. cutoff frequency of the simulated GaN tri-gate HEMT and planar GaN HEMT devices compared to those of experimental GaN HEMTs. Also shown for comparison is the Johnson figure of merit (JFOM) for GaN devices.

In Fig. 4.15 the breakdown voltage is plotted as a function of the cutoff frequency f_T. As can be seen, both the tri-gate and planar GaN HEMTs closely follow the Johnson limit for GaN devices (dashed blue line). The reason for the smaller f_T of the GaN tri-gate HEMT structure is its large gate capacitance compared to that the planar HEMT [65]. The tri-gate concept suffers from additional parasitic coupling between the gate electrodes in-between the GaN tri-gate HEMT bodies and the source/drain regions which does not exist in the planar GaN HEMT.

4.6 Summary

Our simulations have shown that due to its excellent electrostatic integrity, the GaN tri-gate HEMT structure can be scaled down to gate lengths of the order of 10 nm while short-channel effects are effectively suppressed and normally-

off behavior can be achieved. However, the RF performance of GaN tri-gate HEMT suffers from their large gate capacitance compared to planar devices. This is particularly due to parasitic capacitance components inherent to the tri-gate architecture that are absent in planar HEMTs.

Nevertheless, the GaN tri-gate HEMT design can be improved in order to minimize parasitic capacitance components. According to our simulations, such improved GaN tri-gate HEMT designs can outperform planar HEMTs in terms of f_{max}, while the latter still exhibit the larger peak f_T values. Further improvements can be achieved by adding silicon nitride layers at the body sidewalls and/or by using alternative barrier layers like AlInN that provide a larger polarization charge at the barrier/channel interface. For both cases our simulations result in both higher f_T and f_{max} for the GaN tri-gate HEMT compared to its planar counterpart. Even if a substantially degraded mobility is taken into account, improved GaN tri-gate HEMT designs exhibit a better RF performance than planar devices.

The GaN tri-gate HEMTs have also shown to exhibit higher breakdown voltages than planar devices on the price of less increase of the specific on resistance compared to theoretical limits for conventional HEMTs. However, as most of GaN HEMTs, GaN tri-gate HEMT follow the JFOM, where the is it a trade-off between cutoff frequency and breakdown voltage.

Chapter 5

Conclusion and Outlook

5.1 Conclusion

There is great need for high-performance RF power transistors and power switches. For such applications, GaN-based HEMTs show great potential. Conventional GaN HEMTs are normally-on devices and need a negative gate voltage to be switched off while for many applications normally-off transistors are needed. Moreover, conventional GaN HEMTs suffer from short-channel effects deteriorating the transistors' dc and RF performance. The GaN tri-gate HEMT is considered a promising design option to cope with these problems. Unfortunately, at the beginning of the research described in the present thesis, only little has been known on the operation of GaN tri-gate HEMTs and on their merits and drawbacks.

The present thesis, the GaN tri-gate concept has been studied by means of 2D quantum-mechanical Schroedinger-Poisson simulations and of classical 2D and 3D numerical device simulations. The simulation models have been calibrated by comparing simulated device characteristics with experimental data provided by our project partner Fraunhofer IAF Freiburg. The simulations revealed that the threshold voltage of GaN tri-gate HEMTs strongly depends on the body width and to a lesser extent on the etching depth. It has been found that tri-gate structures with body widths around 100 nm are most sensitive to the etch depth. However, the beneficial effect of an increasing side gate area becomes weaker with increasing etch depth and saturates at a depth of about 100 nm. Hence, an etch depth of 150 nm should be more than sufficient for most tri-gate HEMT designs. Furthermore, it has turned out that the threshold voltage depends strongly on the device width and on the degree of relaxation.

Moreover, impact of the barrier design on transistor performance has been investigated. Here, it has been shown that in narrow bodies the barrier composition (Al content) and thickness have only a limited effect on the threshold voltage. Additionally the electric field distribution in the device has been investigated. It has turned out that two major hot-spots are found at the drain-side edge of the sidewall gate GaN contact, one at the AlGaN/GaN interface and the other one at the 3D corner of the sidewall gate. The electric field particularly at these points has been found to be critical when compared to the breakdown field in GaN (i.e.,4 MV/cm) already at drain voltages below 20V. Tri-gate GaN HEMTs provide an excellent suppression of short- channel effects in both the on-state (i.e., smaller subthreshold swing and drain-induced barrier lowering) and in the on-state (i.e., reduced output conductance).

When already the first report on the RF performance of GaN tri-gate HEMTs [31] revealed that the advantages of the tri-gate concept in terms of better gate controllability and suppression of short channel effects may be overcompensated by the large parasitics of tri-gate structures. In particular, GaN tri-gate HEMTs suffer from an increased gate capacitance which degrades the RF performance compared to the conventional planar counterpart. The simulations carried out in the frame of the present thesis have led to the first analysis of the root cause of the degradation of the RF performance due to the large parasitics such degradation and helped to improve its performance.

However, tri-gate HEMTs with optimized design and/or an alternative barrier that provides stronger polarization (e.g., lattice-matched AlInN) can achieve an improved RF performance. The simulations carried out have led to the first analysis of the root cause of the degradation of the RF performance due to the large parasitics such degradation and helped to improve its performance and to elaborate design guidelines for our project partner (Fraunhofer IAF Freiburg).

The simulations have shown that due to its excellent electrostatic integrity, the tri-gate GaN HEMT structure can be scaled down to gate lengths of the order of 10 nm while short-channel effects are effectively suppressed. The tri-gate threshold voltage is not only controlled by the top gate as in standard planar devices but also by the side gates. Therefore, normally-off behavior can be achieved by reducing the body width below 40 nm for the studied layer sequence. While the tri-gate HEMTs exhibit higher breakdown voltages than planar devices, the RF performance of tri-gate HEMTs suffers from a large gate capacitance. This is particularly due to parasitic components inherent to the tri-gate architecture that are absent in planar HEMTs. Nevertheless, optimized tri-gate designs can

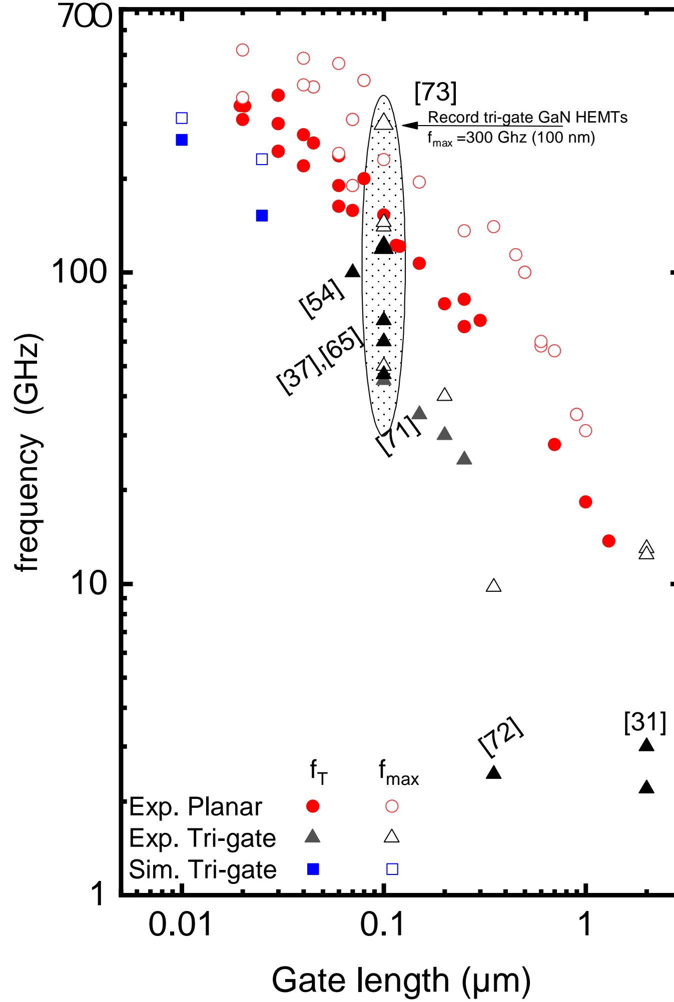

Figure 5.1: The state of research on GaN HEMTs: Transit frequency f_T and maximum frequency of oscillation f_{max} as a function of gate length for both planar and tri-gate GaN HEMTs until mid of 2018 ([31],[54],[37],[65],[71],[72],[73]).

outperform conventional GaN HEMTs in terms of f_T and f_{max}.

5.2 Outlook

This work presented in this thesis has led to a significantly improved understanding of the physics of GaN tri-gate HEMTs. Based on the simulation results, de-

sign guidelines for high-performance GaN tri-gate HEMTs have been elaborated. Moreover, GaN tri-gate HEMTs designed according to the design guidelines and fabricated by our project partner IAF show excellent RF performance. They are the fastest GaN tri-gate HEMTs worldwide in terms of f_{max} (300 GHz for 100-nm gate transistors [71]) and rival the best reported conventional GaN HEMTs with comparable gate length. Given the short history of GaN tri-gate HEMTs, this is a remarkable achievement. Nevertheless, there is still much room for future work. For example, an in-depth study of the large-signal and linearity behavior of GaN tri-gate HEMTs would be of great interest to the community.

List of Figures

1.1 Overview of Si, GaAs, SiC and GaN relevant material properties. 2

1.2 The State of research on the normally-on and normally-off GaN HEMTs. (a)Transit frequency f_T and (b) Maximum oscillation frequency f_{max} as a function of gate length. The experimental data presented are compiled from the current literature. 6

1.3 The State of research on GaN HEMTs: Transit frequency f_T and Maximum oscillation frequency f_{max} as a function of gate length for both planar and tri-gate ([31]) GaN HEMTs until mid of 2013. 7

2.1 A schematic of the investigated planar GaN HEMT structure. . . 14

2.2 Simulated energy band diagrams and electron density underneath the gate region of an AlGaN/GaN heterojunction with 1 μm GaN buffer, 22 nm $Al_{0.22}Ga_{0.78}N$ barrier and a 2 nm cap thickness. . . . 15

2.3 Spontaneous and piezoelectric polarization bound interface charges and 2DEGs in pseudomorphic $GaN/Al_xGa_{1-x}N/GaN$ heterostructure with Ga-face (left) and N-face (right). 16

2.4 Spontaneous polarization of the $Al_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ alloys with wurzite crystals calculated from Eq. 2.1 and Eq. 2.2 17

2.5 Piezoelectric polarization of the $Al_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ alloys with wurzite crystals calculated from Eq. 2.9 and 2.10 18

2.6 A 3D schematic illustration of the investigated GaN tri-gate HEMTs structure. 20

2.7 2D contour plot of the electron distribution of two GaN HEMT device having the same total gate-width calculated at zero applied gate voltage for (a) Planar (b) tri-gate GaN HEMT structures with 100 nm body width. 21

2.8 A comparison between classically (2D Poisson) calculated electron sheet density for planar and tri-gate GaN HEMTs using Nextnano^3 and TCAD Silvaco. Both structures have the same layer sequence: 1 μm GaN buffer, a 14 nm $Al_{0.3}Ga_{0.7}N$ barrier and 2 nm GaN cap. For GaN tri-gate HEMTs, the gate width w is 50 nm and h is 30 nm and depth d is 30 nm. The planar device has a gate width of 1 μm. 26

2.9 Bound interface density of GaN,AlN and InN crystals as a function of the alloys composition x where the dependence of biaxial strain is assumed in the basal plane [48]. Inset: show the tensile and comprehensive strains of the $Al_xIn_{1-x}N$ barrier as a function of the alloy composition. The $Al_xIn_{1-x}N$ barrier is lattice matched at $x = 0.82$ (strain is zero). 28

2.10 Simulated energy Band diagrams and electron densities underneath the gate region of AlGaN/GaN HEMT structure with 22 nm barrier and a 2 nm cap thickness (a) planar (b) in a vertical cut-plane through the channel of GaN tri-gate HEMT structure close to the side−gate Schottky contact. 29

2.11 Electron velocity vs electric field in AlGaN/GaN where the carrier mobility is extracted using the FMCT model in comparison to measured data[62]. 31

2.12 A comparison between simulated vs. measured (device is fabricated by IAF) transfer characteristics for planar GaN HEMT (V_{DS} =3V). 35

2.13 Simulated vs. measured (device is fabricated by IAF) transfer characteristics and gate leakage current (V_{DS} =3V). 36

2.14 Typical (a) transfer (b) output characteristics for GaN HEMT structure. 37

2.15 Conduction band energy in a (a) long channel (b) short channel n-type FETs. 39

2.16 Small signal equivalent circuit diagram for FET with parasitic elements.. 40

3.1 Schematic view of the investigated AlGaN/GaN tri-gate HEMTs structure 44

3.2 Average 2DEG sheet density vs. gate voltage for the GaN tri-gate HEMT structure from Fig. 3.1 (fully strained $Al_{0.3}Ga_{0.7}N$ barrier) for different body widths obtained by classical (CL) and quantum-mechanical (QM) simulation. 45

3.3 The effect of body width reduction on electron distribution in the 2DEG of the structure from Fig 3.1 for zero applied gate voltage assuming zero relaxation. Shown are the electron concentrations in the depth y where for each structure the maximum electron concentration occurs, i.e., the position of the peak in Fig. 3.4, upper right. 46

3.4 Electron distribution in the body of a 100 nm wide GaN tri-gate HEMT structure (compare Fig. 3.1). Upper left: 2D view. Upper right: 1D side view. Lower left: 1D front view. Lower right: 2D top view. In all plots, the AlGaN/GaN channel interface is located at $y = 0$ between $x = 0$ and $x = 100$ nm. The top gate contact is located at $y = 16$ nm. 47

3.5 A comparison between simulated vs. measured transfer characteristics and gate leakage currents for planar and tri-gate GaN HEMTs (V_{DS}=3V). Inset: transfer characteristics comparison on linear scale. 48

3.6 Simulated vs. measured output characteristics of the GaN (a) planar (b) tri-gate GaN HEMT. 49

3.7 Simulated vs. measured (a) transfer characteristics (at V_{DS} = 3V) of planar and tri-gate GaN HEMTs with body widths of 100 and 500 nm. (b) corresponding transconductance as function of gate voltage. I_D and g_m are normalized on the total device width. For the simulated GaN tri-gate HEMT structures $w_{total} = w + d$ (compare Fig. 3.1). 50

3.8 Threshold voltage of the structure from Fig. 3.1 as a function of body width assuming the extreme cases of unrelaxed (strained) and fully relaxed AlGaN barrier obtained by classical and quantum mechanical simulations. Two possible cases are considered for fully relaxed AlGaN layers: relaxed GaN cap (blue triangles) and strained cap (black squares). 52

3.9 Threshold voltage of AlGaN/GaN tri-gate HEMT structures versus body width for (a) two different Al contents (25% and 30%) in the barrier and (b) two different AlGaN barrier thicknesses (10 and 14 nm). 53

3.10 Barrier thickness scaling effect on threshold voltage of $Al_{0.3}G_{0.7}aN$/GaN planar and tri-gate structures. 54

3.11 Comparison between simulated and measured threshold voltage of AlGaN/GaN tri-gate HEMT structures versus body width for two different Al contents (20% and 22%) in the barrier and two different AlGaN barrier thicknesses (20 and 22 nm). 55

3.12 Threshold voltage of GaN tri-gate HEMT vs. body width for different etching depths. Inset: V_{Th}-shift due to an etch depth increase vs. body width. 56

3.13 Transfer characteristics of GaN tri-gate HEMT with 100 nm wide body and different body heights. Inset: threshold voltage vs. etching depth. 57

3.14 Threshold voltage of 100 nm wide GaN tri-gate HEMT with different gate lengths as function of the etching depth. Inset: maximum V_{Th}-shift due to an etch depth increase vs. gate length. 57

3.15 Threshold voltage of 100 nm wide GaN tri-gate HEMT as function of the separation gap g. 58

3.16 (a) Schematic view of the idle rectangular AlGaN/GaN tri-gate structure (b) schematic view of the trapezoidal shape AlGaN/-GaN tri-gate structure (c) sketch of experimental non-idle (with trapezoidal shapes) tri-gate structures [65],[31],[68] 59

3.17 Simulated rectangular and trapezoidal shapes GaN tri-gate HEMT (a) electron line densities with varied body widths as a function of gate voltage.Inset: The corresponding electron concentrations for the simulated GaN tri-gate HEMT structures at V_G=0. (b) threshold voltage as a function of width of normalization. 60

3.18 Simulated rectangular and trapezoidal shapes GaN tri-gate HEMT (a) electron line densities with varied body widths as a function of gate voltage.Inset: The corresponding electron concentrations for the simulated GaN tri-gate HEMT structures at V_G=0. (b) threshold voltage as a function of width of normalization. 61

3.19 Simulated threshold voltage vs. body width assuming a relative dielectric constant of 12.2 for both GaN and AlGaN, together with experimental V_{Th} data from [31]. Two scenarios of top gate and sidewall gate Schottky barriers are considered in the simulations. . 62

3.20 Degree of relaxation required to achieve perfect agreement between the calculated V_{Th} and the experimental data from [31]. Two different cases are considered in the simulations. 63

3.21 2D contour plot of the field distribution in a vertical cut-plane through the channel of the tri-gate GaN HEMT structure close to the side−gate Schottky-contact calculated V_{DS}=3V. 64

3.22 2D contour plot of the field distribution in a vertical cut-plane through the channel of the tri-gate GaN HEMT structure close to the side-gate Schottky-contact calculated V_{DS}=100V. 65

3.23 A schematic of the investigated GaN tri-gate HEMT structure. . . 66

3.24 The field's components at a horizontal cut-line from source to drain at the AlGaN/GaN interface for the 2D contour plot. 66

3.25 The field's components at a vertical cut-line from top to bottom along the side gate edge near the drain−side for the 2D Contour plot. 67

3.26 Schematic view of the investigated critical points. 68

3.27 The total electric field at the investigated points the on/off states. 68

3.28 Simulated components of the electric field in the GaN tri-gate HEMT in the on-state at (a) point 1, (b) point (2), and (c) point 3. 69

3.29 A Comparison of the scaling behavior of planar and GaN tri-gate HEMT in terms of (a) subthreshold swing and (b) drain-induced barrier lowering. 70

3.30 A Comparison of the scaling behavior of planar and tri-gate GaN HEMTs in terms of threshold voltage roll-off 71

3.31 Lateral scaling of planar and tri-gate GaN HEMTs and the effect on the drain conductance. 72

3.32 Calculated drain current as a function of drain voltage for GaN tri-gate HEMT ($w = h = d = 100$nm) and planar GaN-HEMTs at $V_{GS} = V_{Th} + 1$. Inset: Extracting specific on resistance from calculated output characteristic. 73

3.33 (a) specific on resistance vs breakdown voltages for simulated planar and tri-gate GaN HEMTs with L_G = 100 nm compared to theoretical limits for Si, GaN devices (b) Breakdown voltages for GaN tri-gate HEMT with varied bod width 50 to 200 nm compared with planar counterpart. 73

4.1 A schematic of the investigated GaN tri-gate HEMT structure. . . 76

4.2 Simulated cutoff frequency and gate capacitance of planar GaN HEMT with (L_G=100 nm) as a function of (a) height of gate foot H_{gf} (b) width of gate head W_{gh} calculated at V_{DS} = 5V 76

4.3 Simulated cutoff frequency f_T for passivated and unpassivated planar GaN HEMT vs. gate length calculated at V_{DS} = 5V 77

4.4 Simulated vs. measured (a) cutoff frequency and (b) maximum frequency of oscillation f_T and f_{max} of planar and tri-gate GaN HEMTs as a function the effective gate voltage (V_{GS}- V_{Th}) calculated at V_{DS} = 5V 78

4.5 2D contour of the simulated cutoff frequency f_T for planar (a) and tri-gate (b) GaN HEMTs as a function of the gate and drain voltages. 80

4.6 Simulated vs. measured Peak values of the cutoff frequency (f_T) simulated for planar and tri-gate GaN HEMTs as a function of the drain voltage V_{DS}. Inset: simulated source access resistance for GaN planar and tri-gate HEMTs as a function of the drain current. 81

4.7 Simulated vs. measured Peak values of the cutoff frequency (f_T) simulated for planar and tri-gate GaN HEMTs as a function of the drain voltage V_{DS}. Inset: simulated source access resistance for GaN planar and tri-gate HEMTs as a function of the drain current. 82

4.8 Peak values of the (a) cutoff frequency (f_T) and (b) maximum frequency of oscillation (f_{max}) simulated for planar and tri-gate GaN HEMTs at $V_{DS} = 3V$ as a function of the gate length L_G . 83

4.9 Impact of lateral scaling on (a) transconductance (b) output conductance (c) overall gate capacitance of planar and tri-gate GaN HEMTs. All values are normalized on the total gate width w_{total} 84

4.10 Cross section of the investigated GaN tri-gate HEMTs designs (L_G = w = 10 nm) (a) AlGaN/GaN tri-gate as in Fig. 1 (b) AlGaN/-GaN tri-gate with nitride on the sidewalls (c) AlInN/GaN tri-gate HEMTs. 87

4.11 f_{max} vs. f_T with various gate lengths for planar HEMTs and different GaN tri-gate HEMT designs; 1) GaN tri-gate HEMT devices with a body width w, body height h and body separation d of 100 nm (red circles). 2) GaN tri-gate HEMT with optimized body width w, body height h and body separation d of 50 nm (red triangle). 3) GaN tri-gate HEMT device with 10 nm SiN layers at the body sidewalls are shown (red star). 89

4.12 Comparison of planar and tri-gate GaN HEMTs with a gate length of 10 nm in terms of f_T and f_{max} calculated at $V_{DS} = 3$V. The GaN tri-gate HEMT devices possess a body width w of 10 nm and (a) a body height (etch depth) h of 100 nm, whereas the body separation (gap width) d is varied (b) a body separation (gap width) d of 100 nm, whereas the body height (etch depth) h is varied. Furthermore, the results for a GaN tri-gate HEMT device with 10 nm SiN layers at the body sidewalls are shown 90

4.13 Comparison of planar and tri-gate GaN HEMTs with a gate length of 10 nm in terms of f_T and f_{max} calculated at $V_{DS} = 3$V. The GaN tri-gate HEMT devices possess a body width w of 10 nm and a body height (etch depth) h of 100 nm, whereas the body separation (gap width) d is varied. Furthermore, the results for a GaN tri-gate HEMT device with 10 nm SiN layers at the body sidewalls are shown as well as results for GaN tri-gate HEMT and planar HEMTs with a lattice-matched AlInN barrier. 92

4.14 (a) state of research and simulated peak values of the cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) for tri-gate GaN FETs as a function of the gate length L_G. (b) Impact of varying the body height h on the cutoff frequency and maximum frequency of oscillation f_T and f_{max} of GaN tri-gate HEMT as a function of threshold voltage. 93

4.15 Breakdown voltage vs. cutoff frequency of the simulated GaN tri-gate HEMT and planar GaN HEMT devices compared to those of experimental GaN HEMTs. Also shown for comparison is the Johnson figure of merit (JFOM) for GaN devices. 94

5.1 The state of research on GaN HEMTs: Transit frequency f_T and maximum frequency of oscillation f_{max} as a function of gate length for both planar and tri-gate GaN HEMTs until mid of 2018 ([31],[54],[37],[65],[71],[72],[73]). 99

List of Tables

1.1 Properties of GaN in comparison of other competing materials. . . 3

1.2 Comparison between the ratio (g_m/gds), transconductance (g_m), drain conductance (gds), cutoff frequency(f_T) and the maximum frequency of oscillation (f_{max}) of experimental HEMTs: normally-on and normally-off GaN HEMTs. 5

2.1 Metal contacts and their workfunctions 32

2.2 Material parameters used for the simulation (effective masses in growth direction and perpendicular to the growth direction, relative dielectric constant, nonparabolicity of the Γ valley, band gap, conduction band offset, polarization bound charge). 34

4.1 Figures of merit of AlGaN/GaN tri-gate HEMTs with a gate length of 25 nm and various body widths, etch depths and separation widths. Also, the parameters for the planar HEMT with the same gate length are shown for comparison. 85

4.2 The three proposed approaches to improve the RF behavior of the GaN tri-gate HEMTs are investigated, namely design (a) the optimization of geometrical design parameters, (b) the isolation of the body sidewalls with silicon nitride layers and (c) the increase of the polarization charge by using a lattice matched AlInN barrier 88

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List of Symbols

Symbol	Description
V_{Th}	Threshold Voltage
I_{DS}	Drain current
V_{DS}	Drain-source Voltage
V_{GS}	Gate-source Voltage
I_G	Gate leakage current
g_m	Transconductance
$g_{m,int}$	Intrinsic transconductance
$g_{m,int}$	Extrinsic transconductance
f	Electron distribution
q	Elementary charge
ρ	Local space charge density
n	Electrons concentration
p	Holes concentration
$\hbar$	Reduced Planck constant
∇_k	Velocity gradient operator
J_n	Electron current densities
J_p	Holes current densities
${N_D}^+$	Ionized donor impurity concentration
${N_A}^-$	Ionized acceptor impurity concentration
${N_{tD}}^+$	Ionized donor-like traps
${N_{tA}}^-$	Ionized acceptor-like traps
σ	Total polarization induced charge
$q\phi_b$	Schottky barrier of the gate on top of the barrier
E_F	Position of the Fermi level with respect to the edge of GaN conduction band energy
ΔE_c	Offset of conduction band energy at the barrier/GaN interface
T	Lattice temperature
m^*	Effective electron mass
N_V	Effective density of states in valence band
T_L	Ambient temperature
ϕ_B	Barrier height at the metal-semiconductor interface
Q_T	Charge caused by defects and traps
ε	Local permittivity

Symbol	Description
ψ	Electrostatic potential
ρ	Local space charge density
E	Electric field
v_{sat}	Saturation velocity
χ	Thermal conductivity
g_{ds}	output conductance
f_T	Transit frequency
f_{max}	Maximum frequency of oscillation
R_D	Drain Resistance
R_S	Source Resistance
R_G	Gate Resistance
C_{ds}	Intrinsic drain-source capacitance
C_{gs}	Intrinsic gate-source capacitance
C_{gd}	Intrinsic gate-drain capacitance
E_C	Conduction band energy
E_g	Band gap energy
E_F	Fermi level
E_V	Valence band energy
ϵ_0	Vacuum permittivity
ϵ_r	Relative permittivity
L_G	Gate length
w_{total}	Total body width
w_{eff}	Effective gate width
w	Tri-gate body width
d	Tri-gate body depth
g	Tri-gate adjacent spacing between two bodies
V_{Th-QM}	Quantumally calculated threshold voltage
V_{Th-CL}	Classically calculated threshold voltage
L_{Fin}	Fin length
L_{GS}	Gate-source distance
L_{GD}	Gate-drain distance
n_s	Sheet carrier density
μ_n	Electron mobiltiy
μ_p	Holesn mobiltiy
$R_{on,sp}$	specific On-resistance
P^{sp}	Spontaneous polarization charge
P^{pz}	Piezoelectric polarization charge
ϵ_1	Strain

List of Abbreviations

Abbreviation	Description
2DEG	Two-Dimensional-Electron-Gas
CAD	Computer Aided Design
DC	Direct Current
FET	Field Effect Transistor
HEMT	High Electron Mobility Transistor
AlN	Aluminum Nitride
AlGaN	Aluminum Gallium Nitride
RF	Radio Frequency
FET	Field Effect Transistor
Si	Silicon
GaAs	Gallium Arsenide
SiC	Silicon Carbide
GaN	Gallium Nitride
SiN	Silicon Nitride
SS	Subthreshold Swing
DIBL	Drain Induced Barrier Lowering
SCE	Short Channel Effects
BV	Breakdown Voltage
JFOM	Johnson's Figure of Merits

Theses of the dissertation

1. GaN-based high electron mobility transistors are promising devices for radio frequency and high-power electronics and are already in use for power switches and RF power amplifiers (PA).

2. Commonly, these devices are normally-on transistors, i.e., they are in the on-state at zero applied gate voltage which limits their usage for various important designs such as fail-safe and RF amplifiers with single-polarity power supply.

3. Achieving a positive threshold voltage in GaN structures is unfortunately difficult compared to GaAs- and InP-based HEMTs due to the high density of the polarization-induced 2DEG (two-dimensional electron gas) at the barrier/buffer interface.

4. In a radio frequency (RF) circuits, short gate lengths and fast carriers in the channels are required. However, many results for devices with aggressively scaled gate lengths have shown an evidence of short-channel effects because of the decreased control of gate over the channel.

5. The tri-gate design is recently employed to suppress the short channel effects due to the better gate controllability. They have shown excellent down-scaling characteristics and high performance when compared to the conventional top-gate transistors.

6. Tri-gate design ensure a significant shift of threshold voltage toward positive and suppress short channel effects values compared to conventional top-gate control transistors.

7. The tri-gate GaN HEMTs are suffering from increased parasitics causing worse RF performance (cut-off frequency in particular) than planar counterpart. Enhancing the RF performance of these devices by reducing parasitics is essential.

8. A theoretical description and simulation of GaN HEMTs tri-gate electrical behavior of is conducted within this work, which helps to understand the physics of these transistors, assess their potential and develop advantageous designs.

9. RF performance of tri-gate HEMTs with optimized body design can be superior to that of conventional planar devices either by reducing the body etch height and gap, covering the sidewalls of tri-gate channel with dielectric layers to reduce the fringing capacitance components or increasing the polarization charge at the barrier/channel interface by higher aluminum content of the AlGaN or by using another barrier material (lattice matched $Al_{0.83}In_{0.17}N$).

Mohamed Alsharef

List of Publications

Journals

1. **M. Alsharef**, R. Granzner and F. Schwierz, ”Theoretical investigations of tri-gate AIGaN/GaN HEMTs,” IEEE TED, 1335-1341(2013).

2. **M. Alsharef** , M. Christiansen , R. Granzner, E. Ture, R .Quay, O. Ambacher, F. Schwierz, ”RF Performance of Tri-Gate GaN HEMTs,” IEEE Trans. Electron Devices(2016).

3. E. Ture, P. Brueckner, B .J. Godejohann, R. Aidam, **M. Alsharef**, R. Granzner, F. Schwierz, R. Quay, O .Ambacher, ”High-current submicron tri-gate GaN high-electron mobility transistors with binary and quaternary barriers,” IEEE, J. EDS., 4, I-4 (2016).

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2. **M. Alsharef**, R. Granzner, E. Ture, R. Quay, I. Racko, J. Breza, and F. Schwierz,” Design of GaN tri-gate HEMTs,” Proc. of ASDAM, 104-108(2014).

3. E.Ture, P. Brueckner, F.V. Raay, **M. Alsharef**, R .Granzner, F. Schwierz, R. Quay, O. Ambacher, ”Performance and Parasitic analysis of submicron-scaled-Tri- gate AIGaN/GaN HEMTs,” Proc. EuMC, 97-100(2015).

4. E. Ture, P. Brueckner, R. Quay, O. Ambacher, **M. Alsharef**, R. Granzner, F. Schwierz, ”Enhancement-mode AIGaN/GaN FinFETs with high on/off performance 100nm gate length,” Proc. of EuMC, 61-64(2016).

5. **M. Alsharef** , R. Granzner, E. Ture, R .Quay, O. Ambacher, F. Schwierz, ”Performance of Tri-Gate AlGaN/GaN HEMTs,” ESSDERC(2016).

6. E. Ture, P. Brueckner, R. Quay, O. Ambacher, **M. Alsharef**, R. Granzner, F. Schwierz, ”First demonstration of W-band Tri-gate GaN-HEMT power amplifier MMIC with 30dBm output power,” Proc. of IEEE MTT-S (IMS),35-37(2017).

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