Kamal Katkhouda

Aluminum-based PVD rear-side metallization for front-junction nPERT silicon solar cells

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1. Gutachter:	Univ.-Prof. Dr. rer. nat. habil. Peter Schaaf Technische Universität Ilmenau
2. Gutachter:	Univ.-Prof. Dr.-Ing. habil. Edda Rädlein Technische Universität Ilmenau
3. Gutachter:	Dr. rer. nat. Andreas Grohe DirectPhotonics Industries GmbH Berlin
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Coverfoto Scanning electron microscopy images of a typical spiking on a silicon wafer sputtered with an aluminum layer before (left) and after (right) back-etching the aluminum layer

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1 Introduction

1.1 Thesis motivation and objectives

The majority of silicon solar cells in PV industry are fabricated on *p*-type silicon wafers with a passivated front side emitter and a non-passivated aluminum back surface field (Al-BSF) featuring screen-printed front- and rear-side metallization [1]. Though the manufacturing of such solar cells is very established in PV industry, the cell efficiency is limited mainly due to the non-passivated screen-printed rear-side. Working towards higher cell efficiencies can be a very effective way to reduce cost per kilowatt peak of PV systems. In order to reach higher cell efficiencies many approaches can be pursued as for instance by applying a passivation layer or layers to the rear-side of the cell. Rear-side passivation not only enhances the passivation quality of rear surface, but also the internal reflection. Thus, by applying a rear-side passivation, the recombination as well as optical losses at the rear side can be further minimized. Double side contacted silicon solar cells featuring passivated, locally opened rear-sides are for example passivated emitter and rear (PERC) [2], passivated emitter rear totally diffused (PERT) [3], passivated emitter rear locally diffused (PERL) [4] solar cells fabricated either on *p*-type (as for the majority of industrial silicon solar cells at present) or *n*-type silicon.

Though *n*-type silicon wafers had only 8% of the market share in 2010, their market share is expected to increase and dominate the market in the near future according to the International Technology Roadmap for Photovoltaics [5]. The reason for the expected growing interest in *n*-type silicon is due to its numerous advantages compared to the in PV industry well-established standard *p*-type silicon. For an example, *n*-type silicon has a greater immunity to many metal contaminants and impurities that are present in silicon feedstock or induced afterwards by common solar cell processes than *p*-type silicon. Therefore, silicon wafers with higher quality (immunity against recombination) can be produced with *n*-type silicon which results in potentially higher cell efficiencies. The other important feature of *n*-type silicon is that it is significantly more stable under

illumination compared to *p*-type silicon which degrade under illumination due the presence of boron and oxygen [6]. This degradation phenomenon is known as Light Induced Degradation (LID) [7]. Thus, silicon solar cells based on *n*-type silicon have more potential for reaching higher and stable cell efficiencies than on *p*-type silicon. Based on this, high efficiency rear-side passivated *n*-type PERT silicon solar cells featuring double-side screen-printed metallization were developed at Bosch Solar Energy AG. Although screen-printing is a well-established metallization technology in cell processing, it has also cost and performance related drawbacks. With the material cost involved in silver-based screen-printing metallization technology being the highest non-silicon related cost element in the production of silicon solar cells [5], solutions to reduce metallization material cost have to be found. This can be done either by reducing total paste consumption or by replace silver with another cheaper material like copper. Within this work the focus was on a complete replacement of screen-printing technology with other metallization technologies which can assure a reduction of cost per kilowatt peak either by decreasing costs or increasing cell performance or ideally both. Deposition of metal layers with physical vapor deposition (PVD) techniques as evaporation or sputtering deposition can be considered as an attractive metallization choice to replace screen-printing in advanced *n*-type silicon solar cell concepts as PERT solar cells. Physical vapor deposited metal layers offer a number of additional advantages compared to the established screen-printed paste solution due to its compact structure compared to the porous screen-printed layers. PVD metal layers have significantly lower bulk resistivity and lower contact resistance with silicon which in turn means less ohmic losses in the cell. In addition, they can form ohmic contact with silicon at significantly lower sintering temperatures. When they are applied to the rear-side of the cell, some PVD metals can enhance the internal reflection and thus current generation due to their very high reflectivity. They can also fill small contact openings easier compared to screen-printed metal layers which can be very beneficial for some cell designs. Last but not least, the majority of PVD metal layers can be easily deposited by evaporation or sputtering which are well established technologies in other industries like integrated circuits [8]. In recent years, many manufacturers started to adopt this technology to wafer-sized

silicon solar cells on a production scale (e.g. [9-12]) as it fulfills the metallization requirements of advanced cell structures. In spite of these advantages of PVD metal layers, not so many works and investigations have been done on the potential of applying PVD metallization for large scale *n*-type silicon solar cells.

Considering the potential advantages of PVD metal layers, large-area front-junction *n*-type PERT (nPERT) silicon solar cells featuring screen-printed front-side and physical-vapor-deposited rear-side metallization were developed at Bosch Solar Energy during this thesis. The main objective of this work was to define the requirements of rear-side metallization for high efficiency nPERT solar cells and develop one-layer or multi-layer rear-side PVD metallization which fulfils these requirements. Therefore, the impact of various PVD metals on each of these requirements was investigated in detail. The PVD technology used in this work was sputtering deposition. Instead of the PVD technology, the thesis, however, focuses mainly on the various PVD-metals and their influence on cell performance. At the end of the thesis, large-area front-junction nPERT silicon solar cells featuring screen-printed front-side metallization and physical-vapor-deposited rear-side metallization were fabricated. Within this work a cell efficiency of 20.88 % could be obtained which is also independently confirmed by Fraunhofer ISE CalLab PV Cells. To the knowledge of the author this is the highest published cell efficiency of large-area front-junction nPERT silicon solar cells featuring at least one screen-printed side.

1.2 Thesis outline

Chapter 2 presents the fundamentals of large-area front-junction nPERT silicon solar cells featuring PVD rear-side metallization. First, the basics of nPERT solar cells are described. The device structure, working principle, current-voltage characteristics of this type of solar cells and the impact of optical and electrical losses on current-voltage characteristics are explained. Afterwards, the state of the art of rear-side metallization for *n*-type silicon solar cells and a novel cell design featuring the well-established screen-printed front-side metallization combined with PVD rear-side metallization is presented. The basics of PVD metallization are also described. In addition, the losses caused by rear-side metallization are discussed and its requirements are defined. Finally and

based on simulations and cost calculations, aluminum as a main conducting metallization layer of the rear-side metallization to be developed in the thesis is defined.

In **Chapter 3** the sputtering deposition system and the metallization processes used in this work are presented.

Chapter 4 deals with the contact formation process of aluminum-based rear-side metallization. Process simulations and scanning electron microscopy (SEM) structural investigations on the contact-formation process and the spiking phenomenon between aluminum and silicon are carried out. Solutions to prevent aluminum spiking are presented, investigated and discussed. A novel approach featuring Al-Si/Al stack is developed and presented.

In **Chapter 5**, a detailed study of the contacting electrical performance of various aluminum-based metallization schemes on point contacts is investigated in detail. A new characterization method to determine the specific contact resistance of metal-semiconductor point contacts on highly doped silicon is presented. By using this method the specific contact resistance of the various aluminum-based metallization variants on n^+-doped silicon is determined (Al, Al-Si, Al-Si/Al and Ti/Al stack).

In **Chapter 6**, the impact of rear-side metallization on the optical performance of nPERT silicon solar cells is investigated. First, analytical simulations regarding back-side reflectance of PERT solar cells with textured front side and planar rear-side are carried out. Based on the results of the analytical simulations, experiments and numerical ray-tracing simulations with specific test samples are performed. The simulation and experimental results are presented and discussed.

In **Chapter 7,** the damage of silicon-passivation interfaces during plasma-enhanced PVD deposition (e.g. sputtering or e-beam deposition) is investigated. Various passivation layers as SiO_2, Al_2O_3 and SiN_x are investigated. The focus lies on SiN_x passivation, since the nPERT solar cells developed in this thesis feature this layer.

In **Chapter 8** the solar cell results of front-junction nPERT solar cells featuring front-side screen-printed and rear-side PVD metallization are presented. The impact of various aluminum-based rear-side metallization variants on cell performance is investigated and compared to the results obtained from the test samples of the previous chapters.

Chapter 9 summarizes the thesis and gives an outlook.

2 Fundamentals

This thesis deals with physical-vapor-deposited rear-side metallization for large-area front-junction *n*-type *passivated emitter rear totally diffused* (nPERT) silicon solar cells. In this chapter, the device structure, working principle, current-voltage characteristics of this type of solar cells and the impact of optical and electrical losses on current-voltage characteristics are explained. Afterwards, the state of the art of rear-side metallization for *n*-type silicon solar cells and a novel cell design featuring the well-established screen-printed front-side metallization combined with PVD rear-side metallization is presented. The basics of PVD metallization are also presented. In addition, the losses caused by rear-side metallization are discussed and its requirements are defined. Finally and based on simulations and cost calculations, aluminum as a main conducting metallization layer of the rear-side metallization to be developed is defined.

2.1 Basics of silicon solar cells

2.1.1 Device structure and working principle of front-junction nPERT silicon solar cells

Sketches of typical industrial *p*-type as well as front-junction nPERT silicon solar cells are shown in Figure 2.1.

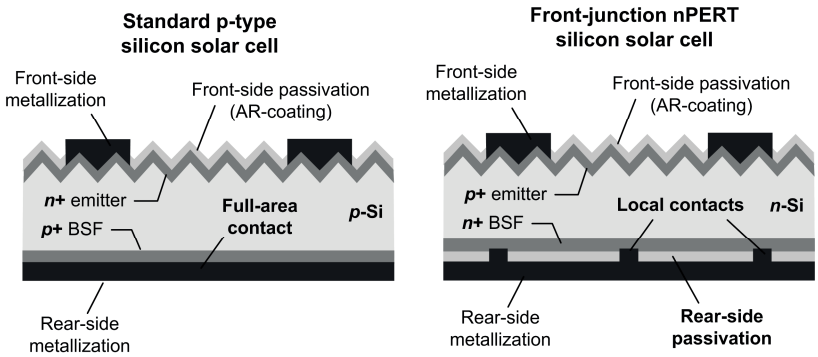

Figure 2.1: A sketch of a standard p-type silicon solar cell (left) and of a front-junction nPERT solar cell (right).

Both devices are in principle *p*-*n*-junctions with a relatively thin emitter on the front (usually 0.2 - 2 µm) and a thick base (usually 50 - 250 µm). The base material is either *p*-type as for typical industrial solar cells or *n*-type as for nPERT solar cells with the emitter being of the opposite polarity. At the interface layer between the emitter and the base, a region depleted of free charge carriers – the so called depletion or space charge region – is formed. Since the space charge region is depleted of free carriers, a built-in electric field is formed. Under irradiation electron-hole pairs are generated in the cell which are separated due to the built-in electric field in the space charge region. The built-in electric field causes the minority carrier of the generated electron-hole pairs in the emitter and the base to diffuse to the space charge region. Afterwards the minority carriers reach the opposite region where they become majority carriers. The majority carriers at each side can then be collected through metal contacts (the metallization) via an external load. The metallization on the front is patterned for both devices (metallization grid) in order to let the light reach the cell and generate carriers. The front-side is also textured and coated with an anti-reflection layer or layer-stack in order to let more light in and further reduce optical losses. The main difference between the structures of both devices is the rear-side. Whereas the rear-side of a typical industrial solar cell features a full-area contact, the rear-side of PERT solar cells features local linear or point contacts. The reason of this is the passivation layer or layer-stack on the rear-side of PERT solar cells in comparison to the typical industrial solar cells which do not feature any passivation layers on the rear-side. Rear-side passivation has two major advantages. Firstly, it reduces the recombination probability on the rear surface remarkably which in turns means mainly higher cell voltage. Secondly, it can increase the internal reflection of the light reaching the rear-side so the photons have a higher probability to generate carriers which in turns means a higher generated current. The rear-side of both devices is also highly doped beneath the contact in order to enable low ohmic contact between the silicon material and the metallization. The highly doped layer at the rear-side also enables surface passivation via an electric field and is therefore called back surface field (BSF).

2.1.2 Current-voltage characteristic of silicon solar cells

As silicon solar cell is basically a large area diode, its current-voltage characteristic under illumination obeys theoretically the diode equation but with additional current shift due to the photo generated current density J_{ph}

$$J = J_{01}\left(e^{\frac{V}{n_1 V_{th}}} - 1\right) - J_{ph}. \tag{2.1}$$

Here, J is the current density across the diode, V is the voltage diode and $V_{th}=kT/q$ is the thermal voltage where k is the Boltzmann constant, T is the temperature and q is the elementary charge. J_{01} is the recombination current density (or dark saturation current density) which describes recombination processes in the emitter and the base and at their surfaces. The ideality factor n_1 is a measure of how closely the cell follows the ideal diode equation. For an ideal diode with no recombination in the space charge region and either Shockley-Read-Hall (SRH) or low level injection band-to-band recombination in the other regions, the ideality factor equals one. In reality, however, there are defects in the space charge region which give rise to recombination processes there. These recombination processes are described with the recombination current J_{02}. For middle-band-gap defects in the space charge region the ideality factor equals two. Furthermore, a real solar cell also includes parasitic parallel resistance R_p (e.g. due to shunting) and series resistance R_s (e.g. resistivity of the base or emitter, of the metallization or of the semiconductor-metal contacts). Taking these characteristics into account, the one-diode-model of the solar cell is extended to a two-diode model

$$J = J_{01}\left(e^{\frac{V-JR_s}{n_1 V_{th}}} - 1\right) + J_{02}\left(e^{\frac{V-JR_s}{n_2 V_{th}}} - 1\right) + \frac{V - JR_s}{R_p} - J_{ph}. \tag{2.2}$$

Figure 2.2 (left) shows the equivalent circuit of a solar cell based on the two-diode model. The first diode describes the recombination current in the base, emitter and at the surfaces whereas the second diode represents the recombination current in the space charge region. The resistance elements R_s and R_p correspondingly model the electrical losses as aforementioned.

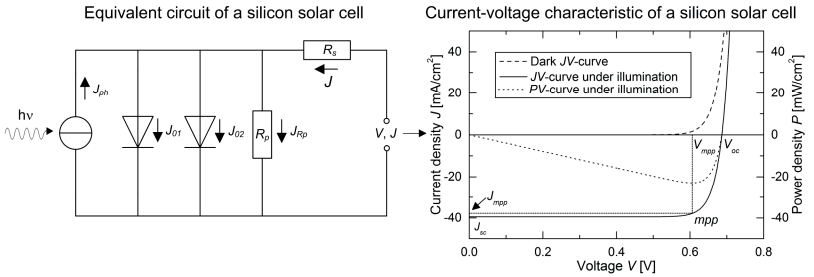

Figure 2.2: Equivalent circuit (left) and current-voltage characteristic (right) of a silicon solar cell.

Typical current-voltage characteristics (*JV*-curves) of a real solar cell in dark and under illumination are shown in Figure 2.2 (right). The basic parameters describing the solar cell are

- Short-circuit current density J_{sc}
- Open-circuit voltage V_{oc}
- Maximum power point *mpp*
- Current density at maximum power point J_{mpp}
- Voltage at maximum power point V_{mpp}
- Fill factor *FF*
- Energy conversion efficiency η.

These parameters are measured under standard test conditions of perpendicular irradiation with an intensity of 1 kW/m² (1 sun, AM1.5 spectrum) at 25 °C [13].

The dark *JV*-curve (dashed line) is shifted by the short-circuit current density J_{sc} when the cell is illuminated. Thus, the short-circuit current density J_{sc} is the intersection point of the illuminated curve with the current axes. The open-circuit voltage V_{oc} is the intersection point of the illumination curve with the voltage axes. Without taking ohmic losses of a real solar cell into account (i.e. $R_s \rightarrow 0$ and $R_p \rightarrow \infty$) the short-circuit current density J_{sc} equals the photo current density J_{ph}.

The maximum power point *mpp* is the point in the illuminated curve at which the maximum power is obtained from the cell ($P_{max} = J_{mpp}V_{mpp}$). The ratio of P_{max} and the product $J_{sc}V_{oc}$ defines the fill factor of the cell

$$FF = \frac{P_{max}}{J_{sc}V_{oc}} = \frac{J_{mpp}V_{mpp}}{J_{sc}V_{oc}}. \tag{2.3}$$

The fill factor is the fraction of the rectangle $V_{mpp}J_{mpp}$ filling the rectangle curve $V_{oc}J_{sc}$ and thus is a measure of how square the output characteristic of the cell is. Without taking the ohmic losses into account, the ideal (maximum) fill factor FF_0 is a function of only V_{oc} [14]

$$FF_0 = \frac{\upsilon_{oc} - ln(\upsilon_{oc} + 0.72)}{\upsilon_{oc} + 1}. \tag{2.4}$$

Here, $\upsilon_{oc} = V_{oc}/(kT/q)$ is a normalized open-circuit voltage.

The energy conversion efficiency η is the ratio of the maximum generated power density under illumination P_{max} and the irradiated power density P_{irr}

$$\eta = \frac{P_{max}}{P_{irr}} = \frac{J_{mpp}V_{mpp}}{P_{irr}} = \frac{J_{sc}V_{oc}}{P_{irr}}. \tag{2.5}$$

2.1.3 Carrier recombination in crystalline silicon

Under generation (i.e. $pn > n_i^2$, where n_i is the intrinsic carrier concentration in silicon) the thermal-equilibrium condition of the solar cell is disturbed. This leads to recombination processes to restore the system back to equilibrium (i.e. $pn = n_i^2$) [15]. For solar cells operating under one-sun applications, carrier recombination is relevant for minority carriers (i.e. electrons in the *p*-doped region and holes in the *n*-doped region). The generated electrons in the *p*-doped or holes in the *n*-doped region have to travel to the *p*-*n* junction without being lost in recombination processes in order to contribute to the cell power.

Recombination of minority carriers is described with the minority carrier lifetime τ which is the average time it takes for minority carriers to recombine

$$\tau \equiv \frac{\Delta N}{U}, \tag{2.6}$$

where U is the net recombination rate and ΔN is the excess minority carrier concentration [14] ($\Delta N = \Delta n$ in *p*-type silicon and $\Delta N = \Delta p$ in *n*-type silicon).

Carrier recombination is very well-studied in semiconductors (e.g. [14], [15]). In bulk silicon there are three recombination processes possible with an assigned lifetime for each of them [14]. Two of them are intrinsic processes (radiative and Auger recombination) and the other one is extrinsic (*SRH*-recombination). The assigned lifetimes are $\tau_{radiative}$, τ_{Auger} and τ_{SRH}, respectively.

Radiative recombination is simply the inverse process of photon absorption [14]. The generated electron in the conduction band recombines with a hole in the valence band releasing the excess energy by a photon. This recombination process is less important for indirect semiconductors like silicon, as one or more phonons are required in the process to fulfill the energy and momentum conversation rule. In **Auger recombination** the excess energy of the recombination process is transferred to another electron in the conduction band or hole in the valence band [14]. The second electron or hole relaxes again by emitting phonons. While both intrinsic recombination processes are independent of material quality, the extrinsic **SRH recombination process** depends highly on impurities and defects present in the silicon material. Defects and impurities introduce energy levels in the silicon band gap where charge carriers might get trapped to either be reemitted or recombined. Further details about intrinsic and extrinsic recombination process in silicon can be found in [14] or [16]. These recombination processes can occur in parallel. The bulk lifetime of minority carriers τ_{bulk} is thus given by the reciprocal sum of these individual recombination processes [16]

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{radiation}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}}. \tag{2.7}$$

In real solar cells where the bulk material is finite, carrier recombination can also occurs at the surfaces of the silicon material. At the silicon surface there are unsaturated chemical bonds (dangling bonds). They generate energy levels within the band gap of silicon where charge carriers may recombine. The corresponding carrier lifetime for surface recombination is τ_s. Commonly, surface recombination is described by surface recombination velocity S (measured in cm/s)

$$S \equiv \frac{U_s}{\Delta N_s}, \tag{2.8}$$

where U_s is the surface recombination rate and ΔN_s is the excess minority carrier density at the surface, respectively.

The measured carrier lifetime of a semiconductor device describing both bulk and surface recombination is called the effective carrier lifetime τ_{eff} and is given by

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}}. \tag{2.9}$$

For good passivated surfaces with small values of S equation (2.9) can be approximated with

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S}{W}, \tag{2.10}$$

where W is wafer thickness [16].

For very large surface recombination velocities (e.g. non passivated surfaces), the recombination is limited by the diffusion of the carriers to the surface D. In this case, the effective carrier lifetime is given by [16]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{D\pi^2}{W^2}. \tag{2.11}$$

2.1.4 Impact of electrical and optical losses on current-voltage characteristic

Crystalline silicon solar cells have conversion efficiencies less than 25 $\%_{abs}$ due to electrical losses, optical and band gap losses (Figure 2.3). Electrical losses are the ohmic and recombination losses. Optical losses are when irradiation is not absorbed by the absorber (e.g. back reflected or transmitted light). Band gap losses can also be seen as optical losses. They are resulting from photon energies higher or lower than the band gap of silicon. Photons with lower energy than the bang gap are not absorbed and thus will not contribute to the cell efficiency. The excess of energy of photons with a higher energy than the band gap will be lost as a heat or in parasitic absorption (e.g. from free electrons). In the following the impact of the electrical and optical losses on current-voltage characteristic are described and in section 2.3 rear-side metallization related losses are discussed.

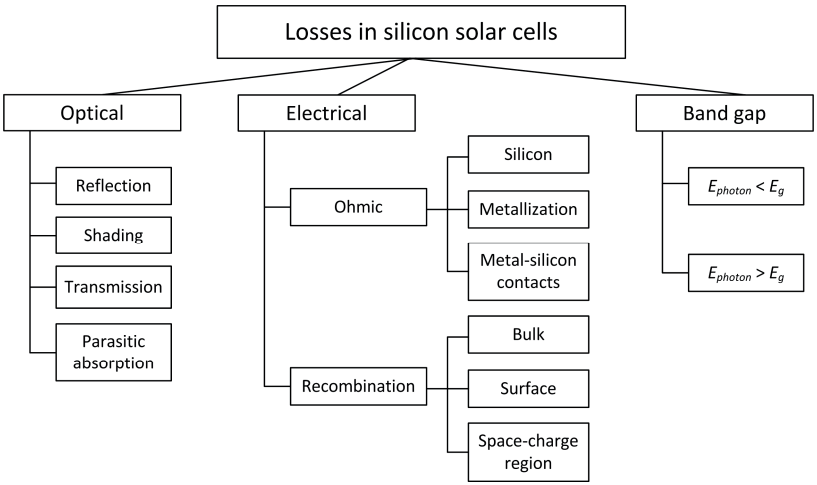

Figure 2.3: Losses in silicon solar cells which lead to energy conversion efficiency far less than 100% (after [16]).

Impact of ohmic losses on current-voltage characteristic

Parasitic series and parallel ohmic losses have a huge impact on the cell characteristic, mainly on the fill factor [14]. Series ohmic losses are e.g. the bulk resistance of the wafer, sheet resistance of the highly doped regions, resistance

of metallization, resistance between the metallization and the cell (the contact resistance). A leakage across the *p-n* junction at the edge of the solar cell is an example for a parallel ohmic loss. Both series and ohmic losses cause a reduction of the fill factor. The fill factor *FF* in presence of series and parallel ohmic losses is given by equations (2.12) and (2.13), respectively [14].

$$FF_s = FF_0\left(1 - \frac{J_{sc}}{V_{oc}}R_s\right) \tag{2.12}$$

$$FF_p = FF_0\left(1 - \frac{(\upsilon_{oc} + 0.7)}{\upsilon_{oc}}\frac{V_{oc}FF_0}{J_{sc}R_p}\right) \tag{2.13}$$

Equation (2.12) is valid for $\upsilon_{oc} > 10$ and $(R_sJ_{sc}/V_{oc}) < 0.4$ while equation (2.13) for $\upsilon_{oc} > 10$ and $(R_pJ_{sc}/V_{oc}) > 2.5$. Figure 2.4 shows simulated *JV*-characteristic of an nPERT solar cell for various R_s and R_p values. While the maximum power point is directly affected by the ohmic losses due to reduced fill factor, V_{oc} and J_{sc} are only reduced for very high R_s or very low R_p.

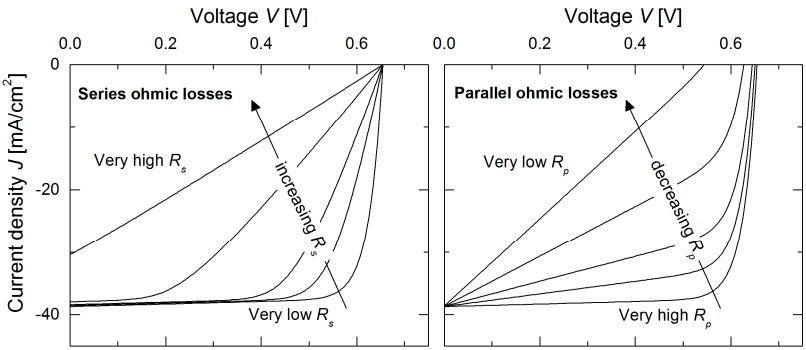

Figure 2.4: The impact of series and parallel ohmic losses on current-voltage cell characteristic.

Impact of recombination losses on current-voltage characteristic

Recombination losses have the highest impact on V_{oc} but also on J_{sc}. A simplified illustration of this is the ideal diode equation (2.1). At open-circuit voltage

condition and without taking the ohmic losses into account, the diode current J equals zero and J_{ph} equals J_{sc}. In this case equation (2.1) will be

$$0 = J_{01}\left(e^{\frac{V_{oc}}{n_1 V_{th}}} - 1\right) - J_{sc}. \tag{2.14}$$

Solving equation (2.14) for V_{oc} gives (with taking into account that $J_{ph} >> J_{01}$)

$$V_{oc} = n_1 V_{th} ln\left(\frac{J_{sc}}{J_{01}}\right). \tag{2.15}$$

Equation (2.15) shows that a higher recombination current J_{01} will reduce the open-circuit voltage of the cell.

In Figure 2.5 the impact of the recombination losses on the whole JV-curve is shown. In Figure 2.5 the recombination current density of the first diode J_{01} – which describes recombination in the base and the emitter and at the cell surfaces – is varied resulting in a reduction of V_{oc} when J_{01} increases.

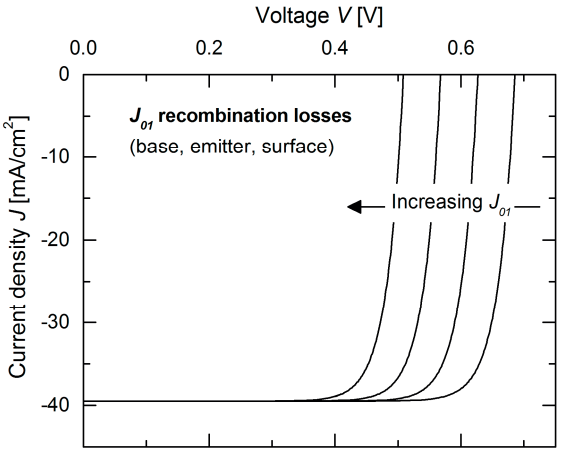

Figure 2.5: The impact of recombination losses in the base, emitter and at the surfaces (J_{01}-losses) on current-voltage cell characteristics.

Impact of optical losses on current-voltage characteristic

Non-absorbed photons in the cell leads to a reduction in the generated photocurrent density J_{ph} and thus a reduction in the short current density J_{sc}. Non-converted photons can be e.g. reflected photons off the front surface or the front side metallization, non-absorbed photons in the silicon, or photons lost in parasitic absorption in the rear side metallization or in the passivation layers [16].

2.2 Rear-side metallization of silicon solar cells

2.2.1 Review and state of the art

Rear-side metallization of a typical industrial silicon solar cell is a screen-printed aluminum layer without a passivation layer beneath it (Figure 2.7-a). Screen-printed aluminum is perfectly suited to *p*-type solar cells as it forms both the back surface field BSF and the metal-semiconductor contact during sintering [1], [17]. Aluminum is an acceptor-dopant in silicon and forms a highly doped p^+-Si layer during the high temperature sintering process. However, for advanced *n*-type cell structures (e.g. nPERT) screen-printed aluminum has its limitation contacting *n*-type silicon. Screen-printed aluminum cannot form an ohmic electrical contact to *n*-type silicon because it will form a p^+-doped silicon layer during sintering. Three different ways can be done in order to overcome this issue for double-side contacted *n*-type silicon solar cells which are illustrated in Figure 2.7-b, -c and -d.

The three approaches are:

- **Using different pastes to aluminum paste which can contact *n*-type silicon (Figure 2.7-b)** [18], [19]**.** Screen-printed silver-containing pastes can contact highly doped *n*-type silicon. These pastes are, however, cost-intensive due to the high material cost of silver. Therefore, in this case bifacial solar cells with grid metallization on both sides instead of full-area metallization on the rear side are usually used in order to spare silver material cost and thus metallization cost (Figure 2.7-b). Large-area bifacial screen-printed nPERT solar cells for

industrial production with cell efficiency up to 20.5 $\%_{abs}$ are reported (e.g. nPERT of Bosch Solar Energy [18], [20], nPERT of ECN (n-Pasha cell) [19]).

- **Using back-junction instead of front-junction cell design (i.e. n^+np^+ instead of p^+nn^+, Figure 2.7-c).** By moving the n^+ doped region to the front-side of the cell, the rear-side can be metallized with screen-printed aluminum. By doing this, the screen-printed aluminum on the rear will form a p^+-emitter on the n-type silicon wafer during sintering (instead of a p^+-BSF on p-type silicon as for typical p-type silicon solar cells). The main advantage of this concept in comparison to the previous one is its simple processing sequence, since almost the same processing sequence as for standard n^+pp^+ cell can be used. For this type of solar cells, however, a higher quality of bulk silicon is required than for front emitter solar cells. In comparison to front emitter solar cells, the generated electron-hole pairs have to move through the whole cell in order to reach the p-n junction at the back which increases the probability of recombination in the bulk silicon. Cell efficiencies up to 20 $\%_{abs}$ are reported for this type of solar cells [21] with a theoretical potential of reaching 21 $\%_{abs}$ [22].

- **Using other metallization technology than screen-printing (Figure 2.7-d).** Physical vapor deposited (PVD) metal layers can be considered as an ideal choice for rear-side metallization to replace screen-printed aluminum in advanced n-type silicon solar cell concepts. They can be easily deposited by evaporation or sputtering and are well established in other industries like integrated circuits [8]. PVD metal layers can contact both p-type and n-type silicon and at less surface dopant concentration than screen-printed metal layers. In addition, PVD metals have significantly higher conductivity than screen-printed ones, due to their compact atomic structure (Figure 2.6). Furthermore, many PVD metals can be plated if a thick metallization is needed for sufficient current transport.

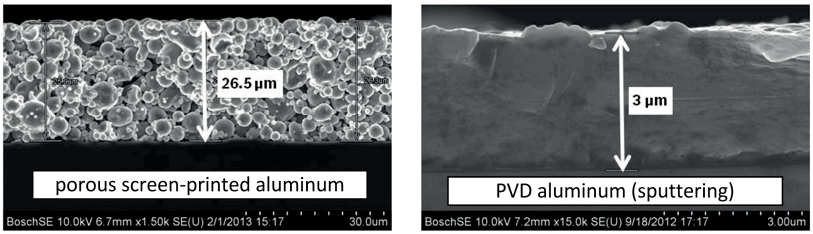

Figure 2.6: Screen-printed vs. physical vapor deposited aluminum. Due to the compact structure of PVD-Al compared to the porous structure of screen-printed Al, PVD-Al has better electrical and optical properties than screen-printed Al.

In recent years, many manufacturers started to adopt this technology to wafer-sized silicon solar cells on a production scale (e.g. [9-12]). However, there are not so many studies on rear-side PVD metallization for silicon solar cells, especially when contacting n^+-silicon. The most reported PVD metal for contacting the rear-side of large area *n*-type silicon solar cells is PVD-Al as for small high efficiency labor solar cells (e.g. [23], [24]). Apart from PVD-Al, there are some other one-layer or multi-layer PVD metallization schemes for large-area *n*-type silicon solar cells as e.g. Ag [25], Ti/Pd/Ag [26], AlSi/TiW/Cu [27], ITO/Ag [25], Al/NiV/Ag [28]. The impact of rear-side metallization of large-area *n*-type silicon solar cells on contact formation, rear-side reflection, metallization-induced damage, current transport, interconnectability, material cost are some reasons for this variation. In this thesis these issues are investigated.

2.2.2 Novel cell design featuring screen-printed front side and physical vapor deposited rear-side metallization

As mentioned in the previous section, a very promising rear-side metallization approach to replace screen-printing for industrial *n*-type silicon solar cells is PVD metallization. PVD metallization can be applied to the rear-side of either front- or back-junction nPERT solar cells.

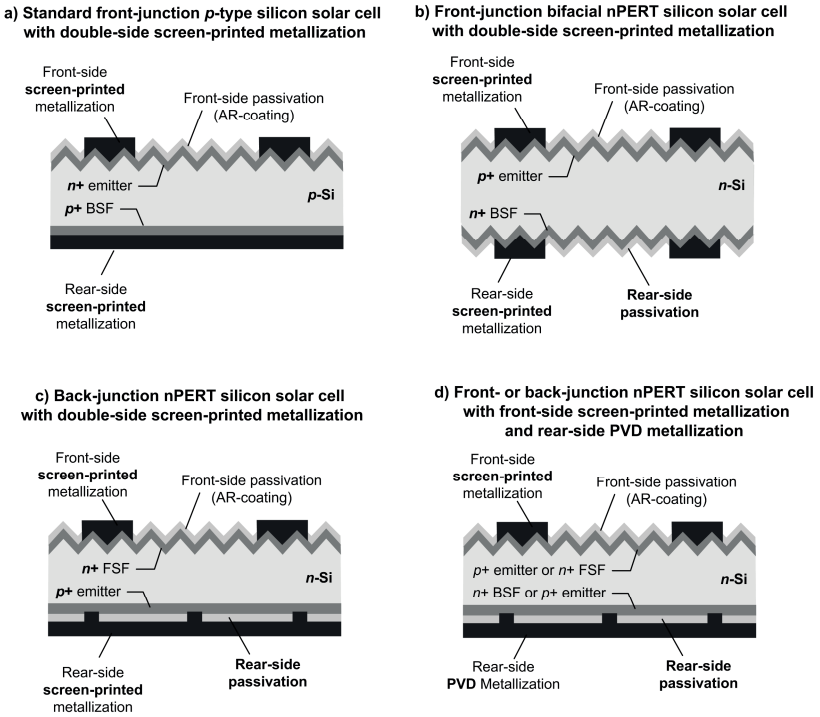

Figure 2.7: Various cell design of double-side contacted n-type silicon solar cells.

In this work, a novel cell design featuring rear-side PVD metallization is developed. The cell design features **front-junction nPERT** silicon solar cell with typical industrial front-side screen-printing metallization and a PVD rear-side metallization (Figure 2.8). To the knowledge of the author, there are similar solar cells featuring both screen-printing and PVD metallization, however, using other cell structures than front-junction nPERT. In 2011, Bordihn et al. [24] published large-area **back-junction nPERT** solar cells featuring screen-printed front-side and Al-PVD rear-side metallization with best cell efficiency of 20.2 $\%_{abs}$. In 2013, Steinhauser et al. [23] reported 20.1 $\%_{abs}$ cell efficiency on **front-junction nPERL** solar cells (PERL: Passivated Emitter Rear Locally doped) featuring screen-printed front-side and Al-PVD rear-side metallization.

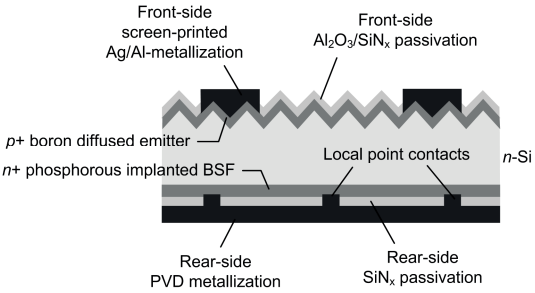

Figure 2.8: nPERT cell structure featuring rear-side PVD metallization developed in this thesis.

A sketch of the cell structure is shown in Figure 2.8. The solar cell is fabricated using 156 × 156 mm² pseudo-square *n*-type Czochralski-grown silicon wafers (Cz-Si) [29] with an initial thickness of 180 µm. The front side is textured, boron doped, passivated with Al_2O_3/SiN_x stack and metallized with industrial Ag/Al screen-printed pastes. The rear side of the cells is planar, phosphorous doped and passivated with SiN_x which is locally opened with picosecond laser ablation (point contacts) in order to enable a physical contact between the rear-side metallization and the silicon wafer. As aforementioned, the rear-side is metallized by physical vapor deposition which is the main subject of this thesis. The processing sequence and the technologies used to fabricate this solar cell is described in Chapter 8.

2.2.3 Physical vapor deposition of metal layers

Physical vapor deposition (PVD) of thin or thick metal layers is extensively used in various industries with a wide range of applications (e.g. for optical, mechanical or electrical coatings). Depending on the field of application, the thickness of the deposited layers varies from sub-nanometers to millimeters. Although there are many PVD deposition methods, they are basically categorized in two general groups

- Sputtering deposition (e.g. DC, RF sputtering)
- Evaporation deposition (e.g. thermal or electron-beam evaporation).

In both deposition methods the atoms of the material to be deposited is controllably transferred in high vacuum from a source to the substrate (e.g.

silicon wafer) where the layer is grown atomistically [30]. The main difference between the two methods is the transition of the component to be deposited from the solid to the vapor phase. In sputtering deposition the atoms of the component are dislocated from a solid source (target) through impact of gaseous ions (in other words sputtering of a target), whereas in evaporation deposition the atoms are removed by heating of an evaporation source (resistance or an electron-beam). Figure 2.9 shows schematically the principle of both techniques.

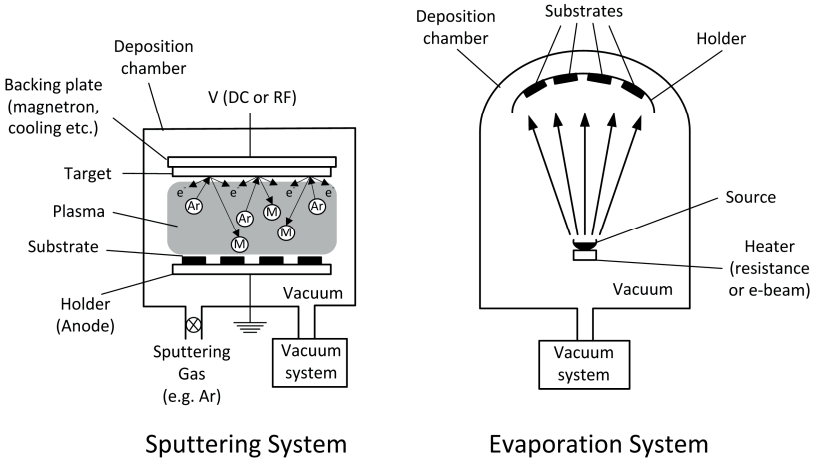

Figure 2.9: Sketches of the two major physical vapor deposition techniques: sputtering (left, modified after [30]) and evaporation deposition (right, modified after [31]).

The choice of the deposition method for a specific device depends on many factors and is not a straightforward decision. Nevertheless, it is worth mentioning the main advantages and disadvantages of each method [31]. The main advantage of evaporation deposition is the high deposition rate and thus this method is more suited for cell concepts where thick metallization is required. Furthermore, evaporated films usually have higher purity than sputtered ones because of the high vacuum condition used by evaporation deposition. One other important criterion is the plasma-induced irradiation damage which is not present in thermal evaporation as it is not a plasma-enhanced deposition technique, unlike sputtering or e-beam deposition techniques. The main advantage of a sputtering system is its flexibility and

reproducibility since film composition is better controlled in sputtering than evaporation deposition. Furthermore, it is better suited for multi-layer metallization especially for thin layers. Another big advantage of a sputtering system is the capability to do in situ plasma cleaning of substrate surfaces prior to deposition.

As mentioned in the introduction of this thesis, the aim of this thesis is not to evaluate and compare both deposition methods in order to choose the better one for rear-side metallization of nPERT solar cells. The thesis focuses mainly on PVD metallization materials and their impact on the cell performance, regardless of the PVD deposition technique used. For the deposition of the investigated PVD materials in this work, an Oerlikon SOLARIS multi-layer sputtering deposition system is used which is described in Chapter 3 along with the sputtering processes used in this work. In the following, the basics of DC sputtering process – which is the process used in the SOLARIS 6 system – are described.

DC-sputtering deposition of metal layers using planar magnetron technology

As aforementioned, the metal layers investigated in this work were deposited using a SOLARIS DC-sputtering system featuring planar magnetron technology. DC-sputtering is a sputtering deposition process in which a DC (direct current) power supply is applied. The target is connected to the negative terminal of the DC power supply (thus identified as a cathode) and the substrate carrier is usually grounded (thus identified as an anode). A plasma (glow discharge) in the process chamber is required in order to execute a sputtering process. In order to produce a plasma in the process chamber an inert gas (e.g. Ar) is introduced into the chamber after evacuation. Some of the gas atoms become ionized (positive ions) under DC power supply. As a result, the gas in the process chamber always contains a small amount of gas ions. This means that some process gas atoms are split up into positive argon ions and negative electrons in accordance with the following chemical reaction: $Ar \rightarrow Ar^+ + e^-$.

The applied electric field accelerates the argon ions to the cathode (i.e. the target) and the free electrons to the anode (i.e. substrate). In the process, the accelerated

electrons collide with further atoms and ionize these atoms with their kinetic energy. The above process is repeated continuously and therefore produces an avalanche of argon ions and electrons. The plasma ignites. The process gas serves therefore as the medium in which the plasma is initiated and sustained. The positive gas ions in the plasma strike the negative connected target and remove neutral target atoms via momentum transfer. The ejected atoms from the target enter and pass through the plasma to eventually deposit on the substrate creating the deposited film. Apart from the target atoms other particles as well as irradiation are emitted from the target which can also hit the substrate and eventually causing damage to it (plasma-induced damage) [32]. These particles are secondary electrons, desorbed gases, negative ions and the irradiation is X-rays and photons.

When a magnetron is positioned behind the target, a magnetic field compels the free electrons to additional circular movements so that they all move in helical (screw-like) paths. This lengthens the electron path, thereby increasing the probability of collisions between electrons and gas atoms. The degree of dissociation of the process gas and therefore the plasma density is increased accordingly. The magnetron technology offers the following advantages over conventional sputtering systems: highly stable plasma, increased sputtering rate, decreased sputtering voltage (i.e. low particle energy), performs well even at low gas pressure.

2.3 Rear-side metallization related losses

2.3.1 Ohmic losses due to lateral resistance of rear-side metallization

In section 2.1.2, it was shown that real solar cells have a parasitic series resistance which reduces the fill factor. In this section, the contribution of the lateral electrical resistance of the rear-side metallization $R_{s,m}$ to the series resistance of the solar cell R_s is calculated. In addition, the fill factor loss and efficiency loss due to the ohmic loss in the rear-side metallization is simulated as a function of the busbar-busbar-resistance R_{bb} and the sheet resistance R_{sh}. Since electrical conductance is material and thickness dependent, the simulations are also done as a function of metallization thickness d_{metal} and resistivity ϱ_{metal}.

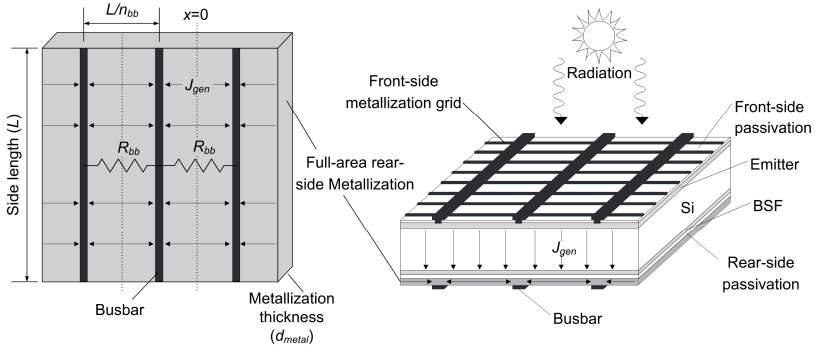

Figure 2.10: Sketch of a full-area rear-side metallization of a 3-busbar PERT solar cell.

Figure 2.10 shows a sketch of a rear-side metallization of thickness d_{metal} (left-hand side) of a 3-busbars PERT solar cell (right-hand side). The generated current in the solar cell j_{gen} is collected by the rear-side metallization via the contact holes and diverted horizontally within the metallization into the collecting busbars (or ribbons) as shown schematically in Figure 2.10. The generated current experiences lateral ohmic loss in the rear-side metallization layer on its way to the busbars. The required lateral conductance of the rear-side metallization for a negligible ohmic loss can be controlled either by measuring the sheet resistance R_{sh} of the metallization or by measuring the busbar-busbar resistance R_{bb} between two busbars. The latter is usually measured during cell flashing in the production line and is thus suitable for controlling the quality of the metallization in mass production. Another use of the busbar-busbar-method is the ability to compare the quality of PVD-metallization with other common metallization e.g. screen printed metallization which cannot be characterized by measuring the sheet resistance if it is a grid metallization as for bifacial solar cells. Nevertheless, for characterizing the conductance of sputtered or evaporated metallization layers, the sheet resistance measurement is very suitable and widely used in microelectronics. In this section both methods will be compared for the evaluation of the conducting quality of the rear-side metallization.

The sheet resistance of a metal layer R_{sh} with a layer thickness d_{metal} and resistivity ρ_{metal} is defined as

$$R_{sh} = \frac{\rho_{metal}}{d_{metal}}. \tag{2.16}$$

$$R_{bb} = \int_{-L/2n_{bb}}^{+L/2n_{bb}} \frac{\rho_{metal}}{L \cdot d_{metal}} dx = \frac{\rho_{metal}}{n_{bb} \cdot d_{metal}} = \frac{R_{sh}}{n_{bb}}, \tag{2.17}$$

where L is the side length of the solar cell and n_{bb} is the number of busbars. The busbar-busbar resistance is thus equal to the sheet resistance R_{sh} divided by the number of the busbars n_{bb}.

To calculate the impact of the lateral electrical resistance of the rear-side metallization on cell performance, the power loss method of Goetzberger [16] is applied. In this method, the current generation is assumed to be homogeneous which is valid for silicon solar cells under one sun illumination power. Under this assumption, the current I_m at distance x is given by

$$I_m(x) = j_{gen} \cdot L \cdot x, \tag{2.18}$$

where j_{gen} is the generated current.

The current at the busbar I_{max} is thus

$$I_{max} = j_{gen} \cdot L \cdot \frac{L}{2n_{bb}} = \frac{j_{gen} \cdot L^2}{2n_{bb}}. \tag{2.19}$$

The power loss in the metallization P_m can be written as

$$p_m = {I_{max}}^2 \cdot R_{s,m}[\Omega] = \frac{{j_{gen}}^2 \cdot L^4}{4{n_{bb}}^2} \cdot R_{s,m}[\Omega], \tag{2.20}$$

where $R_{s,m}$ [Ω] is the series resistance contribution of the metallization to series resistance of the whole solar cell under illumination in the unit Ω.

On the other hand, the power loss in the metallization is also given by

$$\begin{aligned} p_m &= \int_0^{L/2n_{bb}} I^2(x) \cdot dR \\ &= \int_0^{L/2n_{bb}} \left(j_{gen} \cdot L \cdot x\right)^2 \frac{\rho_{metal}}{L \cdot d_{metal}} \cdot dx \\ &= \frac{{j_{gen}}^2 \cdot L^4}{4{n_{bb}}^2} \cdot \frac{\rho_{metal}}{6 \cdot n_{bb} \cdot d_{metal}}, \end{aligned} \tag{2.21}$$

By comparing equations (2.20) and (2.21), the series resistance contribution of the metallization $R_{s,m}$ [Ω] can be found

$$R_{s,m}[\Omega] = \frac{\rho_{metal}}{6 \cdot n_{bb} \cdot d_{metal}} = \frac{R_{sh}}{6 \cdot n_{bb}} = \frac{R_{bb}}{6}. \tag{2.22}$$

The series resistance loss due to the lateral resistance in the metallization is thus a sixth of the bus-bar-resistance or a sixth of the sheet resistance divided by the number of the busbars. In order to get the series resistance loss in the unit Ωcm², equation (2.22) must be multiplied with the area of the symmetry element ($L^2/2n_{bb}$).

This gives the series resistance loss in Ωcm² as

$$R_{s,m}[\Omega\mathrm{cm}^2] = \frac{L^2 \cdot \rho_{metal}}{12 \cdot {n_{bb}}^2 \cdot d_{metal}} = \frac{L^2 \cdot R_{sh}}{12 \cdot {n_{bb}}^2} = \frac{L^2 \cdot R_{bb}}{12 \cdot n_{bb}}. \tag{2.23}$$

The series resistance of the whole cell will then be

$$R_s[\Omega\mathrm{cm}^2] = R_{s1}[\Omega\mathrm{cm}^2] + R_{s,m}[\Omega\mathrm{cm}^2], \tag{2.24}$$

where R_{s1} [Ωcm²] is the series resistance of the cell without the contribution of the lateral resistance of the rear-side metallization in Ωcm².

The fill factor *FF* and the efficiency η of the cells can be written as

$$FF = FF_1 - FF_m, \tag{2.25}$$

$$\eta = \eta_1 - \eta_m, \tag{2.26}$$

where FF_1 and η_1 are the fill factor and the efficiency of the cell without the contribution of the lateral resistance of the rear-side metallization, respectively. The quantities FF_m and η_m are the fill factor loss and efficiency loss due to this contribution and they can be obtained by using equations (2.5) and (2.12). This will result in

$$FF_m = \frac{FF_0 \cdot I_{sc} \cdot R_{s,m}[\Omega\mathrm{cm}^2]}{V_{oc}}, \tag{2.27}$$

$$\eta_m = FF_0 \cdot {I_{sc}}^2 \cdot R_{s,m}[\Omega cm^2], \tag{2.28}$$

where FF_0 is the ideal fill factor given by equation (2.4). By inserting equations (2.27) and (2.28) in equation (2.23), the fill factor loss FF_m and efficiency loss η_m can be obtained as a function of either R_{sh}, R_{bb} or d_{metal}, ϱ_{metal}

$$\begin{aligned} FF_m &= \frac{FF_0 \cdot I_{sc} \cdot L^2 \cdot R_{sh}}{12 \cdot V_{oc} \cdot {n_{bb}}^2} = \frac{FF_0 \cdot I_{sc} \cdot L^2 \cdot R_{bb}}{12 \cdot V_{oc} \cdot n_{bb}} \\ &= \frac{FF_0 \cdot I_{sc} \cdot L^2 \cdot \rho_{metal}}{12 \cdot V_{oc} \cdot {n_{bb}}^2 \cdot d_{metal}} \end{aligned} \tag{2.29}$$

$$\begin{aligned} \eta_m &= \frac{FF_0 \cdot {I_{sc}}^2 \cdot L^2 \cdot R_{sh}}{12 \cdot {n_{bb}}^2} = \frac{FF_0 \cdot {I_{sc}}^2 \cdot L^2 \cdot R_{bb}}{12 \cdot n_{bb}} \\ &= \frac{FF_0 \cdot {I_{sc}}^2 \cdot L^2 \cdot \rho_{metal}}{12 \cdot {n_{bb}}^2 \cdot d_{metal}} \end{aligned} \tag{2.30}$$

Equations (2.29) and (2.30) show that the efficiency and the fill factor losses increases linearly with increasing R_{bb} or R_{sh} which is visualized in Figure 2.11. In order to keep the efficiency loss due to lateral ohmic loss in the metallization layer η_m below 0.05 $\%_{abs}$, the busbar-busbar resistance of the metallization R_{bb} must be below ~ 5 mΩ and the sheet resistance R_{sh} below ~ 15 mΩ.

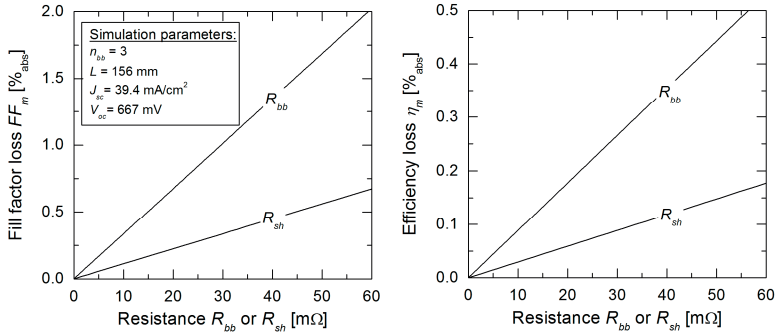

Figure 2.11: Simulated fill factor loss (left) and efficiency loss (right) as a function of busbar-busbar resistance (R_{bb}) and sheet resistance (R_{sh}) of the rear-side metallization.

In Figure 2.12, the efficiency loss η_m is plotted as a function of metallization thickness d_{metal} and resistivity ϱ_{metal} for various metals. Resistivity for bulk-materials is assumed for all metals in the simulation. The busbar-busbar-resistance values corresponding to the efficiency losses are also shown in the secondary y-axes. For all metals the same effect is observed: the efficiency loss decreases with increasing thickness and saturates at a certain thickness, which is less for higher conducting metals like Ag, Cu or Al.

Metallization-thicknesses where the efficiency loss is below 0.05 $\%_{abs}$ (or where R_{bb} or R_{sh} reaches negligible values of 5 and 15 mΩ, respectively) are listed in Table 2.1 for common used metals as Ag, Cu, Al, Ni, Cr and Ti. The results shown in Table 2.1 indicate that significantly lower metallization thickness and hence less material is needed when high conductive metals like Ag, Cu or Al are used.

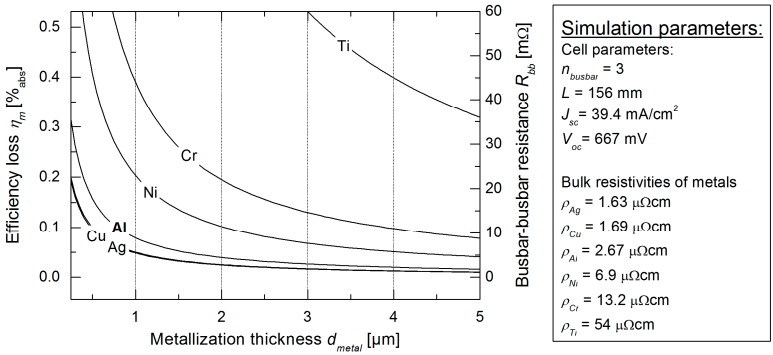

Figure 2.12: Simulated efficiency loss as a function of metal-layer-thickness (d_{metal}) and metal resistivity (ϱ_{metal}) of the rear-side metallization.

Table 2.1: Required metal-layer-thickness as a conducting layer of full-area rear-side metallization for nPERT solar cells with an efficiency loss below 0.05 %$_{abs}$.

Metal	Ag	Cu	Al	Ni	Cr	Ti
Resistivity (µΩcm)	1.63	1.69	2.67	6.9	13.2	54
Required thickness (µm) for efficiency loss η_m < 0.05 %$_{abs}$ (R_{bb} = 5 mΩ or R_{sh} = 15 mΩ)	1.09	1.13	1.78	4.6	8.8	36

2.3.2 Ohmic losses due to contact resistance of rear-side metallization

A metal-semiconductor contact with ohmic behavior is required in order to enable the majority carriers to be transferred across the contact to the metallization. Ohmic metal-semiconductor contacts are very well studied in the literature. A review of metal-semiconductor contact resistance in general as well as for solar cells is given by Schroder and Meier [33]. Depending on the doping level of the semiconductor, there are three mechanisms describing the current transport over the potential barrier of ohmic metal-semiconductor contacts Φ_B: thermionic emission, thermionic field emission and field emission (Figure 2.13). For highly doped substrates with dopant concentration greater than 10^{-19} cm^{-3} (as for the rear-side of nPERT solar cells), the potential barrier of the metal-semiconductor contact is thin enough for majority carriers to tunnel through and therefore the carriers are transported by field emission mechanism [34]. The

increased doping concentration results in a narrowing of the potential barrier which in turn means a sufficient probability of carriers tunneling through the barrier. By further increasing the doping concentration the potential barrier becomes even thinner which reduces the resistance at the metal-semiconductor junction. Thus by increasing doping concentration the specific contact resistance of metal-semiconductor contacts can be reduced [33].

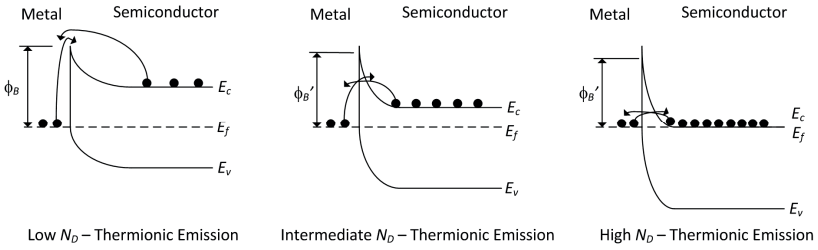

Figure 2.13: Carrier transport through or over the potential barrier of metal-semiconductor contacts. While In thermionic emission the carriers have to be transported over the potential barrier, in field emission the carriers are transported through a thinner potential barrier due to a higher doping concentration of the semiconductor. The higher doping concentration causes a reduction of the barrier height from its original value Φ_B *to* Φ_B'. *Thermionic field emission is a combination of field and thermionic emission (modified after [33]).*

In order to determine the required specific contact resistance of the rear side metallization of an nPERT solar cell for a sufficient low fill factor loss (< 0.25 $\%_{abs}$) a three-dimensional Sentaurus Device simulation [35] was carried out. The influence of the specific contact resistance on the fill factor of the cell is investigated. As in the previous section, an efficiency loss less than 0.05 $\%_{abs}$ – and thus fill factor loss < 0.25 $\%_{abs}$ – is defined as a negligible ohmic loss for a high efficiency solar cell. The cell structure used for this simulation and later experimentally is shown in Figure 2.14. The front-side emitter of the simulated device is assumed to be fully contacted in contrast to the patterned metallization grid on the front-side of a real nPERT solar cell. Therefore, an optical shading of 7% was included to the simulated device in order to obtain reasonable values of short-circuit current density of the simulated device. In addition, an external series resistance to the device is applied that includes the contact and lateral ohmic series losses of the missed front-side metallization grid in the simulated device. On the rear, point contacts with a contact radius of 20 μm and various contact spacing values were assumed. For the highly doped regions, error-

function profiles with sheet resistances about 53 Ω/sq for the emitter and 76 Ω/sq for the back-surface field (as usually used for nPERT solar cells [36]) were assumed. The thickness of the cell was set as 155 µm. The contact spacing L_p and the specific contact resistance of the rear $\rho_{c,rear}$ were varied. The resulted fill factor of the simulated device is shown in Figure 2.14.

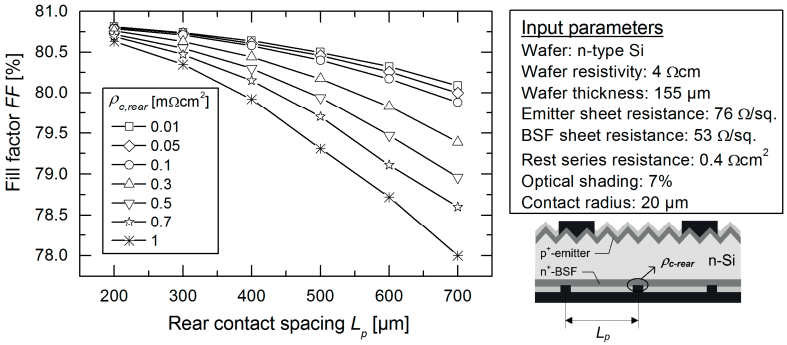

Figure 2.14: Simulated fill factor as a function of contact spacing and specific contact resistance of the rear side of an nPERT solar cell with 76 Ω/sq BSF and 20 µm contact radius. Specific contact resistance <0.3 mΩcm² is required for FF losses <0.25 %$_{abs}$. Solid lines are used as a guide to the eye.

For a contact spacing between 400 and 500 µm (or a metallization fraction area around 0.5 %) comprising ohmic and recombination losses [36], a specific contact resistance < 0.3 mΩ·cm² is required for sufficient low fill factor loss < 0.25%$_{abs}$. A detailed experimental study on the contact resistance of various rear-side metallization schemes on *n*-type silicon is investigated in Chapter 5. The impact of the contact resistance on experimentally obtained cell results is shown in Chapter 8.

2.3.3 Optical losses due to parasitic absorption in rear-side metallization

Due to the fact that silicon is an indirect band gap semiconductor, where one or more phonons are required in the absorption process of visible or infrared photons, the absorption coefficient of these photons is low. A long tail in the absorption curve out to near-infrared (NIR) wavelengths is thus characteristic for silicon (solid line in Figure 2.15 - left). Therefore, the penetration depth of

NIR-photons in silicon is high (> 10 μm) in comparison to photons in the ultraviolet (UV) energy range (dashed line in Figure 2.15 - left). UV-photons penetrate only a few nanometers into the silicon material because direct transition is possible for these high energy photons. Furthermore, the penetration depth of NIR-photons near the band gap (i.e. wavelengths between 1000 and 1100 nm) exceeds typical wafer thicknesses of 150 - 200 μm. Therefore, these low energy photons of the solar irradiation cannot contribute to current generation during their first path through the cell as schematically illustrated in Figure 2.15 - right.

As a conclusion, the rear side of the cell consisting of passivation and metallization layers must have a high internal reflectance in the NIR spectral region in order to reflect as many of these photons as possible back into the cell. These photons can pass several times through the cell and thus get more opportunities to be absorbed in the silicon wafer (Figure 2.15 - right) and contribute to current generation and hence cell performance.

In order to determine the impact of the back-side reflectance on the current generation and thus the efficiency, the short-circuit current density J_{sc} and the efficiency η of a 155-μm-thick nPERT solar cell was simulated as a function of back-side reflectance R_b using PC1D-simulation [37]. In addition, the first derivative of the resulted curves was calculated, in order to find the gain in short-circuit current density and efficiency for 1%-increase in back-side reflectance. The optical model used for the calculation of the current generation implemented in the simulation program PC1D is the Basore model [38]. The simulation results are presented in Figure 2.16.

The results in Figure 2.16 show a quasi-linear increase of short-circuit current density and efficiency in the back-side reflectance range below 50% and a progressive increase for R_b > 50%. This can be explained with the remaining percentage of light after each path through the cell: at high values of back-side reflectance, the number of passes through the cell increases progressively and is significantly higher than at low back-side reflectance values. The back-side reflectance of a silicon solar cell depends on the dielectric passivation and metallization layers used as well as on the device geometry (e.g. front-side

texturing, rear side polishing and surface roughness) [39]. Values of back-side reflectance for rear-side passivated silicon solar cells between 90 and 99 % can be found in the literature [39].

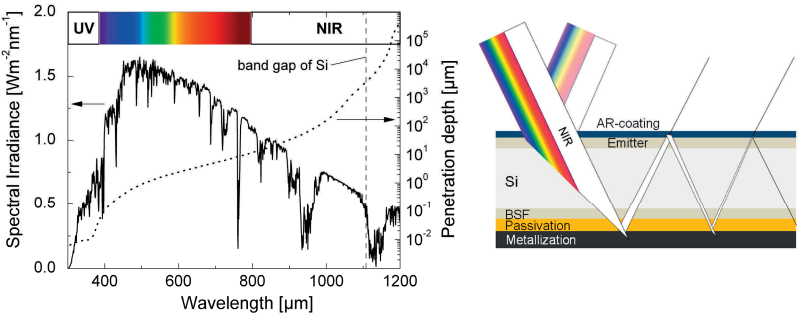

Figure 2.15: The spectral irradiation and the penetration depth in silicon against wavelength (left) and a sketch showing the penetration of solar irradiation in a silicon solar cell (right).

At a first approximation, the short-circuit current density and efficiency gain in this range of back-side reflectance is

$$\frac{\partial j_{sc}}{\partial R_b}\Big|_{89\%<R_b<100\%} = 0.070 \pm 0.007\ \mathrm{mAcm^{-2}/\%}, \tag{2.31}$$

$$\frac{\partial \eta}{\partial R_b}\Big|_{89\%<R_b<100\%} = 0.035 \pm 0.004\ \%_{abs}/\%. \tag{2.32}$$

Thus, an increase of back-side reflectance of 1 $\%_{abs}$ would result in efficiency gain of about 0.03 - 0.04 $\%_{abs}$.

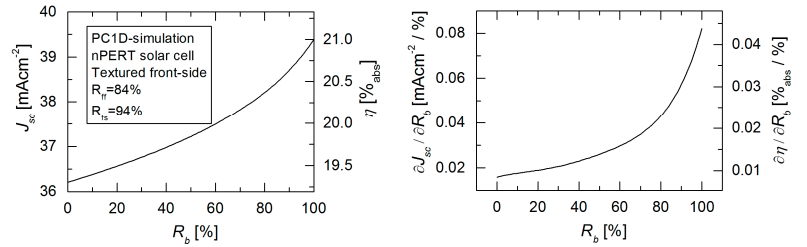

Figure 2.16: Calculated short-circuit current density (j_{sc}) and efficiency (η) as a function of back-side reflectance (R_b) for nPERT silicon solar cells with PC1D simulation program.

A detailed theoretical and experimental study of back-side reflection of various rear-side metallization schemes is presented in Chapter 6.

2.3.4 Rear-side metallization related recombination losses

Rear-side metallization can cause damage to the solar cell during either deposition or contact formation. When using plasma-enhanced deposition techniques for metallization deposition (e.g. sputtering), the underlying passivation layers can be damaged from the plasma irradiation in the deposition chamber. In this case, the passivation quality on the rear side will suffer and more carriers can recombine at the rear surface. During contact formation, impurities can diffuse to the bulk silicon and cause recombination losses there. In case of aluminum metallization, aluminum spiking can also cause damage to the solar cell during deposition or contact formation. Aluminum spiking reduces the fraction of the back surface field which in return means less field effect passivation of the rear side. Aluminum spiking is investigated in detail in Chapter 4 and plasma-induced damage in Chapter 7.

In section 2.1.4 (Figure 2.5) it was shown that J_{01} recombination losses mainly reduce V_{oc}. J_{01} takes into account recombination losses in the base or the emitter or at the surfaces. In order to show the impact of the recombination losses of the rear surface on cell performance, the open-circuit voltage und efficiency of nPERT solar cells were simulated as a function of rear surface recombination velocity S_r for two bulk-lifetime values using PC1D simulation program (Figure 2.17).

For the highly doped regions, error function doping profiles similar to the one used in the real solar cells are used. For the front-side a surface recombination velocity of 1000 cm/s is assumed. The simulation results show that V_{oc} drops from about 670 mV to less than 630 mV when surface recombination velocity of the rear-side degrades to very high values which would result in an efficiency loss of more than $1\%_{abs}$. When the bulk minority lifetime degrades from 1500 to 150 μs (e.g. through impurities from the metallization), the open circuit voltage and efficiency of the cell drops also significantly.

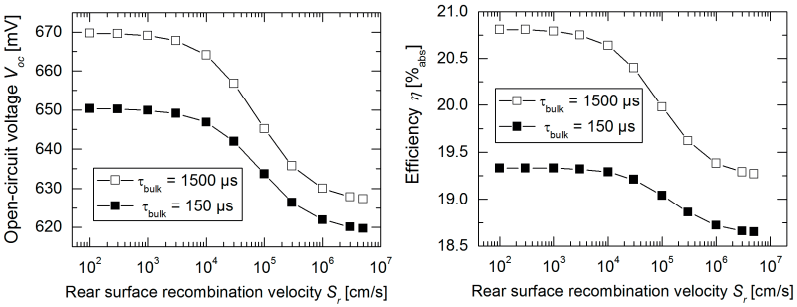

Figure 2.17: Simulated open-circuit voltage and efficiency as a function rear surface recombination velocity and bulk carrier lifetime for front-junction nPERT solar cells.

2.4 Requirements of rear-side metallization for double-side contacted industrial silicon solar cells

Various requirements of rear-side metallization for industrial silicon solar cells arise from the losses discussed in the previous section.

Rear side metallization for industrial silicon solar cells

a. must be first of all **cost effective** in order to be applicable in industrial environment;

b. must be **conductive** enough in order to transport the collected current to the busbars or connectors with only negligible ohmic losses;

c. must form **sufficiently low metal-semiconductor contact resistance** to collect the generated current from the wafer with negligible ohmic loss;

d. must **not allow any serious damage** to the **silicon wafer during contact formation**;

e. must operate as a **high IR-reflector** (in combination with the underlying passivation), in order to enhance the optical path length within the absorber and thus increase the current-generation in the cell;

f. must **not cause any serious damage** to the underlying **passivation layers**;

g. must guarantee a **mechanically and thermally stable connection to the ribbons** (connectors) in order to interconnect the cells for the module fabrication.

Material cost is a very important criterion for the determination of the materials used in the rear-side metallization. The performance requirement with the most material demand is the efficient current transport to the connectors with negligible ohmic loss (requirement b). Ideally, the rear-side metallization consists of only one layer which is conductive enough, cost effective and fulfills all the other performance requirements as well. However, in order to address contacting or capping issues additional thin layers may be required. Therefore, the main layer of the metallization (in case of multi-layer metallization) is referred to thickest layer in the stack which is responsible for efficient current transport with negligible ohmic losses. The rear-side metallization will be based on this layer and the term "based" is used: e.g. Al-based, Ag-based or Cu-based rear-side metallization.

In the following section the determination of the main conducting layer is discussed considering cost and lateral conduction issues (requirement a and b). After defining the main conducting layer, the contact formation process is studied in detail in the Chapter 4 and 5 (requirements c and d). Detailed simulations and experiments studying the impact of the optical properties of rear-side passivation and metallization on cell performance is discussed in Chapter 6 (requirement e). In Chapter 7, plasma-induced damage during sputtering deposition of metal layers is investigated on various passivation layers (requirement f).

2.5 Why aluminum-based PVD rear-side metallization for *n*-type PERT solar cells?

In order to show that aluminum is the ideal material for the main conducting layer of the rear-side full-area metallization for silicon solar cells, cost calculations are performed. Since the electrical conductance is material and thickness dependent (section 2.3.1), cost calculations are done for various metals and thicknesses. The material cost is calculated for the required thickness of

each metal for sufficient current transport. Based on these results, aluminum as a main conducting layer of the rear-side metallization developed in this thesis is defined.

Material cost analysis for full-area conducting metallization layer

In section 2.3.1, it was shown that by using high conductive metals as Ag, Cu or Al, a significant lower layer thickness is needed for sufficient current transport with only negligible efficiency loss than less conductive metals as Ni, Ti or Cr. For industrial solar cells not only cell efficiency but cost is a very essential criterion as well. Therefore, material cost was calculated for Ag, Cu, Al, Ni, Cr and Ti as a conducting metallization layer, in order to evaluate the ideal conducting metal for the rear-side metallization of the cell.

For the calculation of the material cost, one year average of LME[1] metal prices (between February 2013 and March 2014) was taken into account. In addition, no other costs as utilization, recycling, waste, target production etc. were considered. Utilization and recycling depends strongly on the material and metallization technology used. Targets utilization of planar magnetron sputtering, for an example, is usually between 30 and 50 % and targets utilization of rotatable cylindrical magnetron sputtering can reach 90 %. For a detailed cost calculation all other costs have to be taken into account. Nevertheless, pure material cost is a valid criterion for the evaluation of the conducting layer of the rear-side metallization.

The material cost of the metallization layer per wafer (*MC*) can be written as

$$MC = D_{metal} \cdot d_{metal} \cdot A_{cell} \cdot P_{metal}, \tag{2.33}$$

where D_{metal} is the volumetric mass density and d_{metal} is the thickness of the metallization layer, A_{cell} is the cell area and P_{metal} is the metal price.

Figure 2.18 shows the material cost for Ag, Cu, Al, Ni, Cr and Ti as a conducting metallization layer for pseudo-square wafer-sized solar cells with a side length

[1] LME: London Metal Exchange (http://www.lme.com).

of 15,6 cm (A_{cell} = 241 cm²). The thicknesses shown in Table 2.1 (required for efficiency loss < 0.05 $\%_{abs}$) were taken into account for the calculation of the material cost data in Figure 2.18.

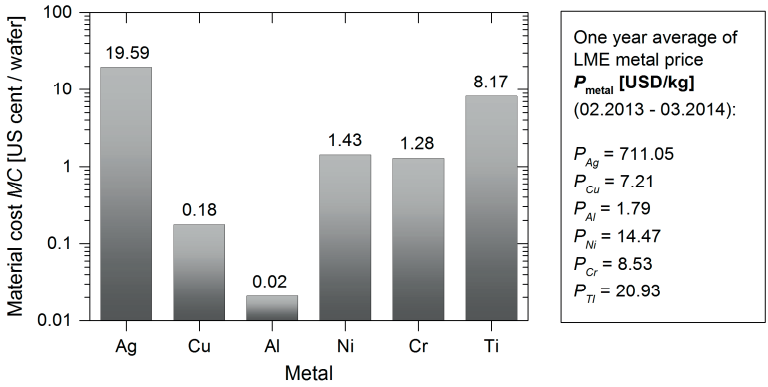

Figure 2.18: Comparison of material cost for the various metals as a conducting layer of full-area rear-side metallization for silicon solar cells.

The results show clearly that Al is the most attractive material to be applied as the main conducting layer of the rear-side metallization. It compromises functionality and material cost very well in contrast to very high conducting Ag, which cannot be implemented industrially due to its very high material cost. Other less conducting materials as Ni or Cr still has too high material cost (> 1 US-cent/wafer) to be implementable for industrial production as a full-area metallization. In addition, they require much thicker layers which can also cause mechanical problems (e.g. bow) for full-area metallization applications.

The only other material apart from Al which is also attractive for full-area rear-side metallization is Cu. The material cost of Cu is still about nine times higher than Al but has other advantages which can be worthy. Due to the lower resistivity of Cu and thus the less required layer thickness, more throughput can be reached (depending on the deposition rate). A higher throughput during production can also spare production costs. Furthermore, Cu is easily solderable in contrast to Al which can also be beneficial when it comes to interconnecting the cells for module fabrication. In the case of Al-metallization, capping layers

are needed in order to solder Al surfaces by conversional soldering technique which means additional cost and process complications [28]. Finally, unlike Al, Cu can be plated which can be very beneficial when structured thick metallization is required, as for e.g. for back-contact back-junction solar cells. However, Cu still has a major setback being a very damaging impurity in silicon material [40]. Cu as a deep level impurity is a very active recombination center in silicon and very mobile as well (even at room temperatures). Therefore, Cu causes major damage to silicon solar cells when diffusing into the active silicon material of the cell. This means that Cu cannot be applied directly to the silicon wafer. Therefore, diffusion barriers between Cu and Si are needed to suppress Cu diffusion into Si. The requirement of diffusion barriers means in turn more cost and process complication. A lot of work regarding Cu-based metallization for silicon solar cells was carried out in recent years in order to replace the cost-intensive Ag-based screen-printing metallization mainly for the front-side of the cell [41-43]. Given the facts as described and on the basis of specific stakeholder decisions by Bosch Solar Energy, this thesis focuses on Al-based full-area metallization for the rear-side of nPERT solar cells. The main conducting layer is thus a 2-µm-thick PVD-Al.

3 Sputtering deposition processes of the investigated metal layers

Based on lateral conductance simulations and cost calculations, an aluminum-based metallization was defined as a rear-side metallization to be developed for nPERT solar cells (section 2.5). This means that the main conducting layer in the metallization to be developed is a sputtered aluminum layer with thicknesses varying from about 0.5 to 2 µm. Various other thin layers were also investigated in this thesis as contacting, diffusion barriers or capping layers. These metals were aluminum enriched silicon (Al-Si), silver (Ag) and titanium (Ti). Therefore, the process chambers of the sputtering deposition system used in this thesis (Oerlikon SOLARIS 6 multi-layer sputtering deposition system) were provided with the following sputtering targets: Al, Al-Si (1 at% Si), Ag and Ti.

In this chapter, a brief description of the SOLARIS 6 multi-layer sputtering deposition system is first carried out. Afterwards, the process parameters and the deposition rates of each of the investigated metals are described. In addition, the substrate temperature during sputtering deposition of the thick aluminum layer at various sputtering powers is investigated, since an in-situ dynamic contact-formation annealing can occur which can spare the standard ex-situ contact formation at 400 °C.

3.1 Oerlikon SOLARIS 6 multi-layer sputtering deposition system

Oerlikon SOLARIS 6 multi-layer sputtering deposition system is a single-substrate multi-chamber sputtering system which uses planar magnetron technology. Figure 3.1 shows the main components of the SOLARIS 6:

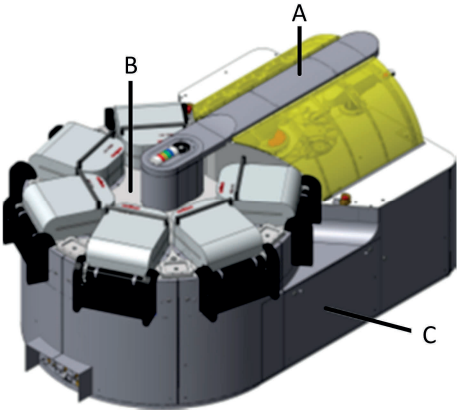

Figure 3.1: Single-wafer SOLARIS 6 multi-layer sputtering system used for depositing the PVD metals investigated in this thesis and for fabricating the rear-side metallization of the front-junction nPERT solar cells [9].

- **Transport system at atmosphere side (A)**. The transport system at atmosphere side transports substrates back and forth between the production line and the processing unit. The transport system is guarded by a load lock cover with interlocked access.

- **Processing unit (B)**. The processing unit consists of a vacuum chamber which contains load lock chamber, main chamber (MC) turntable as well as six process chambers (PC). The sputtering sources (include targets) in each PC are mounted on top and the substrate carriers on down. The substrate and the sputtering sources are horizontal. Planar magnetron sputtering sources are used for the coating processes which are fitted with a rotating magnet system. The rotating magnets ensure erosion of the entire target surface. Other advantages of this technology are higher target utilization and the elimination of re-deposition zones on the target. The sputtering source can be opened with a handle and a source handler. The planar magnetron is particularly maintenance-friendly. The spatial separation of the cooling circuit and the target allows target change to be performed with the cover open within a few minutes. The rotating MC turntable moves the substrate from the load lock chamber to a position below the first process chamber. A lifting device raises the substrate

into the process chamber for coating. When the coating process is completed, the substrate is moved from the MC turntable into the next process chamber. The substrate is returned to the load lock chamber after it has passed through all the process chambers. The load lock is vented and the atmospheric transport unit removes the substrate from the load lock chamber.

- **Underbody with components (C)**. The electrical boxes, fore-pumps and components for the media supply are located in the system underbody. The components are behind casing which is easy to remove.

3.2 Sputtering-deposition processes of the metal layers

The metal layers were deposited using pulsed DC sputtering processes. The layers were either deposited in one step or in a number of executed process cycles which are described as "*shots*". Thus, in each deposition process the number of shots as well as the sputtering time of each shot is given. The process gas used in all processes was argon (Ar) with a gas flow rate of 30 sccm. The range of the sputtering power applied during sputtering deposition of the various metal layers was 1 - 14 kW. The metal layer thicknesses (d_{metal}) were determined by measuring the weight of monitoring wafers (m_{wafer}) before and after deposition using equation (3.1)

$$d_{metal} = \frac{\Delta m_{wafer}}{A_{wafer} \cdot D_{metal}}. \tag{3.1}$$

Here, A_{wafer} is the area of the wafer (A_{wafer} = 241 cm^2 for pseudo-square wafer with a side length of 15.6 cm) and D_{metal} is the volumetric density of the metal layer. The sheet resistance of the conducting aluminum layers was also measured in order to determine the resistivity of the deposited aluminum layers (7 × 7 points mapping), since aluminum is the current main transporting layer.

3.2.1 Process parameters and deposition rate of aluminum sputtering deposition

Since aluminum is the thickest layer in an aluminum-based metallization, the aluminum layer was deposited at the highest possible sputtering power to insure the highest deposition rate. Therefore, a maximum sputtering power of 14 kW was used for the deposition of the various aluminum layers. In the previous chapter it was found by simulations that at least 2-µm-thick aluminum layer is needed for sufficient current transport with negligible ohmic loss. The sputtering process parameters used for the deposition of about 2.1 µm aluminum is shown in Table 3.1 along with sputtering processes for a half and a third of this thickness by scaling the sputtering time. The resulted layer thicknesses by measuring the weight difference of the monitoring wafers before and after deposition are also shown in Table 3.1 and in Figure 3.2. A volumetric mass density of 2.7 g/cm^3 [44] was assumed for the thickness calculation with equation (3.1).

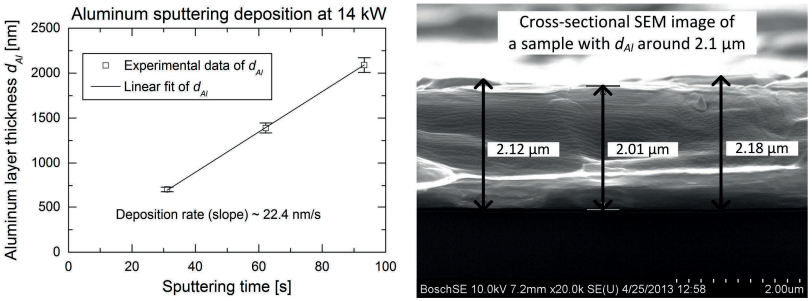

Figure 3.2: Deposition rate of aluminum sputtering deposition with SOLARIS 6 at 14 kW.

The obtained resistivity of the various aluminum sputtered films was around 3 µΩcm which is in a very good correlation with literature values of evaporated or sputtered aluminum films [45]. Furthermore, a linear dependence of layer thickness with sputtering time was observed. The deposition rate at 14 kW was found to be about 22.4 nm/s. In section 3.2.5 the maximum substrate temperature during aluminum sputtering is determined.

Table 3.1: Process parameter for aluminum sputtering deposition.

Process number	1	2	3
Shots	1 x 12 shots	2 x 12 shots	3 x 12 shots
Sputtering time per shot (s)	2.59	2.59	2.59
Sputtering time (s)	31.1	62.2	93.24
Weight difference (mg)	46.7	89.8	135.6
Layer thickness d_{Al} based on weight difference (µm)	0.71	1.39	2.09
Sheet resistance R_{sh} (mΩ)	42.43 ± 1.56	21.00 ± 0.72	14.03 ± 0.47
Non-uniformity of R_{sh} (%)	5.20 ± 0.14	4.71 ± 0.11	4.66 ± 0.20
Resistivity µΩcm ($\rho_{Al} = R_{sh}\, d_{Al}$)	2.99	2.92	2.93
Sputtering power (kW)	14		
Target material	Al		
Process gas	Ar		
Process gas flow rate (sccm)	30		

3.2.2 Sputtering-deposition processes of the Al-Si (1 at% Si) layers

Silicon-enriched aluminum metallization is known to prevent a phenomenon known as aluminum spiking which is described and investigated in detail in Chapter 4. Therefore, a silicon-enriched aluminum target with 1 at% silicon, Al-Si (1 at% Si), was installed to the SOLARIS 6 system in process chamber 2. The main aim of the Al-Si investigations was to study the potential of Al-Si/Al stack instead of the state of the art one-layer Al-Si metallization to prevent aluminum spiking. Therefore, various Al-Si/Al stacks with varying Al-Si layer thicknesses were investigated. The Al-Si layers were deposited at a sputtering

power of 10 kW with the parameters shown in Table 3.2. A volumetric mass density of 2.696 g/cm³ [46] was assumed for the thickness calculation with equation (3.1). The sputtering process parameters used for the deposition of the various Al-Si layers and the resulted layer thicknesses are shown in Table 3.2. Figure 3.3 shows the fitted deposition rate obtained from the layer thicknesses.

Table 3.2: Process parameter for Al-Si sputtering deposition. The thicknesses of the Al-Si layers of process 4 and 5 (60 and 120 nm respectively) were estimated on the basis of the deposition rate.

Process number	4	5	6	7	8	9
Process shots	1	2	4	7	10	3 x 12
Sputtering time per shot (s)	4	4	4	4	4	4
Sputtering time (s)	4	8	16	28	40	144
Weight difference (mg)	---	---	15.5 ± 1.2	26.9 ± 1.6	39.4 ± 2.4	141.3 ± 9.9
Layer thickness based on weight difference (nm)	60	120	239 ± 19	414 ± 26	606 ± 37	2174 ± 153
Sputtering power (kW)	10					
Target material	Al-Si (1 at% Si)					
Process gas	Ar					
Process gas flow rate (sccm)	30					

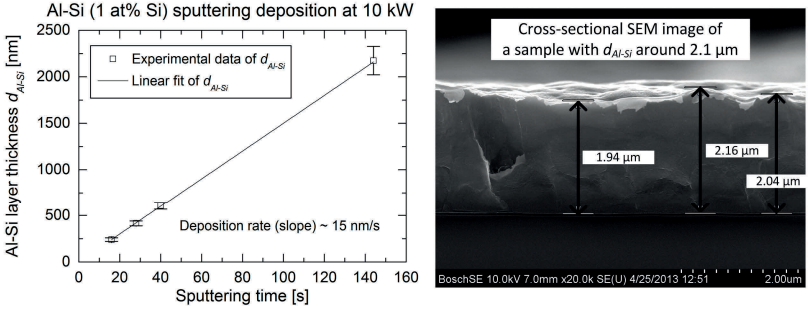

Figure 3.3: Deposition rate of Al-Si sputtering deposition with SOLARIS 6 at 10 kW.

3.2.3 Sputtering deposition processes of the silver layers

In section 2.3.3 it was shown that the transmitted light hits the rear surface in the near infrared spectral range and bounces back into the cell to further generate current in the cell. Thus, a high reflecting metal in this spectral range like silver can enhance the internal reflection on the rear surface compared to other metals. This is studied in detail in Chapter 6 where various rear-side reflectors were investigated. The optical performance of the high reflecting PVD-Ag is compared with other PVD metals. Furthermore, a multi-layer stack with thin silver (< 100 nm) as a contacting high reflecting layer was investigated. Therefore, a silver target was installed in chamber 6 of the SOLARIS 6 machine.

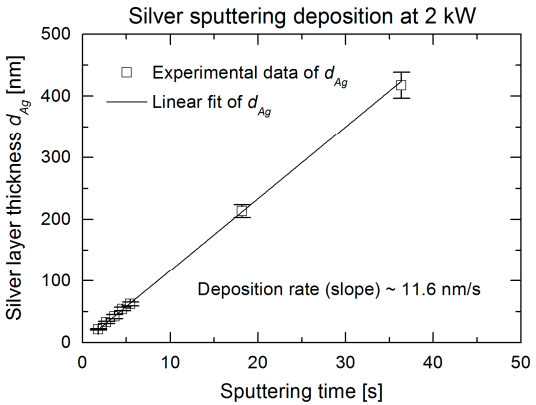

Figure 3.4: Deposition rate of Ag sputtering deposition with SOLARIS 6 at 2 kW.

Since mainly thin silver layers were used, the various silver layers were deposited at low sputtering power in order to better control the layer thicknesses. A volumetric mass density of 10.49 g/cm³ [44] was assumed for the thickness calculation with equation (3.1). The sputtering process parameters used for the deposition of the various silver layers and the resulted layer thicknesses are shown in Table 3.3. Figure 3.4 shows the fitted deposition rate of silver sputtering obtained from the layer thicknesses.

Table 3.3: Process parameter for silver sputtering deposition. The thickness of the silver layer of process 10 (10 nm) was estimated on the basis of the deposition rate.

Process number	10	11	12	13	14	15	16	17
Process shots	1	1	1	1	1	1	5	10
Sputtering time per shot (s)	1.82	1.82	2.73	3.64	4.55	5.45	3.64	3.64
Sputtering time (s)	1.82	1.82	2.73	3.64	4.55	5.45	18.18	36.36
Weight difference (mg)	---	5.3 ± 0.3	8.2 ± 0.7	10.6 ± 0.8	13.7 ± 1.2	15.7 ± 1.1	53.9 ± 4.9	105.5 ± 6.3
Layer thickness (nm)	10	21.1 ± 1.1	32.5 ± 1.6	41.9 ± 3.4	54.2 ± 2.7	62.2 ± 3.1	213 ± 11	418 ± 21
Sputtering power (kW)	1	2						
Target material	Ag							
Process gas	Ar							
Process gas flow rate (sccm)	30							

3.2.4 Sputtering deposition processes of the titanium layers

Titanium is one of the most used contacting metals in silicon technology due to its superior contacting properties as very low contact resistance to silicon and high adhesion. Furthermore, it can be used as a diffusion and spiking barrier. Therefore, titanium was investigated in this work in various aspects. The titanium layers were deposited in chamber 3 of the SOLARIS 6 machine at low power, since mainly thin titanium layers were investigated. A volumetric mass density of 4.5 g/cm^3 [44] was assumed for the thickness calculation with equation (3.1). The sputtering process parameters used for the deposition of the

various titanium layers and the resulted layer thicknesses are shown in Table 3.4. Figure 3.5 shows the fitted deposition rate of Ti sputtering.

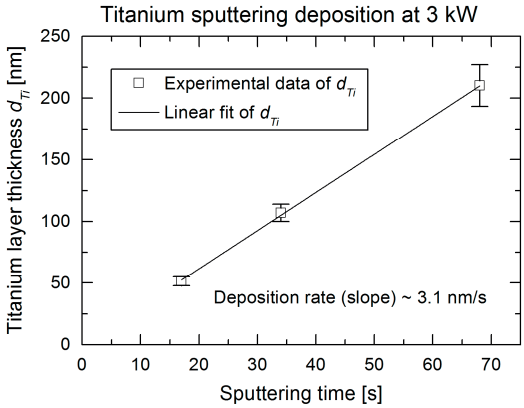

Figure 3.5: Deposition rate of Ti sputtering deposition with SOLARIS 6 at 3 kW.

3.2.5 Maximum substrate temperature during aluminum sputtering deposition

Substrate temperature during metal sputtering deposition is an important process information, since it can affect the contact formation with the silicon wafer in the contact openings or influence the passivation quality in the passivated regions. Substrate heating during sputtering depends on several factors, e. g. the kinetic energy of the sputtered atoms, heat of condensation, plasma radiation and the kinetic energy of ions and electrons at the substrate. Furthermore, it can be determined by external factors within the sputtering system such as sputtering power, geometry, and pressure of the background gas. Ekpe and Dew [47] reported that steady state thermal flux to the substrate increases linearly with increasing magnetron power during sputtering.

Due to the single-wafer design of the SOLARIS 6 and its transportation system, it is nearly impossible to determine the temperature during sputtering by mounting a thermocouple or similar temperature sensors. Therefore, the maximum temperature during sputtering was determined by using temperature indicating sticks Tempilstick® from the company Tempil®.

Table 3.4: Process parameter for titanium sputtering deposition. The thickness of the titanium layers of processes 18, 19 and 20 (3, 10 and 20 nm, respectively) were estimated on the basis of the deposition rate

Process number	18	19	20	21	22	23
Process shots	1	1	1	1	1	1
Sputtering time per shot (s)	1.82	1.82	2.73	3.64	4.55	5.45
Sputtering time (s)	1.82	1.82	2.73	3.64	4.55	5.45
Weight difference (mg)	---	---	---	5.6 ± 0.4	11.6 ± 0.8	22.8 ± 1.8
Layer thickness based on weight difference (nm)	3	10	20	51.4 ± 3.6	106.8 ± 6.9	210.2 ± 16.8
Sputtering power (kW)	1	3				
Target material	Ti					
Process gas	Ar					
Process gas flow rate (sccm)	30					

Tempilsticks are indicting crayons for a range of temperatures that will record the highest bracketed temperature reached by the Tempilstick. The temperature range covered by Tempilsticks is 38 - 1093 °C. The Tempilsticks used in this work were with these melting temperatures: 149, 177, 204, 232, 260, 288, 316, 343, 378, 390 and 427 °C. Tempilstick makes a mark by melting at the point of contact once the surface reaches the specific temperature of the Tempilstick. In order to verify which maximal temperature is reached during sputtering deposition the Tempilstick is stroked on the non-deposited side of the wafer. The wafer is then placed on another dummy wafer (i.e. the stroked crayon is sandwiched between the two wafers) in order to prevent the crayon spreading in the process chamber during deposition. If the crayon is completely melted after deposition, then the specific temperature of the Tempilstick is reached.

The wafer-sandwich method with Tempilstick was first tested on a calibrated hotplate before using it in the deposition chamber with satisfying results. It is worth mentioning that if the crayon is not completely melted (i.e. it can still be smeared, even if it leaves an imprint), then the temperature is not reached yet; this leads to a decrease in precision of the temperature determination.

The maximal temperature during sputtering deposition T_{max} was tested for ~ 0.7 μm aluminum layer deposited at various sputtering powers and also for ~ 1.4 and ~ 2.1 μm aluminum layer sputtered at 14 kW. For the aluminum layers which are deposited at 14 kW, the same parameters were used as in Table 3.1. For the deposition of the 0.7 μm aluminum layers at different sputtering powers, the layers are also sputtered after linearly scaling the sputtering time per shot. The results are shown in Table 3.5. The maximal temperature during deposition T_{max} is given in a range. The lower limit of this range is the temperature at which the last Tempilstick crayon is melted and the upper limit is the next level Tempilstick at which the Tempilstick crayon is not melted. The result shows that by sputtering deposition at higher power the substrate reaches significantly higher temperatures. The maximal substrate temperature during sputtering deposition (T_{max}) of ~ 0.7 nm aluminum layer at 2 kW is in the range between 232 and 260 °C whereas at 14 kW T_{max} is between 316 and 343 °C. Furthermore, T_{max} for thicker aluminum layers (1.4 and 2.1 μm) reaches contact-formation annealing temperatures around 400 °C which may result in an in-situ contact-formation. This will be tested in Chapter 5.

Table 3.5: Maximal temperature during sputtering deposition of various aluminum layers.

Process nr.	4	5	6	7	8	9	10
$P_{sputter}$ (kW)	2	7	10	12	14	14	14
d_{Al} (μm)	0.7	0.7	0.7	0.7	0.7	1.4	2.1
T_{max} range °C	232 - 260	260 - 288	288 - 316	288 - 316	316 - 343	371 - 390	390 - 427

3.3 Summary and conclusion

In this chapter, the various sputtering processes for the investigated metals in this thesis are described. Furthermore, the maximal temperature during sputtering deposition of the conducting aluminum layers were determined by using temperature indicating sticks Tempilstick®. It was found that substrate temperatures in the region of contact-formation annealing temperature of aluminum metallization (400 °C) are reached during sputtering deposition of aluminum at high power (14 kW). In the following chapters the electrical and optical properties of the investigated metals and their impact on cell performance are investigated.

4 Contact formation process of aluminum-based metallization

In Chapter 2 (section 2.5), an aluminum layer of 2 μm layer thickness was defined as the main conducting layer of the rear-side metallization for nPERT silicon solar cells. Apart from the conduction requirement, a solar cell metallization must also form an ohmic metal-semiconductor contact with a sufficiently low contact resistance without any damage to the wafer during contact formation. Aluminum is known to form low-resistance contacts to n^+- as well as *p*-doped silicon [33]. However, it can also cause damage to the underlying silicon by aluminum spiking [48].

In this chapter, process simulations and scanning electron microscopy (SEM) structural investigations on the contact formation process and the spiking phenomenon between aluminum and silicon are carried out. Furthermore, solutions to prevent aluminum spiking are studied, presented and discussed. The impact of aluminum spiking and spiking barriers on the cell performance of nPERT solar cells will be presented at the end of this thesis in Chapter 8. The results of this chapter are published in [49].

4.1 Theoretical background on the contact-formation process of Al/Si-contacts

Rear contacts of a rear-side passivated silicon solar cell are usually opened by laser ablation or by etching processes (e.g. plasma etching or chemical etching) prior to the metallization process. After the contact opening process a very thin native oxide layer of some nanometers grows on the silicon surface where the growth rate depends on several factors such as room temperature, dopant species and level, cleanliness of the wafer surface and room air properties (e.g. cleanliness, humidity) [50]. Figure 4.1 shows exemplary the growth rate of native silicon oxide on *p*-type silicon in air at room temperature after HF etching (data taken from [51]).

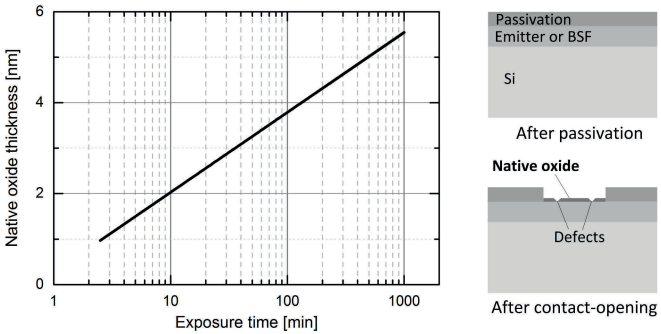

Figure 4.1: Growth rate of native oxide on silicon in air at room temperature after HF etching (data taken from [51]).

The native oxide in the contact openings prevents a direct contact between the metallization and the silicon wafer. In order to ensure that the contacting metal is in a good physical contact to silicon, a thermal process is required to reduce the native silicon oxide formed in the contact openings – sometimes with a pre-cleaning step directly before metal deposition. The thermal annealing process can be done either during deposition (*in-situ* annealing) or after deposition (*ex-situ* annealing). In some cases the annealing process can also be useful to reduce interface traps in the passivated regions of the cell as well as under the contacts and thus improve the passivation quality of the cell [52]. For aluminum metallization, temperatures around 400 °C are usually applied to reduce the native oxide in the contact openings and ensure a good physical contact of aluminum to the underlying silicon [53].

In order to understand interface reactions between aluminum and silicon at these temperatures, the phase diagram of aluminum-silicon binary system, the diffusivities of these elements in each other as well as their self-diffusivities are required.

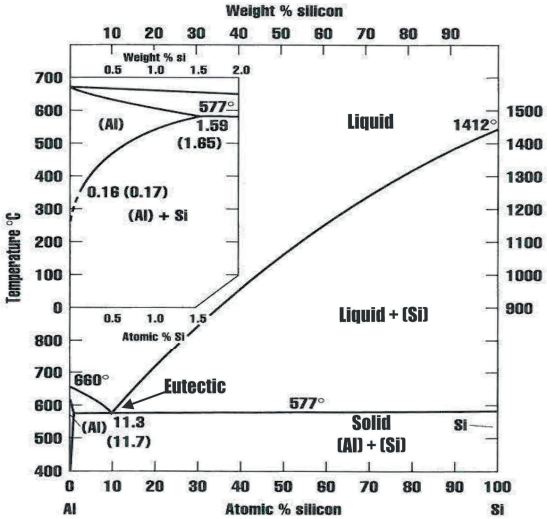

Figure 4.2: Aluminum-Silicon phase diagram (taken from [48]).

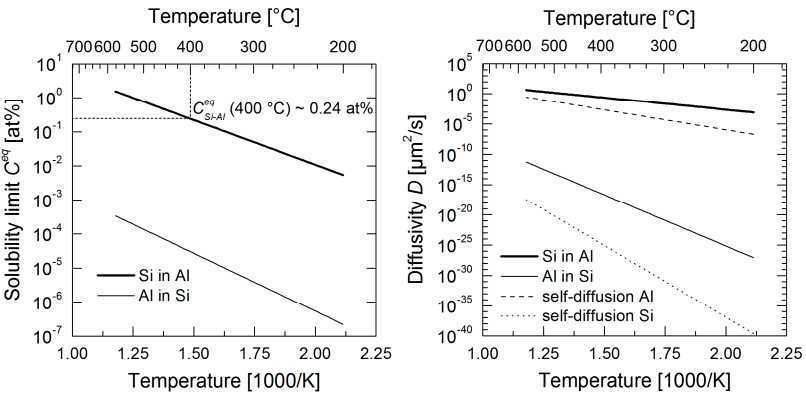

Figure 4.3: Solubility limit of Si and Al and vice versa (left-hand side) and the diffusivity of Si and Al in each other and their self-diffusivities (right-hand side). Although Al is the fastest diffusing acceptor element in Si [54], its diffusivity and solubility limit in Si at 400 °C is negligibly low compared to those of Si in Al. Diffusivity data of Si in evaporated Al are taken from [55] and diffusivity data of Al in Si from [56]. The self-diffusion data of Al are taken from [57] and the self-diffusion data of Si from [54]. The data of the solubility limit of both elements in each other are taken from [58].

Figure 4.2 shows the phase diagram of aluminum-silicon binary system. The aluminum-silicon system is a simple eutectic system with two solid solution

phases and an eutectic temperature at around 577 °C. This eutectic temperature is higher than the contact-formation annealing temperature at 400 °C and thus no solid alloy will be formed during contact-formation annealing. However, silicon is well soluble and diffuses in aluminum at 400 °C with a solubility limit of 0.24 at% (Figure 4.3, left) and a diffusivity of 0.26 $\mu m^2/s$ in evaporated aluminum (Figure 4.3, right). The solubility limit and diffusivity of aluminum in silicon at these temperatures compared to those of silicon in aluminum are negligibly low (Figure 4.3).The high solubility limit and diffusivity of silicon in aluminum causes dissolution of silicon from the wafer into the aluminum layer during contact-formation annealing. The dissolution of silicon from the wafer into the aluminum layer creates voids in the silicon wafer that are quickly filled by the overlying aluminum due to the much higher self-diffusion of aluminum than the self-diffusion of silicon. Since the native oxide growth and the reduction of the native oxide by aluminum is not uniform, aluminum will penetrate locally in silicon. The silicon will be anisotropically consumed causing aluminum spikes in the underlying silicon wafer. This phenomenon is referred as aluminum spiking and illustrated schematically in Figure 4.4.

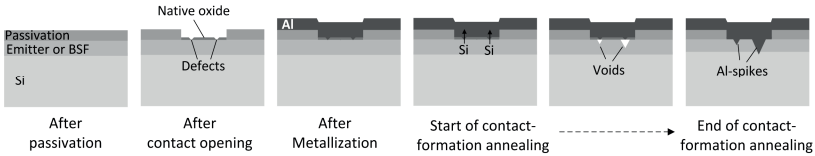

Figure 4.4: A sketch illustrating the aluminum spiking phenomenon in silicon.

Figure 4.5 shows SEM images of a typical spiking on a silicon wafer sputtered with an aluminum layer before (left) and after (right) back-etching the aluminum layer. Since the solubility limit of silicon in aluminum increases with increasing temperature (Figure 4.3, left), more silicon will move from the wafer into the aluminum layer at higher temperatures. Thus, aluminum spikes can penetrate deeper with increasing thermal stress. Deep penetrating spikes can cause major damage to the cell, e.g. shunt the *p-n* junction (Figure 4.6, right). In the case of a high–low junction (e.g. n^+-*n* junction as for nPERT solar cells with front-side emitter where no shunting can occur), deep penetrating spikes can reduce the area fraction of the highly doped region. In this case, the contacts are no longer

well passivated, and the passivation quality of the cell can degrade. The degradation of the passivation quality results in a reduction of the open-circuit voltage and hence the performance of the solar cell as shown in section 2.3.4.

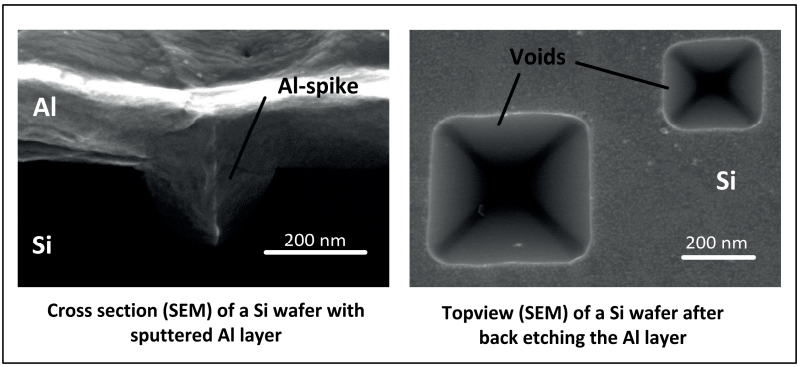

Figure 4.5: SEM images of a typical spiking on a silicon wafer sputtered with an aluminum layer before (left) and after (right) back-etching the aluminum layer.

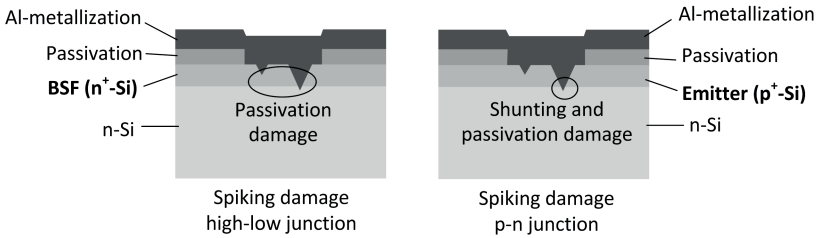

Figure 4.6: Spiking damages of a high-low junction (left) and a p-n junction (right) of silicon solar cells.

In order to protect the device from the damage caused by aluminum spiking several approaches can be used:

a. **Optimization the contact-formation annealing process between sufficient low-resistance contact and undamaging spikes**. Since the solubility limit of silicon in aluminum increases with increasing temperature, a contact formation annealing at lower temperatures will result in a less spiking penetration depth. However, this approach might be at the expense of other power losses, e.g. contact resistance losses.

b. **Optimization the doped regions by using doping profiles deeper than the spikes can penetrate**. This approach can also be at the expense of other power losses like contact resistance losses, since deeper profiles usually have less dopant surface concentration which in turn can result in a higher contact resistance. The impact of the contact-formation annealing process and the doping level on the stability of the cell against aluminum spiking will be investigated directly on nPERT solar cells in Chapter 8.

c. **The use of conductive diffusion barriers like titanium or vanadium between aluminum and silicon**. A diffusion barrier can prevent silicon from diffusing into the aluminum layer and aluminum spiking can be suppressed [59]. Diffusion barriers like titanium can be beneficial regarding the reduction of the native oxide or the contact resistance and are thus widely used in microelectronics. In this work the use of titanium as a spiking barrier in aluminum-based metallization on the rear-side of nPERT solar cells is investigated. To the knowledge of the author, this approach (Ti/Al stack) has not been tested previously as a rear-side metallization of silicon solar cells.

d. **The use of silicon-enriched aluminum metallization (Al-Si alloys)**. Aluminum metallization alloyed with 0.5 - 2 at% silicon fulfills the solubility requirement of silicon in aluminum and thus no silicon from the wafer will diffuse into the aluminum layer. Al-Si alloys can suppress spikes formation, however, undesired precipitation of *p*-doped silicon at the boundaries between silicon and aluminum can occur during cooling down if the atomic concentration of silicon in the aluminum layer is higher than the solubility requirement at a given annealing temperature. In this case an increase in contact resistance for contacting n^+-doped silicon may occur, since the silicon precipitates are *p*-doped. Single layer Al-Si metallization to overcome spike formation is also investigated in this work.

e. **The novel approach Al-Si/Al stack instead of one-layer Al-Si or aluminum metallization**. The idea of using Al-Si/Al stack instead of

single layer Al or Al-Si metallization is to tune the thickness of the Al-Si layer to the thickness at which the solubility limit is exactly reached at a given annealing temperature. In other words, the aim to find the Al-Si thickness at which both spiking and precipitation formation are suppressed. This approach is investigated in detail by process simulations and experiments in this work and compared to pure Al and Al-Si metallization as well as to Ti/Al-stack.

4.2 Characterization of contact formation process

The test samples for the experimental investigations on spikes and precipitates formation were fabricated featuring the rear side structure of nPERT solar cells. For these samples, *n*-type Cz silicon wafers with highly doped n^+ damage-etched surface passivated with plasma enhanced chemical vapor deposited (PECVD) SiN_x were used. On the rear-side of the test samples point contacts of about 20 µm contact radius were realized by laser ablation and afterwards the investigated metallization variations (Al, Al-Si, Al-Si/Al and Ti/Al stacks) were sputtered. The aluminum layer thickness was about 2.1 µm thick for all investigated samples (process 3 of Table 3.1). The layer thicknesses of the contacting metal layers (Ti or Al-Si with 1 at% Si) are described in the following sections. A contact-formation annealing step in a tube furnace at 400 °C for 5 min in N_2-ambient was afterwards applied to the test samples. After the annealing process, the samples were first dipped in phosphoric acid to etch back the aluminum layer and then in hydrofluoric acid to ensure that the titanium layer is also removed for the samples with Ti/Al metallization. The etched surface of the samples was then studied with secondary electron microscopy (SEM) as shown in Figure 4.7.

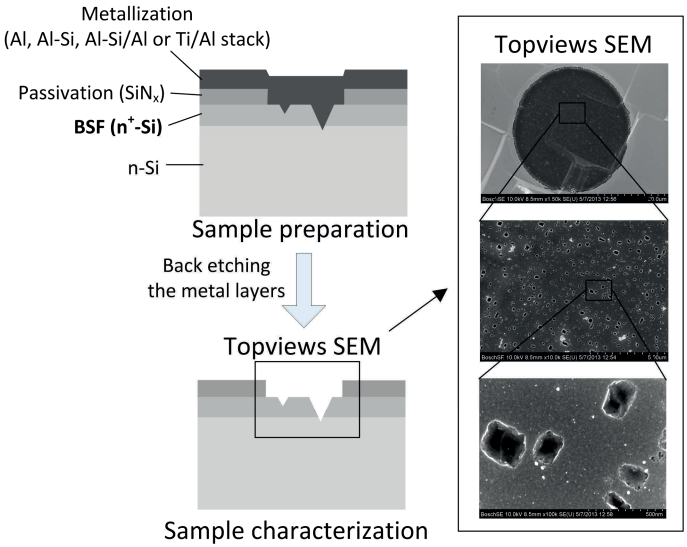

Figure 4.7: Preparation and characterization of the spiking samples.

4.3 Ti/Al stack against aluminum spiking

In this section the use of a thin titanium layer as a spiking barrier between aluminum and silicon to suppress aluminum spiking at a given thermal stress is investigated.

4.3.1 Theoretical background of titanium as a spiking barrier

Spiking barriers must prevent metallurgical reactions as well as diffusion between silicon and aluminum at processing temperatures. In addition, they must be thermally stable and show low stress and good adhesion. Electrically, they must also be conductive and have low contact resistance to both silicon and aluminum. Using titanium as a barrier fulfills these requirements. It adheres very well to common passivation layers as SiN_x or SiO_2. In addition, it is a very good reducing agent of silicon oxide [60] and thus can reduce the native oxide in the contact openings. Furthermore, it is electrically conductive and has a very low contact resistance to both n^+ and p^+ doped silicon [61]. This makes titanium a very attractive contacting metal and is therefore very widely used in

microelectronics as a contacting metal. However, it reacts also with aluminum and silicon to form aluminides and silicides at certain temperatures [62], [63]. In other words, titanium effectively maintains a separation between aluminum and silicon as long as it is not fully consumed by aluminum or silicon as illustrated schematically in Figure 4.8 (right) [64]. Such barriers are therefore classified as sacrificial barriers [65].

When the two reaction rates between the barrier and the other two elements (in this case silicon and aluminum) are known as a function of temperature and time, the minimum thickness to suppress aluminum spiking can be predicted. The formation of titanium aluminides and silicides is very well studied in literature. Aluminides formation starts at temperatures around 350 °C for titanium aluminides [62] and at 500 °C for titanium silicides [63]. In this work only titanium aluminides are considered, since the contact formation annealing applied to the solar cells is below 500 °C.

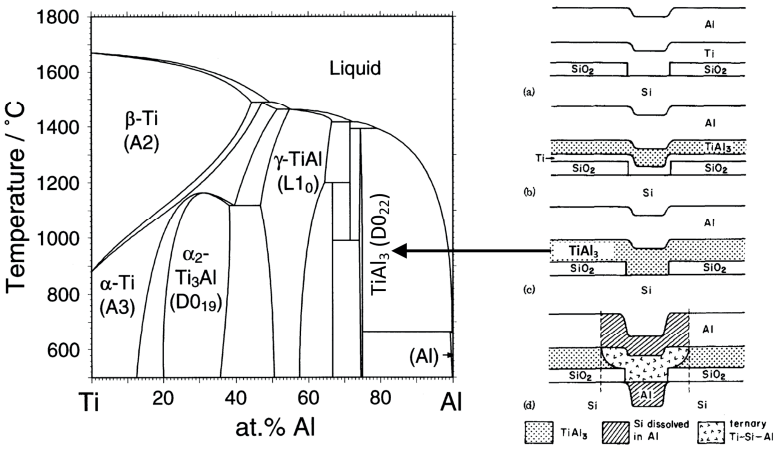

Figure 4.8: Ti-Al phase diagram (left, taken from [66]) shows the first Al-rich intermetallic equilibrium aluminde phase $TiAl_3$. On the right, a sketch illustrating the operation of the sacrificial barrier Ti between Al and Si is shown (taken from [64]).

In thin films reactions, usually a growth of one intermetallic phase is observed at a time in contrast to bulk diffusion couples where all equilibrium phases can exist with sufficient annealing [62]. For aluminides, the initial aluminde phase is

usually the most aluminum-rich phase on the phase diagram and the dominant diffusing species during this phase formation is aluminum [62]. The initial phase formation is determined more by kinetics and moving species than by thermodynamic driving forces [62]. Nucleation, initial reaction temperature, interface uniformity, presence of impurities, etc. can also be influential factors for initial phase formations [62].

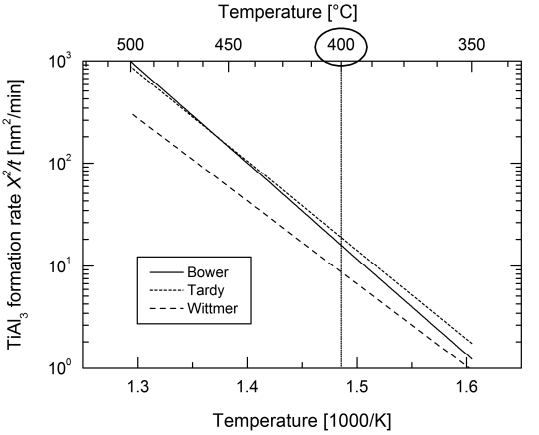

Figure 4.9: Arrhenius plot for $TiAl_3$ formation from data obtained from Bower [64], Tardy [67] and Wittmer [68].

The reaction rate (X^2/t) of two materials with diffusion controlled kinetics are given by

$$\frac{X^2}{t} = D_0 \cdot e^{-\frac{E_a}{kT}}. \tag{4.1}$$

Here, X is the compound layer thickness, E_a is the activation energy for the compound growth, D_0 is pre-exponential constant and t and T are the annealing time and temperature, respectively [62].

Based on the phase diagram of titanium-aluminum system (Figure 4.8, left), the compound $TiAl_3$ will be initially formed when titanium and aluminum thin films start to react which is also observed and extensively studied by many authors

[64], [67], [68]. In Figure 4.9 the Arrhenius plot for $TiAl_3$ formation (reaction rate as a function of annealing temperature) is shown from various literature data obtained from RBS-measurements (Rutherford Backscattering Spectrometry) below 500 °C.

Table 4.1: The formation rate of $TiAl_3$ at 400 °C and the consumed layer thickness of titanium at 400 °C after 5 min from data obtained from Bower [64], Tardy [67] and Wittmer [68].

Ref.	D_0 (cm^2/s)	E_a (eV)	X^2/t at 400 °C (nm^2/min)	d_{TiAl3} formed at 400 °C after 5 min (nm)	d_{Ti} consumed at 400 °C after 5 min (nm)
[64]	1.9	1.85	16	8.9	7.9
[67]	0.25	1.72	19	9.7	8.7
[68]	0.014	1.6	8.8	6.6	5.9

The formation rate of $TiAl_3$ at 400 °C and the consumed layer thickness of titanium at 400 °C after 5 min are summarized in Table 4.1. The literature data show that a titanium layer thickness around 8 nm will be consumed for the formation of $TiAl_3$ intermetallic compound when a contact formation annealing at 400 °C for five minutes is applied. In other words, a thin titanium layer of at least ~ 8 nm layer thickness is required to maintain a separation between aluminum and silicon and thus prevent aluminum spiking for the above mentioned thermal stress.

4.3.2 SEM structural investigations of Ti/Al-stack

To verify the theoretical data summarized in Table 4.1, specific test samples featuring the rear side structure of nPERT solar cells were fabricated and characterized as illustrated in section 4.2. Table 4.2 summarizes the metallization variants of the investigated samples with Ti/Al metallization. The experimental results are shown in Figure 4.10.

Table 4.2: The metallization variants of the investigated samples with Ti/Al metallization. The process details of the aluminum and titanium sputtering deposition are given in Table 3.1 and Table 3.4, respectively.

Sample	a	b	c	d
Metallization	Ti/Al	Ti/Al	Ti/Al	Ti/Al
Ti process nr.	18	19	20	21
Ti thickness (nm)	~ 3	~ 10	~ 20	~ 50
Al process nr.	3	3	3	3
Al thickness (µm)	~ 2.1	~ 2.1	~ 2.1	~ 2.1

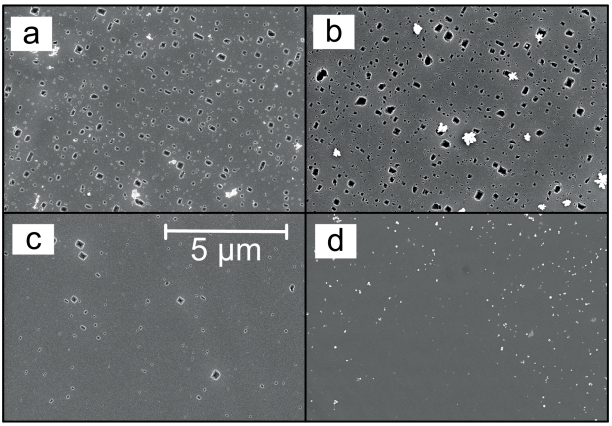

Figure 4.10: SEM-images after metallization removal of Ti/Al stack with 3 (a), 10 (b), 20 (c) and 50 (d) nm Ti thickness. A Ti barrier thickness of >20 nm is needed to prevent Si-diffusion in Al for a thermal process at 400 °C for 5 min.

As expected from the theoretical study the number and size of spikes is reduced with increasing titanium layer thickness. However, they completely disappear for titanium thickness between 20 and 50 nm. This does not fit well to the theoretical results of Table 4.1. Many factors could be the reason for this discrepancy. The high surface roughness of Cz silicon wafers compared to the polished surface of float-tone silicon (FZ-Si) wafers used in the literature studies might be the main reason. Interface uniformity, presence of impurities and inaccuracy of the layer thickness or of the annealing temperature can also be

reasons for this discrepancy. The thicknesses of the thin titanium layers were estimated by adjusting the sputtering process time on the basis of the deposition rate.

4.4 Novel Al-Si/Al-stack against Al-spiking

It is well known that the use of silicon-enriched aluminum-metallization (Al-Si) instead of pure aluminum suppresses aluminum spiking in silicon. The alloying of aluminum with silicon fulfills the solubility requirement of silicon in aluminum and no silicon from the wafer will diffuse into the aluminum layer. The amount of aluminum penetration can be adjusted and reduced by optimizing the concentration of silicon in the Al-Si layer needed to fulfill the solubility limit requirement at a given temperature (e.g. 0.24 at% at 400 °C and 0.8 at% at 500 °C, Figure 4.3-left). Al-Si alloys can suppress spikes formation, however, undesired precipitation of *p*-doped silicon [69] at the boundaries between silicon and the Al-Si metallization occurs if the atomic concentration of silicon in the aluminum layer is higher than the solubility requirement at a given annealing temperature. In this case an increase in contact resistance for contacting n^+-silicon may occur [70].

In order to vary the silicon concentration required to withstand an annealing process at a given temperature, a stack of Al-Si (1 at% Si throughout the thesis) with varying layer thicknesses and a 2.1-µm-thick aluminum cap-layer was used. The aluminum cap-layer is required to minimize the lateral ohmic losses of the full-area metallization to negligible values (section 2.3.1). Since one atomic percent of silicon in aluminum is about four time higher than the solubility limit of silicon in aluminum at 400 °C (0.24 at%), a one-layer Al-Si metallization will result in an undesirably strong silicon precipitation. Thus, by using Al-Si/Al stack instead of one-layer Al-Si metallization, the amount of silicon precipitation may be reduced, which will be investigated in this section. Rear-side metallization consisting of an Al-Si/Al stack can be therefore a promising approach between one-layer Al-Si metallization with undesired strong silicon precipitation and one-layer aluminum metallization with undesired aluminum spiking. To the knowledge of the author only one-layer Al-Si metallization against spike formation has been reported e.g. [70], [71].

Firstly, simulations were performed to model the interdiffusion in these stacks. Subsequently, test samples were fabricated to verify the simulation results experimentally.

4.4.1 Process simulation of Al/Al-Si/Si system

A model for the interdiffusion was created using the multiphysics code COMSOL 4.3a [72]. The models in the package "Transport of diluted species" [73] were modified to include the dependence on the solubility of the diffusing species aluminum and silicon. The resulting Fick-like equations are given by

$$\frac{\partial}{\partial x}\left[D_A\left(\frac{\partial C_A}{\partial x}-\frac{C_A}{C_A^{eq}}\frac{\partial C_A^{eq}}{\partial x}\right)\right]=\frac{\partial C_A}{\partial t}. \tag{4.2}$$

Here, C_A, D_A, and C_A^{eq} are the concentration, diffusivity and solubility limits of the species A [74].

A one dimensional system model with aluminum and silicon regions in contact serves as a matrix for the diffusion of the species Al and Si. An Al-Si layer of thickness ($d_{Al\text{-}Si}$) is considered a part of the aluminum matrix. The x-coordinate gives the depth of the stack with zero starting at the Al-Si/Al contact point, the aluminum matrix in negative, and correspondingly the silicon matrix in positive direction with a start at the depth $d_{Al\text{-}Si}$ (Figure 4.11). Since the diffusivities of aluminum and silicon in a silicon matrix at 400 °C are more than ten orders lower than in an aluminum matrix (Figure 4.3), only the latter are considered in this simulation. The value of the solubility limit of aluminum in silicon can also be neglected at 400 °C (Figure 4.3) and is therefore not considered in the simulation as well. Furthermore, the voids created during contact formation annealing will be filled by aluminum rather than silicon due to the significantly higher self-diffusivity of aluminum than the self-diffusivity of silicon (Figure 4.3). Therefore, aluminum will come in contact with new zones deeper in the silicon matrix and the diffusivity of the silicon species will increase there. This diffusion can be simulated by its consequences in silicon: the increase of the diffusivity of silicon in the contact region until a given depth (in this work

assumed to be 200 nm[2]). Based on this, the model contains only two temperature dependent parameters: diffusivity and solubility limit of silicon in aluminum and hence only the diffusion equation for silicon must be solved.

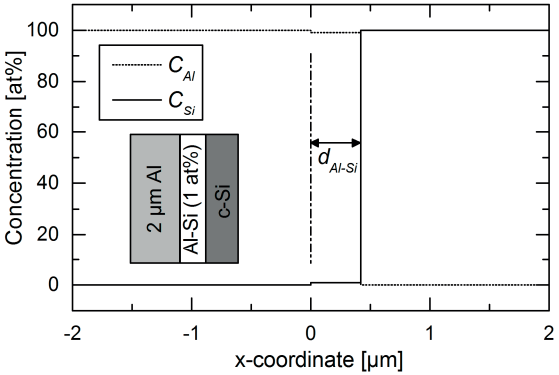

Figure 4.11: One dimensional model for Al/Al-Si/Si system. The Al-Si layer with 1 at% Si and a thickness $d_{Al\text{-}Si}$ is considered as a part of the Al-matrix and starts at the x-coordinate zero.

By checking the concentration of silicon in the contact region the degree of spiking and precipitation can be monitored. The thickness of the Al-Si layer in the Al-Si/Al stack was varied from 0 to 600 nm, whereas the simulation with only Al-Si metallization was done with 2 µm layer thickness. The heat treatment profile used in the simulation has a peak temperature at 400 °C for 5 min and a smooth ramp-up and -down around 3 K/s. The simulation results represent the sample status after the peak temperature zone of the annealing profile.

Figure 4.12 (left) shows the results of one-layer aluminum metallization and Figure 4.12 (right) shows the results of one-layer Al-Si metallization at 400 °C after 5 min. The simulation results for single layer aluminum metallization shows that the concentration of silicon in the silicon matrix near the contact interface is decreased. This indicates that silicon from the silicon matrix diffused out into the aluminum matrix and left a void which will be filled by aluminum. This is typical spiking. In the case of one-layer Al-Si metallization – where silicon

[2] The volume change of the resulting void or Si-precipitate at the interface, which quantifies the amount of Si out-diffused or precipitated, is independent of the selection of this depth.

concentration of 1 at% is well over the solubility limit during the whole heat treatment – the concentration of silicon in the silicon matrix near the contact interface is increased. This indicates that silicon from the Al-Si layer diffused into the silicon matrix and precipitated at the interface. Silicon precipitates are *p*-doped silicon (with aluminum as a dopant) [69] and can increase the contact resistance between aluminum and n^+-silicon [70], [71].

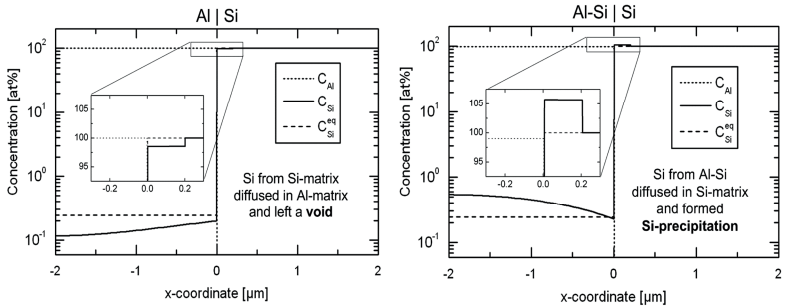

Figure 4.12: Simulation results of Al/Si system without an Al-Si barrier at 400 °C after 5 min (left). Since the concentration of Si at the beginning of the annealing process is below the solubility limit, Si from Si-matrix diffused in Al-matrix and left a void at the interface which is filled by Al. Simulation results of Al-Si/Si system at 400 °C after 5 min (right). Since the concentration of Si at the beginning of the annealing process (1 at%) is above the solubility limit (~0.24 at%) for the given process conditions, Si from Al-Si diffused back in the Si matrix and precipitated at the interface.

The results of the simulated samples with Al-Si/Al stack and varying Al-Si layer thickness are shown in Figure 4.13. The Al-Si barrier acts as a source of silicon for the aluminum layer during the heat treatment as long as the concentration of silicon in the Al-Si layer stays above the solubility limit. As soon as the concentration of silicon in the Al-Si layer is reduced below the solubility limit, silicon from the silicon matrix starts to diffuse out into the Al-Si/Al stack leaving voids. The amount of the removed silicon from the silicon matrix near the contact region, which gives information about the amount of aluminum penetration, strongly depends on the Al-Si layer thickness used. Observation of the close-ups of the interface region in Figure 4.13 shows that spiking is reduced by increasing Al-Si thickness until there is no spiking for Al-Si thickness around 400 nm. By further increasing the Al-Si thickness the opposite process silicon precipitation starts to occur. In this case the initial silicon content in the Al-Si

layer is greater than the Al-Si/Al stack can dissolve. The precipitation is minimal in the case of 420-nm-thick Al-Si and by increasing the thickness beyond this value the degree of silicon precipitation increases as observed in Figure 4.13 (d).

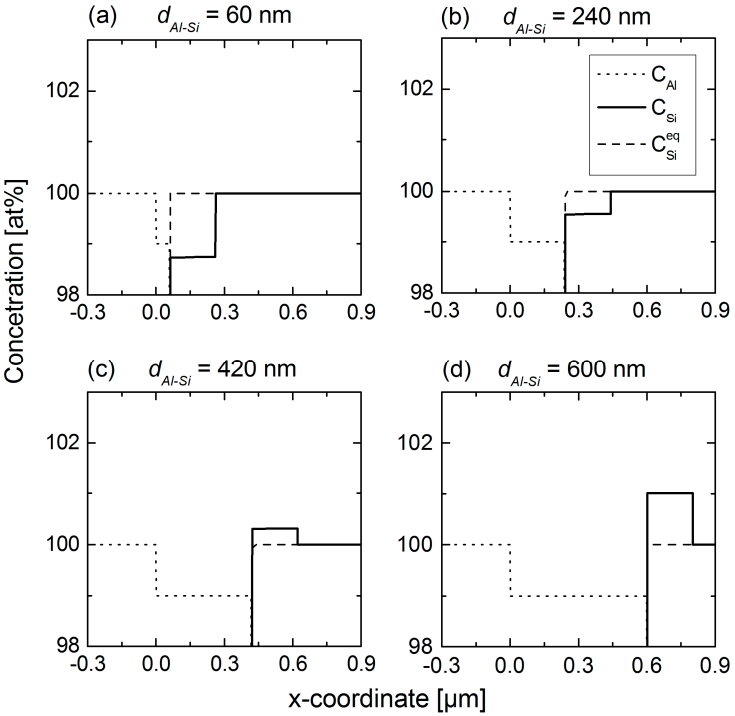

Figure 4.13 Simulation results of Al/Al-Si/Si system for 60 nm (a), 240 nm (b), 420 nm (c) and 600 nm (d) Al-Si barrier. The optimal Al-Si barrier when Al-spiking is suppressed with only a slight Si-precipitation is around 400 nm.

4.4.2 SEM structural investigations of Al-Si/Al stack

In order to verify the process simulation results experimentally, test samples featuring the rear side structure of nPERT solar cells were fabricated and characterized as illustrated in section 4.2. For the sputtering of the aluminum layer the process 3 of Table 3.1 was used. Table 4.3 summarizes the metallization variants of the investigated samples with Al, Al-Si and Al-Si/Al metallization. The various Al-Si layers were sputtered as in Table 3.2.

Table 4.3: The metallization variants of the investigated samples with A, Al-Si and Al-Si/Al metallization.

Sample	a	b	d	e	f
Metallization	Al	Al-Si/Al	Al-Si/Al	Al-Si/Al	Al-Si
Al-Si process	---	4	6	7	9
Al-Si thickness (nm)	0	~60	~ 240	~ 420	~ 2170
Al process	3	3	3	3	3
Al thickness (µm)	~ 2.1	~ 2.1	~ 2.1	~ 2.1	---

The experimental results are presented in Figure 4.14.

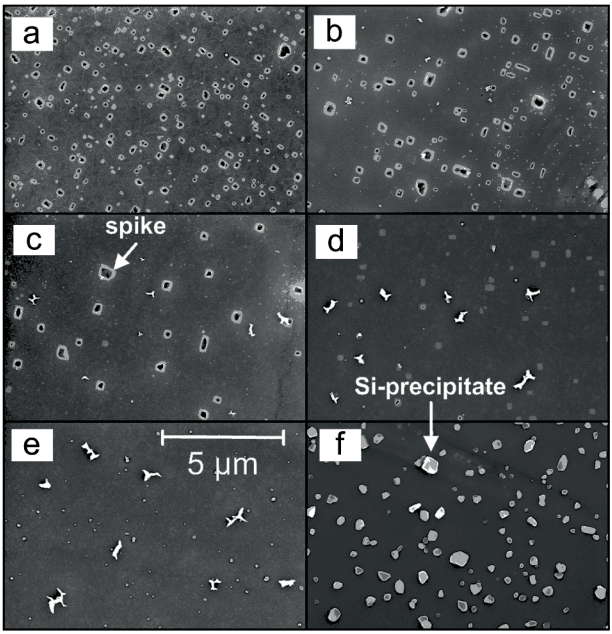

Figure 4.14: SEM-images after metallization removal with 2 µm Al (a), 2 µm Al-Si (f), and Al-Si/Al stack with 60 (b), 240 (c), 420 (d), and 600 nm (e) Al-Si thickness. As predicted from the simulation, the optimal Al-Si barrier where Al-spiking is suppressed with only a slight Si-precipitation is ~ 420 nm.

The experimental results are in very good agreement with the simulation results: The number and size of spikes is reduced with increasing Al-Si layer thickness

and they almost disappear for d_{AlSi} ~ 420 nm. No spikes were detectable for the sample with 600-nm-thick Al-Si barrier but slight silicon precipitation is observed. For ~ 2.1-µm-thick Al-Si metallization strong silicon precipitation and complete absence of spikes is also clear in the SEM-image as predicted from the process simulation.

4.5 Summary and conclusion

In this chapter, the contact-formation process of aluminum-based metallization was investigated. The spiking phenomenon of aluminum in silicon due to the high solubility and diffusivity of silicon in aluminum at processing temperatures was illustrated. Solutions to overcome aluminum spiking were presented and discussed. The state of the art approaches to suppress spike formation as the use of the sacrificial barrier titanium or one-layer Al-Si (1 at% Si) were investigated for silicon solar cells applications on Cz wafers. Furthermore, a novel approach by using Al-Si/Al stack was presented. Simulations as well as SEM structural investigations on Cz silicon wafers featuring the rear-side of nPERT solar cells were carried out in order to study the potential of these approaches against aluminum spiking.

The results showed that aluminum spiking can be overcome by the use of a sufficiently thick sacrificial spiking barrier like titanium. For a contact formation annealing at 400 °C for 5 min, a titanium layer thickness of at least 20 nm is required to suppress spike formation on Cz silicon wafers which is more than the thickness obtained from reported reaction kinetics between aluminum and titanium. SEM images of the samples with one-layer Al-Si metallization showed a complete absence of aluminum spikes, however, with a strong silicon precipitation. Silicon precipitations are *p*-doped silicon and might cause an increase in contact resistance when applied to an n^+-doped silicon. The use of Al-Si/Al stack instead of one-layer Al-Si metallization resulted in a significant decrease of silicon precipitation combined with a suppression of aluminum spiking. The process simulation as well as the experimental results showed that an Al-Si layer thickness around 400 nm is required to suppress the formation of aluminum spikes as well as silicon precipitations for 2-µm-Al metallization and a contact formation annealing at

400 °C. It is worth to note, that if the aluminum layer thickness or the thermal stress applied is different (e.g. for other applications than the one in this thesis), the thickness of the Al-Si must be adapted.

In the following chapter the specific contact resistance of the different rear-side metallization schemes Al, Ti/Al stack and Al-Si/Al stack on n^+-Si point contacts as for the rear-side of front-junction nPERT solar cells is investigated.

5 Specific contact resistance evaluation

In the previous chapter the spiking phenomenon was investigated in detail and it was shown that a diffusion barrier (e.g. 20-nm-thick titanium) between the silicon wafer and the aluminum layer can suppress the out-diffusion of silicon and hence aluminum spiking. It was also demonstrated that a silicon-enriched aluminum metallization (Al-Si or Al-Si/Al) can also prevent spike formation, however, a formation of undesired *p*-doped silicon precipitation can occur. The *p*-type silicon precipitation can have a negative influence on the contact resistance on highly doped *n*-type silicon.

Specific contact resistance of metal-semiconductor contacts is a very important parameter for high efficiency silicon solar cells. Its value must be kept sufficiently low in order to reduce the ohmic loss to a negligible level and ensure high performance of a solar cell (Figure 2.14). Depending on the cell design, rear contacts can be of either linear (i.e. grid) or circular (i.e. point contacts) shape. Point contacts are more promising since they require less total contact area and hence more passivation area can be kept which in return means a higher cell efficiency. Many cell designs can be found featuring point contacts on the rear such as PERC [2], PERT [3] (as in this thesis), PERL [4], and BJ-BC [75] solar cells. The cell structure of PERC solar cells features silicon wafer without a highly doped region on the rear whereas the other aforementioned cell designs include highly doped regions on the rear side of the silicon wafer. In order to develop high performance and cost-effective rear point contacts for these solar cells in an industrial environment, a reliable and quick determination of rear specific contact resistance is required which done during this thesis. The characterization method is presented in the following section. By using this method, experimental results of specific contact resistance are shown for the metallization variants Al, Al-Si, Al-Si/Al and Ti/Al stack on two n^+-Si profiles with varying surface dopant concentrations. The experimental results are compared with previously published results. The results of this chapter are published in [76] as well as in [49].

5.1 Determination of specific contact resistance of point contacts on highly doped silicon

Specific contact resistance of semiconductor–metal contacts can be determined in several ways as twin contact, extrapolation, differential, interface probing, and the widely used transfer length method [77]. These measuring techniques are mainly based on linear contact geometries and cannot be applied to determine specific contact resistance on point contacts automatically without further efforts. Wolf et al. [78] and Nekarda [79] did modelling and experimental works to characterize point contacts on bare *p*-type silicon wafers without any highly doped regions (e.g. for PERC solar cells). In this work a similar approach is developed but in contrast to Wolf and Nekarda, the method is used to determine the specific contact resistance of metal-semiconductor point contacts exclusively on silicon wafers with highly doped regions. This approach is presented in the following.

5.1.1 Sample structure and experimental setup

The sample structure and the experimental setup for the determination of specific contact resistance of point contacts is shown in Figure 5.1. Similar to the twin contact method [80] and the approach used by Wolf and Nekarda, the test sample has two contacts on opposite sides of the wafer. The difference to the other methods is the full-area highly doped regions underneath both front and rear contact. The front-side of the test samples features full-area contact whereas the rear side is contacted with a number of point contacts of radius r_c and contact spacing L_p by using a locally opened passivation layer. A wafer of the same polarity as the doped regions must be used to ensure a current flow across the sample. This means that *n*-type silicon wafer must be used when the characterization of the contact resistance to n^+-Si is required and *p*-type wafers for the opposite case. The determination of rear specific contact resistance $\rho_{c,rear}$ is effected by measuring the resistance R through the test sample. The latter is obtained from a linear fit of *J-V* data measured with a Keithley source meter and a suitable four point probe setup by contacting both sides of the test sample with copper plates as shown in Figure 5.1 (c) and Figure 5.1 (d). The applied voltage in the *J-V* measurement was varied from 0 to 50 mV for all samples.

The extraction of the rear specific contact resistance from the measured resistance of the whole sample is described in 5.1.2 and 5.1.3.

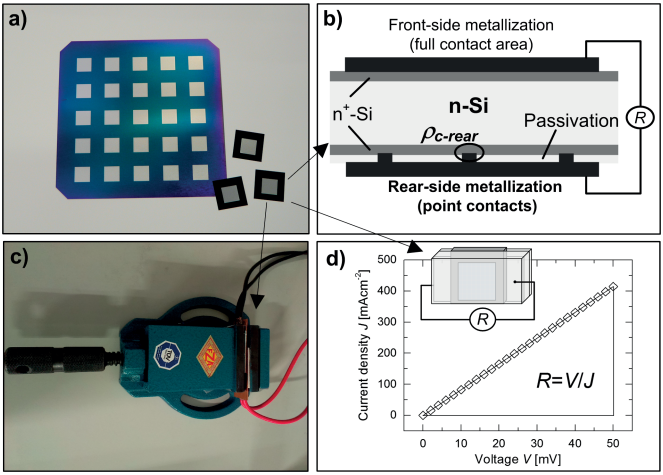

Figure 5.1: A processed silicon wafer (a), a sketch of the test sample (b), the measurement apparatus (c) and J(V) (d) are shown.

Since the objective of this work is the determination of the specific contact resistance of point contacts on n^+-doped silicon – as for the rear-side of nPERT solar cells with front side emitter – *n*-type silicon wafers were used. The wafers were taken from the same region of the ingot to ensure wafer resistivity of about the same value for all test samples. The wafer resistivity has a big influence on the overall resistance of the test sample. Consequently, the resistivity of monitoring wafers from the same region of the ingot was measured before and after processing the test samples determining the wafer resistivity confidence range. The resistivity of the test sample might be different after processing due to the high thermal processing steps during test samples fabrication (e.g. during firing or high temperature doping processes). The resistivity of Czochralski-grown silicon is known to change after thermal processing due to the activation or deactivation of oxygen related thermal donors in silicon [81]. Thermal donors can be activated at temperatures around 450 °C and deactivated at temperatures above 550 °C [82]. Therefore, the resistivity of the monitoring wafers was measured after destroying the thermal donors by a high thermal process similar

to the test samples. The wafer resistivity was determined by measuring the sheet resistance and the thickness of five monitoring wafers at five positions each. The thickness and resistivity of the monitoring wafers are shown in Table 5.1.

Table 5.1: Thickness and resistivity results of five monitoring wafers before and after deactivation of thermal donors.

W (µm)	R_{sh} (Ω/sq) As-cut	R_{sh} (Ω/sq) After firing	ϱ_{bulk} (Ωcm) As-cut	ϱ_{bulk} (Ωcm) After firing
158.7 ± 3.6	249.1 ± 12.1	292.6 ± 17.3	3.95 ± 0.16	4.64 ± 0.25

The n^+-doped regions were fabricated on both sides by ion implantation and with phosphorous as dopant species. By varying the implant dose and thus the doping level, the influence of dopant surface concentration N_s on rear specific contact resistance $\rho_{c,rear}$ was investigated, since N_s is known to affect $\rho_{c,rear}$ [33]. The parameters of the implantation processes and the resulting sheet resistances are shown in Table 5.2. Specific p-type silicon wafers were used here in order to measure the sheet resistance of the highly doped regions without the influence of the wafer resistivity. The resulting SIMS profiles are shown in Figure 5.2.

Table 5.2: Implant parameters and resulted sheet resistances.

Ion implantation process	Dose (cm^{-3})	Energy (keV)	Drive-in annealing process	R_{sh} (Ω/sq)
1	0.5×10^{15}	10	930 °C, 2h	136.1 ± 1.3
2	1×10^{15}	10	930 °C, 2h	75.3 ± 0.9

The surface doping concentration of profile-1 is found to be approximately 3.8×10^{19} cm^{-3} and profile-2 of about 6.9×10^{19} cm^{-3}. After processing the n^+-Si regions on both surfaces, the wafers were chemically cleaned. Thereafter, the rear-side was passivated with PECVD SiN_x/SiO_2 stack (70 / 210 nm). The point contacts were identically processed as for the nPERT solar cells by laser ablation using a Nd:YVO4 laser source with a fixed pulse length of ~ 10 ps and a wavelength of 532 nm resulting in laser fluence of about 0.8 J/cm². The resultant contact radii were in the range 18 ± 0.5 µm (the confidence range was obtained from measured contact radius data over 100 values) and a varied contact spacing from 300 to 1200 µm (Figure 5.3).

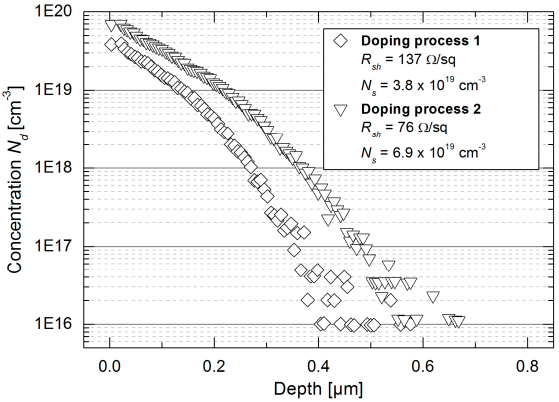

Figure 5.2: Doping profiles of the fabricated test samples.

Subsequently, Ti/Al stack was sputtered on the front side to ensure that the front side is identical for all samples. The investigated metallization schemes were deposited on the rear side by the SOLARIS 6 deposition system with the high-power Al-sputtering process at 14 kW to ensure an in-situ dynamic contact formation annealing. The metal layers were sputtered using a shadow mask in order to get 25 small test samples from the whole 15.6 × 15.6 cm² Cz-wafer as shown in Figure 5.1-a. The investigated metallization variants are listed in Table 5.3. The processed wafers were afterwards laser cut into pieces with a metalized area of 1.2 × 1.2 cm². Finally, contact formation annealing step at 400 °C for 5 minutes in N_2-ambient was applied to the half of the test samples.

Table 5.3: The metallization variants of the investigated resistance samples. The metallization layers were sputtered as described in Chapter 3 (Al at 14 kW, Al-Si at 10 kW and Ti at 3 kW).

Group	1	2	3	4
Metallization	700 nm Al	20 nm Ti / 700 nm Al	120 nm Al-Si / 700 nm Al	700 nm Al-Si

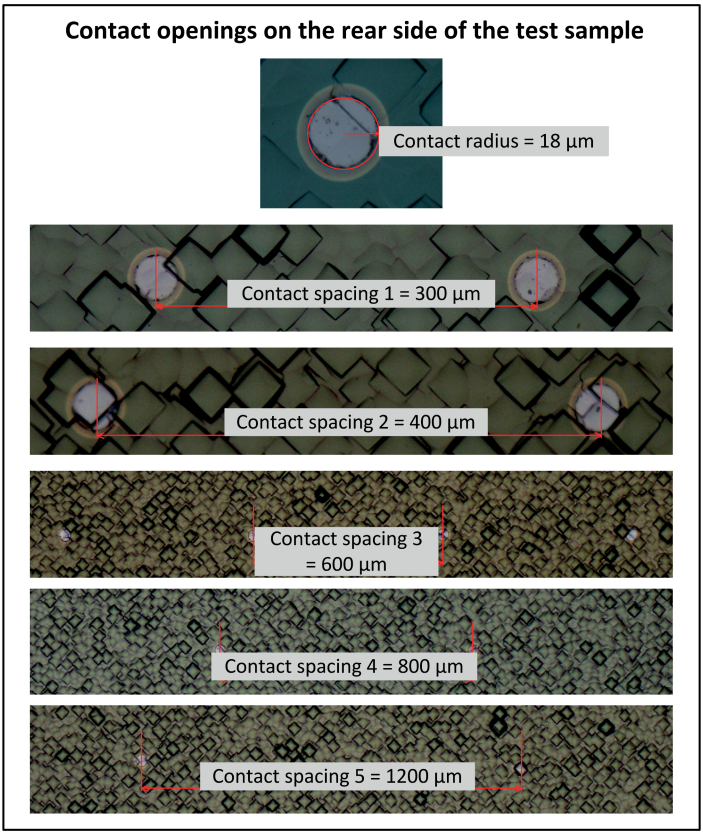

Figure 5.3: Microscope images of the rear contact openings of the test samples.

5.1.2 Analytical model to extract the contact resistance of the point contact from the measured data

The measured total resistance of the test sample includes many resistance contributions such as bulk resistance of the silicon wafer, sheet resistance of the highly doped regions, lateral resistance of the metallization and contact resistance of both sides. In the following, a simplified analytical model to extract the contact resistance of the point contact $R_{c0,back}$ is derived and verified later with device simulations.

In order to simplify the derivation of an analytical model describing the resistance of the test sample, two approximations are used. In the first one, it is assumed that the current homogeneously flows in the vertical direction through the sample from the front contact to the highly doped back surface field and afterwards laterally to the rear point contact (Figure 5.4). This approximation is acceptable as the difference in the doping level between the bulk *n*-type silicon and the n^+-doped back surface field (BSF) is high.

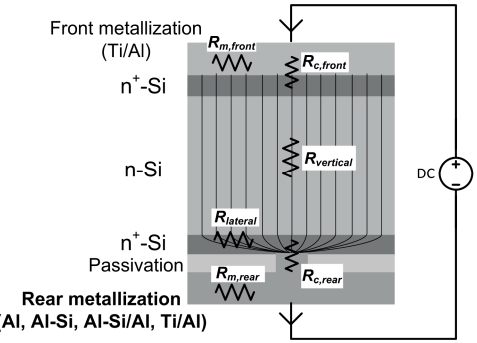

Figure 5.4: Cross-sectional view of the symmetry element of the test sample showing the resistance contributions to the total resistance of the sample.

Under this approximation, the resistance through the sample can be written as

$$R[\Omega cm^2] = R_{vertical} + R_{lateral} + R_{c,rear} + R_{rest}, \tag{5.1}$$

where $R_{vertical}$ is the vertical resistance contribution through the wafer, $R_{lateral}$ is the lateral resistance contribution in the wafer to the rear point contacts, $R_{c,rear}$ the contact resistance of the rear side and R_{rest} the rest resistance contributions such as contact resistance of the front and the lateral resistance of both front and rear metallization (Figure 5.4). In the following, a formula will be derived for each resistance contribution in order to model the resistance of the sample *R*.

The vertical resistance $R_{vertical}$ is given by

$$R_{vertical}[\Omega] = \int_0^W \frac{\rho_{bulk}}{A}\,dx = \frac{W \cdot \rho_{bulk}}{A}. \tag{5.2}$$

Here, W is the wafer thickness and A is the area through which the current flows in the vertical direction and equals 1 cm² for resistance unit Ωcm². Thus, the lateral resistance in Ωcm² will be

$$R_{vertical}[\Omega cm^2] = W \cdot \rho_{bulk}. \tag{5.3}$$

The contribution of the highly doped thin and very conductive regions to the vertical resistance is neglected, since it is very small compared to the contribution of the wafer itself.

The second approximation is used in order to calculate the lateral resistance contribution $R_{lateral}$ with a simple analytical approach. In a real sample, the current flows from a square shaped symmetry element to a circle shaped contact opening with radius r_c. This is simplified with a circle shaped symmetry element instead of the real square one. Both assumptions will be verified with TCAD device simulations in 5.1.4. With this assumption, $R_{lateral}$ will be

$$R_{lateral}[\Omega] = \int_{r_c}^{L_p/2} \frac{\rho}{A}dr = \int_{r_c}^{L_p/2} \frac{\rho}{d2\pi r}dr = \frac{R_{sh}^*}{2\pi} ln\left(\frac{L_p}{2r_c}\right). \tag{5.4}$$

In this equation, ρ and d is the effective resistivity and the thickness of the layer or layers through which the current flows in the lateral direction. As the sample structure features a highly doped BSF and a silicon wafer of the same polarity, the current will effectively flow through a parallel connection of the wafer and the BSF layer towards the back contact resulting in an effective resistance R_{sh}^*

$$R_{sh}^*[\Omega] = \frac{(\rho_{bulk}/W) \cdot R_{sh}}{(\rho_{bulk}/W) + R_{sh}} = \frac{\rho_{bulk} \cdot R_{sh}}{\rho_{bulk} + W \cdot R_{sh}}, \tag{5.5}$$

where R_{sh} is the sheet resistance of the highly doped BSF layer. In order to obtain the lateral resistance $R_{lateral}$ in the unit Ωcm^2, equation (5.4) must be also multiplied by the area of the symmetry element (L_p^2-πr_c^2). The lateral resistance $R_{lateral}$ in the unit Ωcm^2 is thus

$$R_{lateral}[\Omega\mathrm{cm}^2] = \left({L_p}^2 - \pi {r_c}^2\right)\frac{R_{sh}^*}{2\pi}\, ln\left(\frac{L_p}{2 \cdot r_c}\right). \tag{5.6}$$

The contact resistance of the rear-side $R_{c,rear}$ is a parallel connection of the contact resistance of all contact openings on the rear-side $R_{c0,rear}$ and is given by

$$R_{c,rear}[\Omega\mathrm{cm}^2] = \frac{R_{c0,rear}}{n} = {L_p}^2 \cdot R_{c0,rear}\,, \tag{5.7}$$

where n is the number of rear point contacts and equals $1/L_p^2$ for point contacts in an area of 1 cm^2 and $R_{c0,rear}$ is the contact resistance of a one contact opening.

At this point inserting the obtained expressions of $R_{vertical}$, $R_{lateral}$ and $R_{c,rear}$ (equations (5.3), (5.6) and (5.7), respectively) in equation (5.1), the overall resistance of the test sample in the unit Ωcm^2 can be obtained. Hence producing

$$\begin{aligned} R[\Omega\mathrm{cm}^2] = R_{rest} &+ W \cdot \rho_{bulk} \\ &+ \left({L_p}^2 - \pi {r_c}^2\right)\frac{R_{sh}^*}{2\pi}\, ln\left(\frac{L_p}{2 \cdot r_c}\right) \\ &+ {L_p}^2 R_{c0,rear}. \end{aligned} \tag{5.8}$$

From equation (5.8), it can be concluded that that by measuring the resistance through the sample R for various contact spacings L_p the contact resistance of the contact opening $R_{c0,rear}$ can be obtained by fitting the measured data as shown in Figure 5.5 (left). The wafer thickness W, wafer resistivity ρ_{bulk} and the sheet resistance of the highly doped BSF R_{sh} can be measured on real samples and thus used as input parameters. The knowledge of the remaining resistance R_{rest} is not required, since R_{rest} neither depends on the contact spacing nor on the radius of the contact openings. A different R_{rest} value results only in a curve shift in the y-axis direction and has no influence on the fitted $R_{c0,rear}$ as shown in

Figure 5.5 (right). The term R_{rest} can be obtained from the fitted data as well. The estimation of the rear specific contact resistance $\rho_{c,rear}$ from the contact resistance of the contact opening $R_{c0,rear}$ is described in the following section.

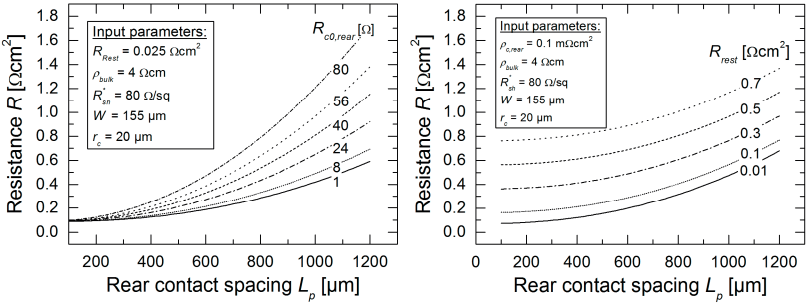

Figure 5.5: Simulated total resistance of the used test samples as a function of rear contact spacing for various $R_{c0,rear}$ (left) and R_{rest} (right).

5.1.3 Circular transmission line model to determine rear specific contact resistance $\rho_{c,rear}$

Specific contact resistance ρ_c in general is defined as [77]

$$\rho_c[\Omega\text{cm}^2] = \lim_{\Delta A_c \to 0} (R_{c0} \cdot \Delta A_c), \tag{5.9}$$

where R_{c0} is the contact resistance and A_c is the contact area of the contact. Assuming the current flows uniformly through the whole contact area of a point contact, equation (5.9) is simplified to [77]

$$\rho_c[\Omega\text{cm}^2] = R_{c0} \cdot A_c = R_{c0} \cdot \pi {r_c}^2. \tag{5.10}$$

In a real sample, however, the current collection might occur at a less area than the contact area A_c due to the lateral current flow towards the contact opening which gives rise to current crowding at the edge of the contact (Figure 5.6).

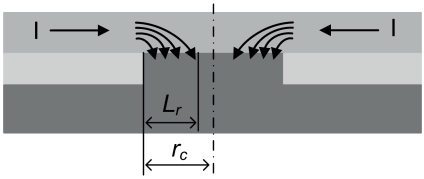

Figure 5.6: The current can be crowded at the edge of the contact depending on the specific contact resistance, sheet resistance beneath the contact and contact radius due to the lateral current transport to the point contact.

Therefore, equation (5.10) has to be modified. For this, a circular transmission line model is used which is taken from the circular transmission length method (CTLM) [83]. CTLM uses a central dot with two circular concentric contact rings. Reeves et al. [83] derived circular transmission line models for the central dot as well as the circular contact rings in the CTLM method. In order to determine rear specific contact resistance $\rho_{c,rear}$ of the samples from the experimentally obtained $R_{c0,rear}$, the circular transmission line model of the inner dot in the CTLM method is adapted. The sheet resistance in Reeves model is replaced by the effective sheet resistance R_{sh}^* described in equation (5.5).

The contact resistance of the point contact is correspondingly given by [83]

$$R_{c0,rear}[\Omega] = \frac{R_{sh}^*}{2\pi\alpha} \cdot \frac{I_0(\alpha)}{I_1(\alpha)}, \tag{5.11}$$

where I_0 and I_1 are the zero- and first-order modified Bessel functions of the first kind, respectively [84] and α is defined as

$$\alpha = r_c \sqrt{\frac{R_{sh}^*}{\rho_c}}. \tag{5.12}$$

The ratio between the contact resistance of the point contact $R_{c0,rear}$ (5.11) and the one without considering current crowding (5.10) is defined as β

$$\beta = \frac{R_{c0,rear}}{\left(\rho_{c,rear}/A_c\right)}. \tag{5.13}$$

When $\beta \approx 1$, then the contact resistance $R_{c0,rear} \approx \rho_{c,rear}/A_c$ and the effect of current crowding is negligible. This is the case if α is less than 0.5 as can be seen

in Figure 5.7. From equation (5.12) it is obvious that for point contacts not only the sheet resistance and specific contact resistance has an influence on the magnitude of current crowding (as the case of linear contacts) but also the contact radius.

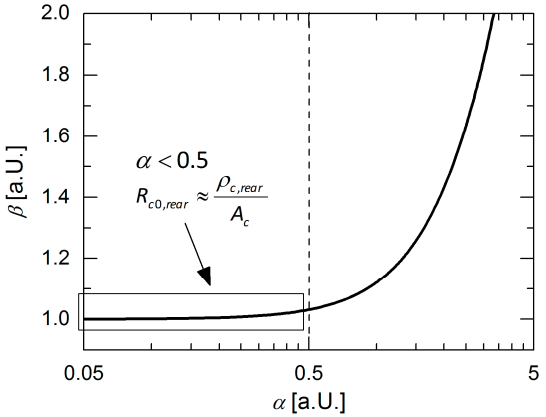

Figure 5.7: The ratio between the contact resistance of point contact with and without current crowding β as a function of α showing that when α is less than 0.5 the effect of current crowding can be neglected.

The contact resistance $R_{c0,rear}$ can also be written as

$$R_{c0,rear}[\Omega] = \frac{\rho_{c,rear}}{A_{c,eff}} = \frac{\rho_{c,rear}}{2\pi r_c L_r - \pi {L_r}^2}, \tag{5.14}$$

where $A_{c,eff} < A_c$ is the effective contact area as a ring instead of a circle and $L_r < r_c$ is defined as the radial transfer length (similar to the transfer length of the TLM method) and is given by

$$L_r = r_c \left[1 - \sqrt{1 - \frac{1}{\alpha r_c}\frac{I_1(\alpha r_c)}{I_0(\alpha r_c)}}\right]. \tag{5.15}$$

This means that the current will be crowded at the edge of the contact and transfer for a length of only L_r instead of the whole contact radius r_c. This is illustrated in Figure 5.8. Both graphs show that if the specific contact resistance

is high enough in comparison to the sheet resistance beneath the contact the current will flow almost through the whole contact area in the event that the contact radius is small enough. In this case $\alpha < 0.5$ and the effect of current crowding can be neglected. For specific contact resistance values less than 5×10^{-4} Ωcm² (as for reported values for PVD-Al on various doped silicon [33]), the effect of current crowding must be considered. For a contact radius around 20 µm (as used in this work) and a specific contact resistance around 10^{-4} Ωcm² the current will transfer for a distance of almost half of the contact radius (Figure 5.8, left-hand side - solid line) and the effective contact area will be about 80 % of the whole contact area (Figure 5.8, right-hand side - solid line). In this incident, 20 % of the contact area of the solar cell is not used as a contact area which might cost recombination losses if the contacts are not passivated.

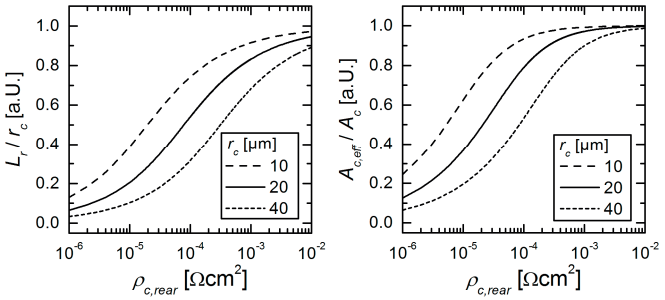

Figure 5.8: The ratio L_t/r_c (left) and $A_{c,eff}/A_c$ (right) as a function of $\rho_{c,rear}$ for various contact radii.

5.1.4 Verification of the analytical approximation with 3D numerical device simulations

In order to verify the analytical approximation for the determination of the rear specific contact resistance, three dimensional numerical device simulations were performed using Synopsys TCAD Sentaurus Device [35]. The same device structure was used as for the resistance sample shown in Figure 5.1-b. Therefore, a 155-µm-thick square-shaped symmetry element with full area front-side contact and a circle contact of radius r_c = 18 µm on the rear is used. The bulk material of the symmetry element is an *n*-type silicon with bulk resistivity ρ_{bulk} of 4 Ωcm and is symmetrically highly doped (n^+) on both sides. For the highly

doped n^+ regions, an error-function profile with a sheet resistance of about 77.5 Ω/sq (similar to the experimental one) was used. An external series resistance of 0.025 Ωcm² is applied to the device in order to take into account the rest resistance R_{rest} of the real sample. Resistance R was simulated as a function of rear contact spacing L_p, while in each run rear specific contact resistance $\rho_{c,rear}$ was varied from 0.01 to 1 mΩcm². The resistance R of the simulated devices were afterwards fitted with equation (5.8) as a function of contact spacing L_p. Afterwards, $\rho_{c,rear}$ was obtained from the fitted $R_{s0,rear}$ by using the circular transmission line model in equation (5.11) in order to compare $\rho_{c,rear}$ obtained by the analytical model with the one set in the time-intensive 3D numerical simulations. The results are shown in Figure 5.9 along with the percentage error of the analytical approximation. The results show an excellent match between $\rho_{c,rear}$ values set in the time-intensive numerical device simulations and ones obtained by the simplified analytical approach for $\rho_{c,rear} > 0.1$ mΩcm². For $\rho_{c,rear} < 0.1$ mΩcm² the percentage error is higher than 10 % and increase to more than 50 % when $\rho_{c,rear}$ is as low as 0.01 mΩcm² (Figure 5.9, right). For nPERT solar cells, however, this error is acceptable since the required specific contact resistance for a sufficiently low ohmic loss is defined to be less than 0.3 mΩcm² for *FF*-loss < 0.25 $\%_{abs}$ (Figure 2.14).

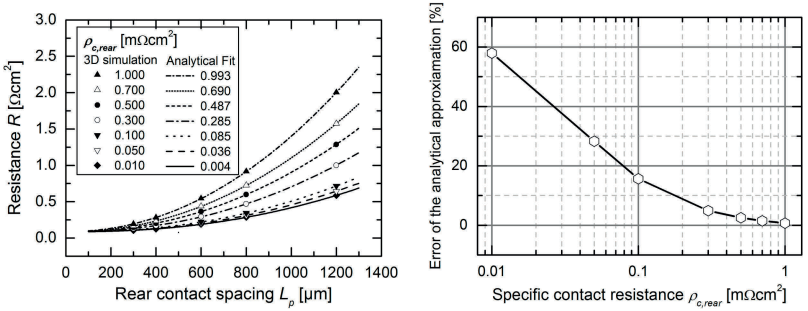

Figure 5.9: Simulated total resistance of the test samples as a function of rear contact spacing. The symbols show the 3D device simulation results and the lines represent the analytical fittings.

5.1.5 Error contributions of wafer thickness and resistivity, BSF sheet resistance and contact radius

The estimation of the specific contact resistance by this method requires the knowledge of wafer thickness, wafer resistivity, sheet resistance of the n^+-doped BSF and contact radius as aforementioned. The uncertainty of these input parameters can affect the estimated specific contact resistance and thusly leading to uncertainty in its obtained value. Given this, a confidence range of the obtained specific contact resistance is investigated in this section.

Due to the specific contact resistance not being measured directly but estimated from the fitted measured data of the sample resistance as a function of rear contact spacing, the error of the obtained specific contact resistance from the fit cannot be determined by standard calculation techniques of error propagation. In the case of standard calculation techniques of error propagation, an error can be obtained for one specific contact resistance value at a certain contact spacing. This, however, does not give any information about the real error, since the specific contact resistance is not obtained at a certain contact spacing value but from the fit of the measured data at various contact spacing values. It is possible that the same error propagation occurs at different contact spacing values which would only result in an offset of the fitted curve and in this case the estimated specific contact resistance from the fit would still be the same. In other words, the uncertainty of this method is described by how far the uncertainty of the input parameters affects the specific contact resistance value obtained from the fitted data.

In order to attain the error contribution of each input parameter, various fittings of one numerical simulation were carried out by varying the investigated parameter between the maximum and minimum value of its confidence range and keeping all other parameter fixed.

Half the difference between the maximum and minimum specific contact resistance values obtained from these fittings is assumed to be the error contribution of the investigated parameter

$$\Delta\rho_{cn} = \frac{\rho_{cn,max} - \rho_{cn,min}}{2}, \tag{5.16}$$

where $\Delta\rho_{cn}$ is the error contribution of a given input parameter. The values $\rho_{cn,max}$ and $\rho_{cn,min}$ are the obtained specific contact resistance values at the boundaries of the confidence range of this input parameter. The whole error is assumed to be the sum of the error contribution of all input parameters plus the error by using the analytical approximation $\Delta\rho_{c0}$:

$$\Delta\rho_c = \Delta\rho_{c0} + \Delta\rho_{c1} + \Delta\rho_{c2} + \Delta\rho_{c3} + \Delta\rho_{c4}. \tag{5.17}$$

Here, $\Delta\rho_{c1}$ is the error contribution of the wafer thickness, $\Delta\rho_{c2}$ is the error contribution of the wafer resistivity, $\Delta\rho_{c3}$ is the error contribution of the highly doped BSF region and $\Delta\rho_{c4}$ is the error contribution of the contact radius. The errors are estimated for the specific contact resistance range between 0.01 and 1.00 mΩcm² by using the numerical simulations. The confidence range of the various input parameters is taken from 5.1.1. For this confidence range of input parameters, the resulting percentage error contributions are shown in Figure 5.10 along with the percentage error of all contributions together $\Delta\rho_c$. For very small contact resistance values below 0.05 mΩcm², the relative error in the determination of $\rho_{c,rear}$ is high (about 60 %) which decays to less than 40 % for $\rho_{c,rear}$ around 0.1 mΩcm² and to less than 10 % when $\rho_{c,rear}$ is above 0.5 mΩcm². The whole relative error could be fitted with the formula shown inside the diagrams of Figure 5.10. This formula is used to determine the confidence range of the measured data in the next section.

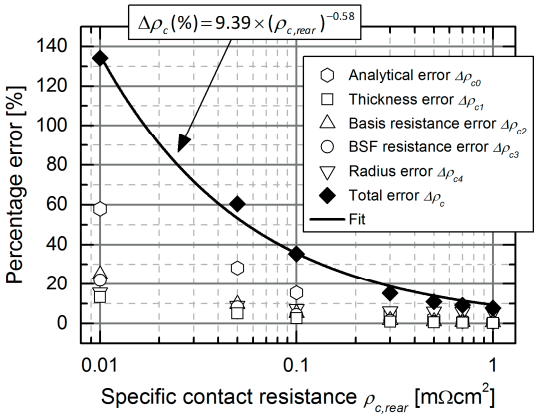

Figure 5.10: Uncertainty analysis of specific contact resistance.

5.2 Specific contact resistance experimental results

In this section the experimentally determined specific contact resistance results are presented.

5.2.1 Specific contact-resistance results on lowly doped n^+-BSF

The results of the samples with the various metallization schemes on the lowly doped n^+-BSF are shown in Figure 5.11. On the left hand side the measured whole resistance of the test samples (symbols) and the analytical fittings (lines) are shown. The estimated specific contact resistance from the measured data is shown on the right hand side of Figure 5.11. The analytical fittings were carried out with equation (5.8) in order to calculate $\rho_{c,rear}$ with equation (5.11). The input parameters for the analytical fitting as well as for the error calculations are shown in Table 5.4.

Table 5.4: Wafer thickness W, wafer resistivity ρ_{bulk}, sheet resistance R_{sh}^{BSF} and surface dopant concentration N_s of the BSF profile, and contact radius r_c of the contact openings of the test samples of run 1. These values are also used for the calculation of the analytical fittings and the error range of the estimated specific contact resistance values.

W (µm)	ρ_{bulk} (Ωcm)	R_{sh}^{BSF} (Ω/sq)	N_s (cm^{-3})	r_c (µm)
158.7 ± 3.6	4.64 ± 0.25	136.1 ± 1.3	3.8×10^{19}	18 ± 0.5

The results of Figure 5.11 show that one-layer Al-Si metallization will result in a significant ohmic loss when contacting lowly doped n^+-Si. The estimated specific contact resistance value of one-layer Al-Si metallization is around 6 mΩcm² for *as-sputtered* samples and around 4 mΩcm² after annealing the samples at 400 °C for 5 min. A further annealing at 425 °C did not result in any improvement of the estimated specific contact resistance (not shown in Figure 5.11). By using Al-Si/Al stack instead of one-layer Al-Si metallization the specific contact resistance can be reduced to between 1 and 2 mΩcm² which is still too high for high efficiency solar cells with a metallization fraction area as low as 0.5 % on the rear (see Figure 2.14). A specific contact resistance value around 2 mΩcm² might result in a fill factor loss around 2 %$_{abs}$ when applied to PERT solar cells with a metallization fraction around 0.5 %. The estimated specific contact resistance of the samples with pure Al metallization on the rear is about five times lower than of Al-Si/Al metallization. The specific contact resistance values are around 0.5 mΩcm² for the *as sputtered* samples. A slight improvement to 0.4 mΩcm² could be obtained after annealing the samples at 400 °C for 5 min. This may result in a marginal fill factor loss around 0.5 %$_{abs}$ (see Figure 2.14). As expected from literature data, titanium shows the best results for contacting lowly doped n^+-Si with a specific contact resistance values around 0.15 mΩcm². Furthermore, there is no significant difference between the specific contact resistance values of as-sputtered and annealed samples which might be due to better reduction of native oxide of Ti than Al or Al-Si.

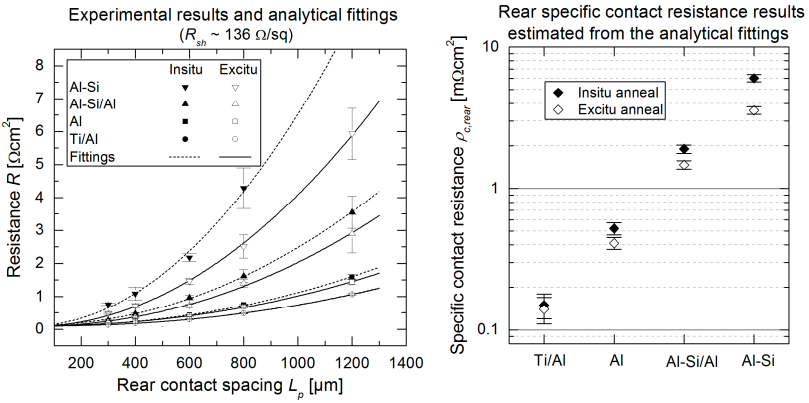

Figure 5.11: The experimental results (symbols) of the test samples and the analytical fittings (lines) are shown on the left hand side whereas the estimated specific contact values from the analytical fittings are shown on the right hand side.

5.2.2 Specific contact-resistance results on highly doped n^+-BSF

Since it was found that Al-Si/Al stack shows lower contact resistance than Al-Si in the first run, one-layer Al-Si metallization was not tested in this run. In this run only Al, Al-Si/Al and Ti/Al stack are tested on highly doped n^+-Si. The results of the test samples are shown in Figure 5.12 (as sputtered) and Figure 5.13 (annealed at 400 °C for 5 min). On the left hand side the measured whole resistance of the test samples (symbols) and the analytical fittings (lines) are shown. The estimated specific contact resistance from the measured data is shown on the right hand side of Figure 5.12 and Figure 5.13. The analytical fittings were carried out with equation (5.8) in order to calculate $\rho_{c,rear}$ with equation (5.11). The input parameters for the analytical fitting as well as for the error calculations are shown in Table 5.5.

Table 5.5: Wafer thickness W, wafer resistivity ρ_{bulk}, sheet resistance R_{sh}^{BSF} and surface dopant concentration N_s of the BSF profile, and contact radius r_c of the contact openings of the test samples of run 2. These values are also used for the calculation of the analytical fittings and the error range of the estimated specific contact resistance values.

W (µm)	ρ_{bulk} (Ωcm)	R_{sh}^{BSF} (Ω/sq)	Ns (cm^{-3})	r_c (µm)
158.7 ± 3.6	4.64 ± 0.25	75.3 ± 0.9	6.9 x 10^{19}	18 ± 0.5

The most important result of this run (highly doped n^+-BSF) is that the estimated specific contact resistance for all metallization variants is lower than the required rear specific contact resistance of nPERT solar cells with metallization fraction area as low as 0.5 %. The specific contact resistance of the samples with Ti/Al metallization is very low (less than 0.02 mΩcm²) and almost ten times lower than of the samples with Al-Si/Al metallization, but it might only bring very marginal fill factor gain, since the specific contact resistance values of all sample are below the required specific contact resistance of 0.3 mΩcm² (Figure 2.14) for fill factor loss less than 0.25 $\%_{abs}$. Furthermore, the results show that there is no significant difference between as-sputtered and annealed samples which indicates that the optimized sputtering process at high power results in a sufficient dynamic annealing for in-situ contact formation.

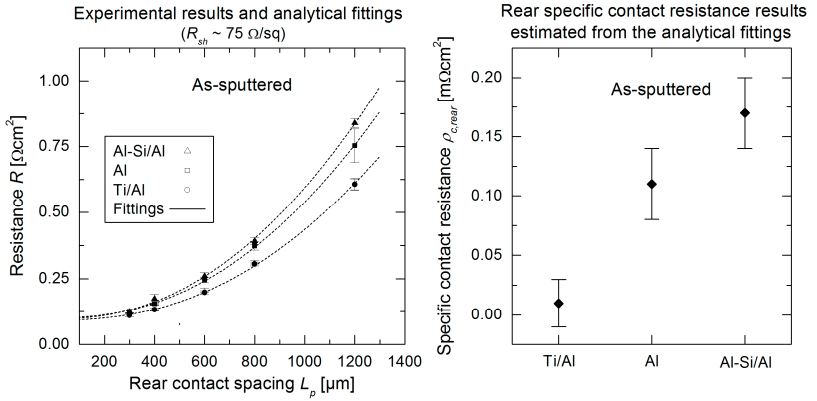

Figure 5.12: Resistance of as-sputtered contact layers (symbols) of the test samples and the analytical fittings (lines) are shown on the left hand side whereas the estimated specific contact values from the analytical fittings are shown on the right hand side.

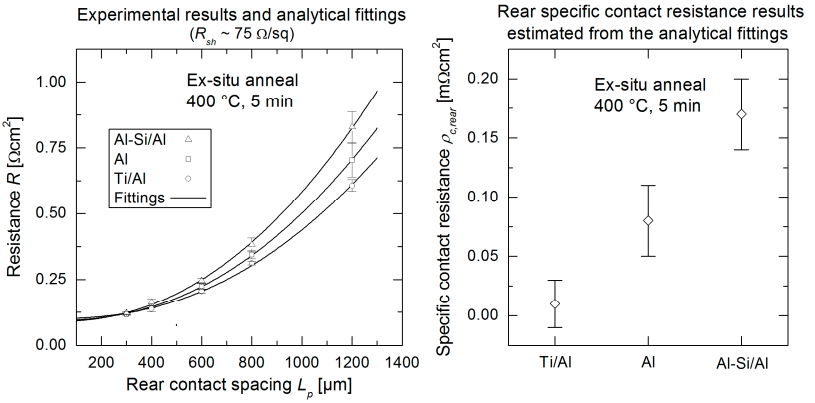

Figure 5.13: Resistance of sputtered and annealed contact layers (symbols) of the test samples and the analytical fittings (lines) are shown on the left hand side whereas the estimated specific contact values from the analytical fittings are shown on the right hand side.

5.2.3 Comparison of the experimentally obtained $\rho_{c,rear}$ data with previously published ones

Figure 5.14 shows previously published specific contact resistance data of Al/n^+-Si system (hollow symbols) [33] plotted with data obtained in this work (black symbols). These values are in the same order of previously published data for PVD-Al on n^+-Si [12]. The slight difference between the obtained results and previously published data, especially in comparison with the lowly doped BSF, might be due to the picosecond laser ablation process which is reported to reduce the doping concentration at the surface [85].

5.2.4 Summary and conclusion

In this chapter the specific contact resistance Al, Al-Si, Al-Si/Al and Ti/Al stack on n^+-doped silicon of point contacts was determined. Two doping profiles and hence surface dopant concentration were used. In order to determine the specific contact resistance of point contacts, a new characterization method was presented. An analytical model was introduced and verified with numerical device simulation. It was found that the method is applicable for specific contact resistance values > 0.01 mΩcm^2.

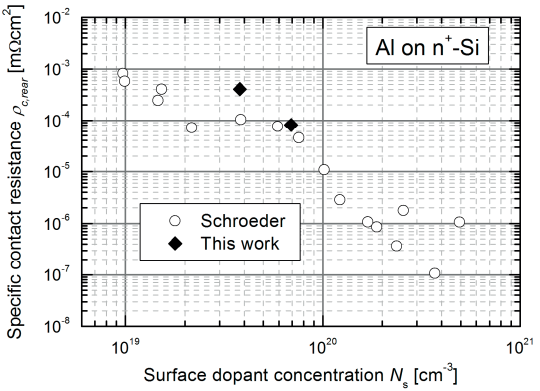

Figure 5.14: Comparison of specific contact resistance with previously published results from Schroder [33].

The experimental results of the samples with lowly doped n^+-Si with a surface dopant concentration of about 3.8×10^{19} cm^{-3} showed that one-layer Al-Si metallization will result in a very high specific contact resistance leading to a significant ohmic loss. By using Al-Si/Al stack instead of one-layer Al-Si metallization the specific contact resistance can be reduced to around 2 mΩcm^2. This may result in a fill factor loss around 2 %$_{abs}$. The estimated specific contact resistance of the samples with pure Al metallization on the rear was found to be about five times lower that of Al-Si/Al metallization with specific contact resistance values around 0.4 mΩcm^2. This may result in a marginal fill factor loss around 0.5 %$_{abs}$. Titanium showed the best results for contacting lowly doped n^+-Si with a specific contact resistance values around 0.15 mΩcm^2. Thus, for lowly doped n^+-Si, titanium as a contact layer seems to be the best choice.

The experimental results of the samples with highly doped n^+-Si with a surface dopant concentration of about 6.9×10^{19} cm^{-3} and a sheet resistance of about 75 Ω/sq (as usually applied to nPERT solar cells [36]) showed that the estimated specific contact resistance for all metallization variants is lower the required rear specific contact resistance of nPERT solar cells with metallization fraction area as low as 0.5 % (< 0.3 mΩcm^2).

Furthermore, the results of all samples showed that there is no significant difference between as-sputtered and annealed samples which indicates that the

sputtering process of aluminum at high power (14 kW) results in a sufficient dynamic annealing for in situ contact formation.

6 Detailed optical study on rear-side reflectors for nPERT solar cells

In this chapter the impact of rear-side contact-metal on the optical performance of PERT silicon solar cells is investigated. In the previous chapter it was shown that a rear-side metallization based on highly conductive metals as Al, Ag or Cu must be used for a sufficient current transport with negligible lateral resistance losses. Since Cu cannot be used as a contact-metal because it causes a degradation of cell performance when diffusing into the silicon wafer [86], it is not considered in the optical investigations of this chapter. Al-based metallization can also feature other contact metals like Al-Si or Ti for a spiking-free metal-semiconductor contact as shown in the previous chapters. Therefore, rear-side metallization schemes with Al, Al-Si, Ti or Ag as contact-metals are considered in the optical investigations of this chapter. In the literature, optical investigations on Al and Ag as rear-side metallization for SiO_2-passivated silicon solar cells are found [39], [87]. In this work, similar optical investigations are carried out and extended to other passivation layers like SiN_x as well as other metal layers like Al-Si or Ti. First, a brief overview of the optical properties of dielectric materials and metals is given. Analytical simulations regarding the back-side reflectance of PERT solar cells with textured front side and planar rear-side covered with various passivation and PVD-metallization layers follow. Based on the results of the analytical simulations, experiments and numerical ray-tracing simulations with specific test samples were carried out. The simulation and experimental results are presented and discussed. Some of the results of this chapter are published in [88].

6.1 Theoretical background

6.1.1 Optical properties of dielectric materials and metals

Since rear-side reflectors usually consist of dielectric passivation layer or layer-stack covered with metal layer or layer-stack, the optical properties of these materials will be briefly presented in this section.

- **Optical properties of passivation layers**

Dielectric materials are insulators and do not have free electrons in contrast to metals. Their optical properties are therefore determined by the interaction of the electromagnetic wave with bound electrons, atoms or impurities that are present in the material. Such absorption processes can be well described with the classical theory of dielectric materials proposed by Lorentz [89], which will be briefly explained in the following.

Under influence of an electric field, the positive charge of the atomic nucleus will be displaced against the negative charged electron cloud of the bound electrons and each atom will be represented as an electric dipole. When alternating electric field is applied, the dipole starts to oscillate and can absorb a maximal amount of energy when excited near its resonance frequency as a harmonic oscillator.

An alternating electric field $E(t)$ can be written as

$$E(t) = E_0 e^{i\omega t}, \tag{6.1}$$

where $\omega = 2\pi\nu$ and E_0 are the angular frequency and the amplitude of the electromagnetic wave.

As for harmonic oscillator, the vibration equation for the bound electron will be

$$m_e \frac{d^2x}{dt^2} + \gamma \frac{dx}{dt} + \kappa x = eE(t), \tag{6.2}$$

where e is the electron charge and m_e is the electron mass. The first term in equation (6.2) describes the acceleration by the driving force $eE(t)$, the second term the damping of the oscillator, where γ is the damping parameter. The third term describes the binding strength between the atom and the electron, where the factor κ is the spring constant.

Based on equation (6.2), the optical constants ε_1 and ε_2 and thus the refraction index n and the extinction coefficient k for multiple absorption process of the

material can be obtained[3] as a function of the frequency of the electromagnetic wave ν (where ε_1 and ε_2 are the real and imaginary parts of the relative permittivity ε_r of the material)

$$\begin{aligned}\varepsilon_1 &= n^2 - k^2 \\ &= 1 + \frac{e^2 m_e N_a}{\varepsilon_0} \sum_i \frac{f_i({\upsilon_{0i}}^2 - \upsilon^2)}{4\pi^2 {m_e}^2 ({\upsilon_{0i}}^2 - \upsilon^2)^2 + {\gamma_i}^2 \upsilon^2},\end{aligned} \tag{6.3}$$

$$\varepsilon_1 = 2nk = \frac{e^2 N_a}{2\pi\varepsilon_0} \sum_i \frac{f_i \gamma_i \upsilon}{4\pi^2 {m_e}^2 ({\upsilon_{0i}}^2 - \upsilon^2)^2 + {\gamma_i}^2 \upsilon^2}. \tag{6.4}$$

Here, N_a is the atom density, ε_0 is the vacuum permittivity and f_i and ν_{0i} are the oscillator strength and resonance frequency of the ith oscillator.

Figure 6.1 shows experimental data of n and k for typical dielectric passivation-layers as SiO_2 and SiN_x along with a typical semiconductor passivation-layer as amorphous silicon aSi. The experimental data are shown in the spectral range between 300 and 1200 nm, where a silicon solar cell operates.

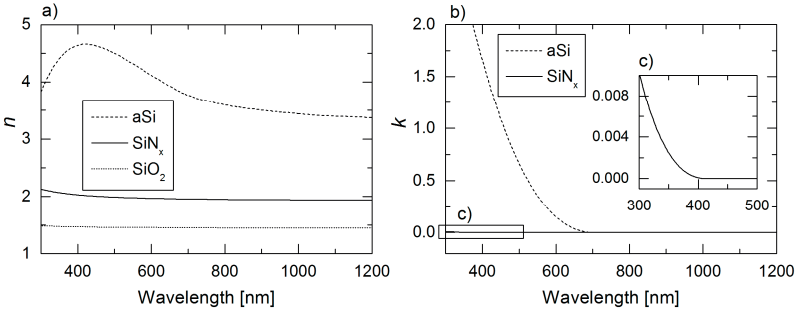

Figure 6.1: Optical constants n and k for the passivation layers aSi, SiO_2 and SiN_x used in this work.

The dispersion curves were obtained by a spectral ellipsometry measurement. There are no absorption processes for SiO_2 in this spectral range and thus the extinction coefficient $k = 0$ for SiO_2. In addition, the extinction coefficient k is also equal to zero for SiN_x and aSi in the NIR spectral range (Figure 6.1 - right).

[3] For the complete derivation it is referred to [89] pp. 238–243.

This means that all three passivation layers are transparent in the NIR spectral region. Their optical properties in the NIR spectral range differ mainly in the refractive index, which has a huge influence on the back-side reflectance of the solar cell as will be shown later in this chapter. This optical data in Figure 6.1 are used in the analytical and numerical ray-tracing simulations later in this chapter.

- **Optical properties of metals**

Metals are characterized by a high reflectivity in a spectral range below a characteristic cut-off frequency, which is called the plasma frequency. At this frequency the reflectivity of the metal drops sharply and the metal becomes transparent (when other absorption processes are not present) [91]. This characteristic reflection behavior is caused by the interaction of the electromagnetic wave with the free electrons that are present in the metal layer. The free electron density in metals is very high (10^{22} – 10^{23} cm^{-3}) and responsible for their characteristic high electrical and thermal conductivity as well as their high reflectivity. The plasma reflectivity of metals is described by the refined Drude model of free electron [89], which will be briefly explained in the following. When free electrons interact with electromagnetic waves they experience no restoring forces in contrast to bound electrons that have resonant frequencies owing to the restoring forces of the medium. Free electrons undergo only collisions in the non-ideal lattice after being accelerated by the electrical field. On average, the electrons are accelerated for a certain amount of time (damping time τ) before they undergo the next collision.

The equation of motion for a free electron under influence of an alternating electric field is therefore given by

$$m^* \frac{d^2x}{dt^2} + \frac{m^*}{\tau}\frac{dx}{dt} = eE(t), \tag{6.5}$$

where m^* is the effective mass of the free electron in the metal. The first term in equation (6.5) describes the acceleration of the free electron by the driving force $eE(t)$. Since the electron loses its momentum in time τ after being

accelerated by the electrical field, a second damping term is added to the equation of the free electron motion. There is no restoring force term in equation (6.5) in contrast to the equation of motion for bound electrons (6.2).

Based on equation (6.5), the dispersion curves of metals after considering only free electron interactions with the electromagnetic field (the so called Drude equations for the optical constants) can be obtained [89]

$$\varepsilon_1 = n^2 - k^2 = 1 - \frac{{\upsilon_p}^2}{\upsilon^2 + {\upsilon_d}^2}, \tag{6.6}$$

$$\varepsilon_2 = 2nk = \frac{\upsilon_d}{\upsilon}\frac{{\upsilon_p}^2}{\left(\upsilon^2 + {\upsilon_d}^2\right)}. \tag{6.7}$$

The characteristic frequencies ν_p and ν_d are the plasma and the damping frequencies respectively and defined as follows

$$\upsilon_p = \sqrt{\frac{e^2 N}{4\pi^2 \varepsilon_0 m^*}}, \tag{6.8}$$

$$\upsilon_p = \frac{2\pi\varepsilon_0 {\upsilon_p}^2}{\sigma_0} = 2\pi\varepsilon_0 {\upsilon_p}^2 \rho_0. \tag{6.9}$$

Free electron density N in the range $10^{22} – 10^{23}$ cm^{-3}, as typical for metals, leads to plasma frequencies in the ultraviolet spectral region. The damping frequency ν_d (i.e. the reciprocal of the damping time τ) is indirect proportional to the electrical conductivity σ_0. This means that high conductive metals have lower values of the absorption dielectric constant ε_2 and thus are less absorbing and higher reflective than low conductive ones.

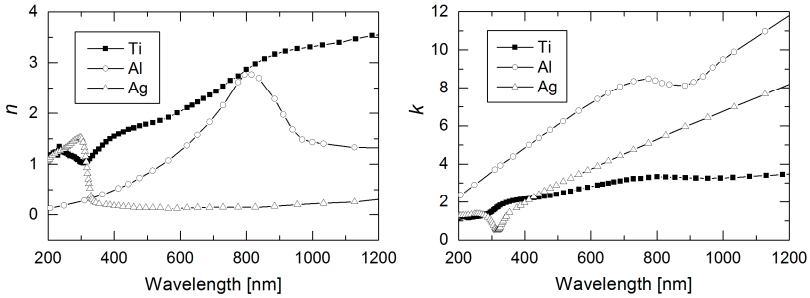

Figure 6.2: Optical constants n and k for Ti, Al and Ag (data from [90]).

The plasma reflectivity gives information about the highest possible reflectivity of the metal for $\lambda > \lambda_p$[4]. Metals can also absorb light at certain resonance frequencies as dielectric or semiconductor materials, which is related to light interaction with bound electrons, atoms or impurities that are present in the metal layer. These interactions lead to a reduction of the reflectivity of the metal in the high reflective spectral region. The classical theory of dielectric materials by Lorentz, which is briefly explained at the beginning of this section, can be also applied to metals to describe these optical processes. The contribution of both free as well as bound electrons, atoms or impurities on the optical constants of the metal can be obtained by simply adding Drude equations (6.6) and (6.7) to Lorentz equations (6.3) and (6.4), which results in the Lorentz-Drude model for optical constants in metals [89]. Experimental data of the optical constants *n* and *k* for Ti, Al and Ag is shown in Figure 6.2 (data obtained from [90]). This data includes the contribution of both free as well as bound electrons, atoms or impurities and are used in all analytical and numerical simulations in this work. To show the characteristic optical behavior of metals, the reflectivity of Al, Ag and Ti was calculated by applying the optical constants of Figure 6.2 in the following Beer equation

$$R = \frac{(n-1)^2 + k^2}{(n+1)^2 + k^2}. \tag{6.10}$$

[4] λ_p is the wavelength of incident electromagnetic wave corresponding the plasma frequency ν_p.

The calculated reflectivity of the various metals is shown in Figure 6.3 (symbols) along with the plasma reflectivity (the contribution of free electrons only – solid lines).

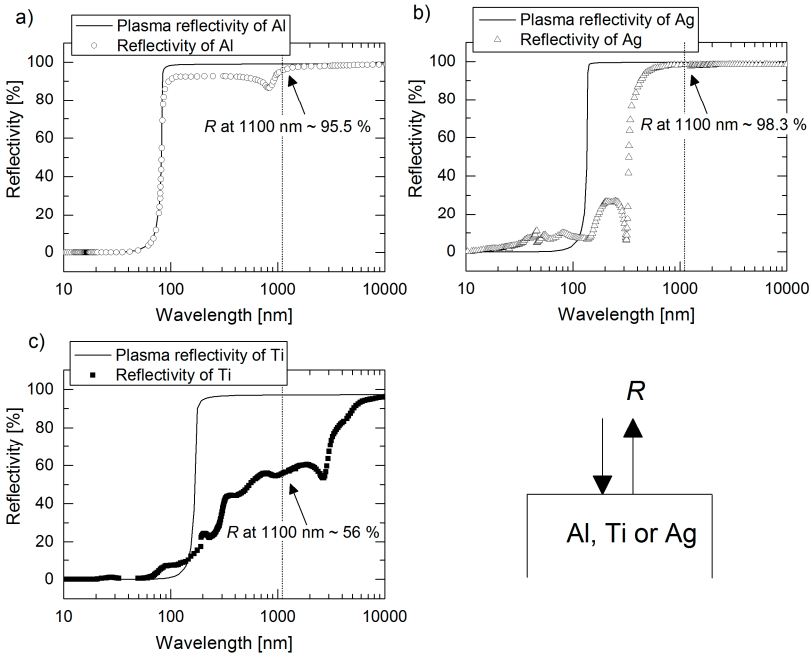

Figure 6.3: Reflectivity and plasma reflectivity (contribution of only free electrons) of perpendicular incident light for Al, Ag and Ti. The perpendicular reflectivity is calculated using optical constants data taken from [90].

The plasma reflectivity was also calculated with Beer equation (6.10) by using the optical constants n and k obtained by equations (6.6) and (6.7). Qualitatively, all three metals show the characteristic reflection behavior of metals (highly reflective at $\lambda > \lambda_p$ and transparent for $\lambda < \lambda_p$), as can be seen in Figure 6.3. Quantitatively, however, there are considerable differences. Silver shows the highest reflectivity in the visible and infrared spectral region where the spectral dependence of the reflectivity has the characteristic curve shape of the plasma reflectivity (free electron contribution). Silver has also the highest plasma reflectivity due to its highest electrical conductivity. In the ultraviolet spectral

region the reflectivity of silver drops, however at $\lambda > \lambda_p$, which is related to interband electronic transitions (silver has an interband absorption edge around 310 nm [92]). The reflectivity of aluminum is slightly lower than of silver at $\lambda > \lambda_p$ with a characteristic dip around 800 nm, which is also related to interband electronic transition [92]. The incompletely filled 3d bands of the transition metal titanium can trigger interband optical absorption at small energies [91], which is responsible for the significantly lower reflectivity than silver and aluminum in the spectral region $\lambda > \lambda_p$. The reflectivity of titanium reaches high values at wavelengths beyond the long-wavelength infrared spectral region LW-IR ($\lambda > 8$ μm), exceeding, however, the wavelength of the photons reaching the rear side of the cell (see Figure 2.15). Thus, using titanium as a rear side contact metal on silicon solar cells might result in non-negligible efficiency-losses due to its low reflectivity in the near infrared spectral region. The impact of the reflectivity of the rear side contact metal on the cell performance is investigated in detail by simulations and verified by experiments in the following sections.

6.1.2 Light paths for PERT solar cell with regular upright pyramids and frustrated total reflection

PERT solar cells have a textured front side (as in industrial solar cells) and a planar rear side. Industrial silicon solar cells are usually chemically textured by anisotropic etching of the silicon surface with inorganic alkaline solutions [93]. This etching process leads to the formation of random upright pyramids in contrast to high efficiency labor PERT solar cells with inverted pyramids structured by KOH etch and lithographically defined masks [3]. The textured front side with anti-reflection coating (usually 70 - 75 nm SiN_x) reduces the front-side reflection in order that more light can be absorbed in the cell [94]. The pyramidal texture of the front side has also an influence on the paths of the light reaching the rear side [39]. Depending on the front surface texturing, the transmitted light through the cell will internally hit the rear surface at different angle of incidents.

The paths of transmitted light followed by rays reflected at the front surface of the solar cell with regular upright pyramids are calculated by geometrical analysis and shown schematically in Figure 6.4. The possible refracted beams are A_n, B_n

and C_n are shown schematically in Figure 6.4. Beams A_n are the beams entering the cell from the first reflection, B_n from the second reflection, and C_n from the third reflection. The index (1) is for beams refracted directly to the rear side and index (2) is for beams with a further internal front side reflectance before being transmitted towards the rear side.

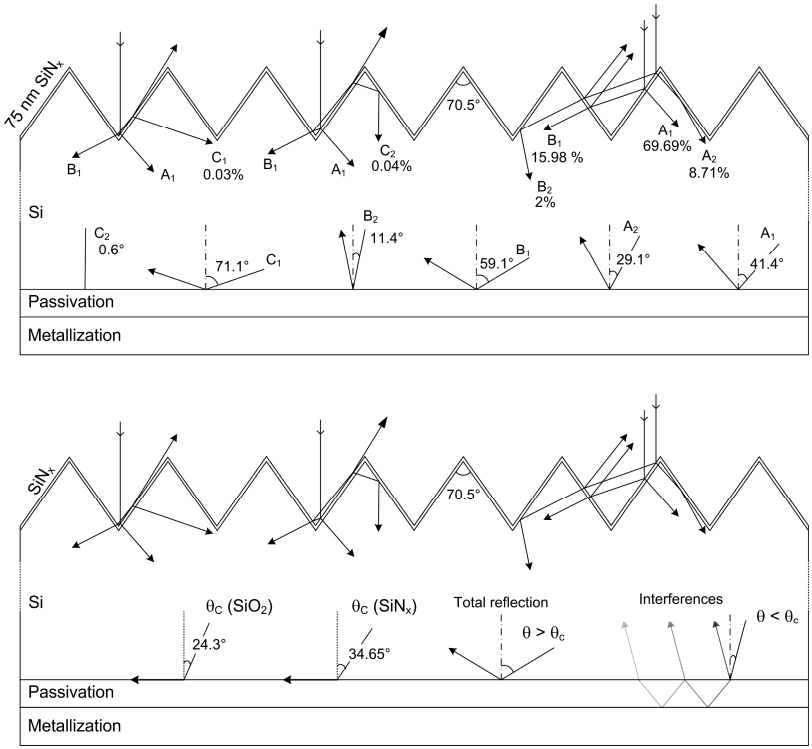

Figure 6.4: Sketch of rear-side passivated silicon solar cell with regular upright pyramids showing the possible light paths in the cell for perpendicular incident light.

It can be seen from Figure 6.4 that the transmitted rays hit the rear surface at angles of incident ranging from very narrow angle of 0.6 ° to flat angle of 71.1 ° with respect to the surface normal. Due to the higher refractive index of silicon at NIR wavelengths (n_{Si} ~ 3.52 at 1100 nm) compared to the refractive index of common passivation layers like SiO_2 (n_{SiO2} ~ 1.45 at 1100 nm) or SiN_x

(n_{SiNx} ~ 1.94 at 1100 nm), the rays hitting the rear surface with angles wider than the critical angle will be totally reflected. Total reflection occurs where electromagnetic wave is reflected from a dense optical medium like silicon into a less optical dense medium like SiO_2 or SiN_x if the angle of incident light is greater than the critical angle. The critical angle θ_c can be obtained from Snell's Law by setting the refraction angle equal to 90° [95]

$$\theta_c = \arctan\frac{n_2}{n_1}, \tag{6.11}$$

where n_1 is the refractive index of the optical denser medium ($n_1 > n_2$). By using equation (6.11) the critical angle for the transition Si to SiN_x and to SiO_2 can be obtained. The critical angle for the transition Si to SiN_x is thus 34.7° and for transition Si to SiO_2 is 24.3°. Therefore, a higher fraction of transmitted rays will be internally totally reflected at the rear surface in the case of SiO_2 passivation.

The fractions of transmitted rays at wavelength of 1100 nm for regular upright pyramids coated with 75 nm SiN_x front-side passivation are also presented in Figure 6.4. The majority of transmitted light (97.88 %) reaches the rear surface with an angle of incident greater than the critical angle for SiO_2 rear side passivation and will be therefore totally internally reflected at the first bounce. In the case of SiN_x rear side passivation only 88.85 % of transmitted light will be totally reflected at the first bounce due to the wider critical angle. That means that about 9 % more transmitted rays will travel towards the rear side metallization, and experience absorption losses in the metal layer, for SiN_x than for SiO_2 rear side passivation. For narrow angles of incident smaller than the critical angle, interference effects take place which will be discussed in section 6.1.3.

Depending on the wavelength of incident light, on angle of incident, and on the thickness of rear side passivation, totally internally reflected rays can also experience absorption losses in the passivation or in the metal layer. This effect is known as Frustrated Total Internal Reflection (FTIR) or optical tunneling [96], [97], [98]. Totally reflected light at the interface between two media

generates a non-transverse evanescent wave along the optical surface that penetrates into the optical thinner medium. The density of the evanescence wave decays exponentially with increasing distance normal to the optical interface. The energy-flow through the boundary into the second medium is in average a zero net flow [96]. This means that if the passivation layer does not absorb light at the given wavelength, the incident light will be totally reflected and no optical losses occur. Otherwise, if there are absorption processes in the passivation layer at the wavelength of incident light, the reflected beam will lose some of its intensity and the total internal reflection will be frustrated. In addition, the total internal reflection can also be frustrated at the interface between the passivation and metallization if the thickness of the passivation layer is less than the depth length of the evanescence wave. The exponential decay of the intensity of the evanescent wave can be written as [99]

$$I_{ev} = I_0 e^{-\frac{d}{d_p}}, \tag{6.12}$$

where d is the distance normal to the optical interface, d_p is the penetration depth, and I_0 is the intensity at the interface ($d = 0$). The penetration depth d_p is the distance at which the intensity of evanescence wave decays to 1/e of I_0 and is given by

$$d_p = \frac{\lambda}{2\pi n_1 \sqrt{\sin^2\theta - \left(\frac{n_2}{n_1}\right)^2}}. \tag{6.13}$$

Here, n_1 is the refractive index of the optically denser first medium, n_2 the refractive index of the optically thinner second medium, λ is the wavelength of the transmitted electromagnetic wave, and θ is the angle of incidence.

The intensity-decay of the evanescence wave in the rear-side passivation for the transition Si to SiO_2 and to SiN_x for various angles of incidence is calculated using equations (6.12) and (6.13). The results are shown in Figure 6.5. For angles of incident slightly above the critical angle (θ_c + 0.5°) the intensity of the

evanescence wave decays to a negligible value (below 5% of the original intensity) at thicknesses around 1800 nm. The depth length is reduced to ~ 500 nm for angles of incident $\theta = \theta_c + 5°$. The depth length of the evanescence wave decreases further with increasing angle of incident to less than 200 nm for wider angles of incident. In other words, if the thickness of the passivation layer is not sufficiently thick for a certain angle of incident, the totally reflected beam will be frustrated by the rear side metallization because less intensity will be reflected due to the absorption losses of the evanescence wave in the metal layer. In this case the internal reflectance will be decreased which is referred to frustrated internal total reflection. Furthermore, due to the lower refractive index and hence smaller critical angle of SiO_2, the needed thickness for sufficiently high internal total reflection is lower for SiO_2 than for SiN_x at the same angle of incidence (Figure 6.5 right). For an example, this thickness is around 500 nm for SiN_x and 300 nm for SiO_2 at angle of incidence of 40 °. At θ = 60 °, around 230 nm SiN_x and 190 nm SiO_2 is needed for undisturbed total reflection.

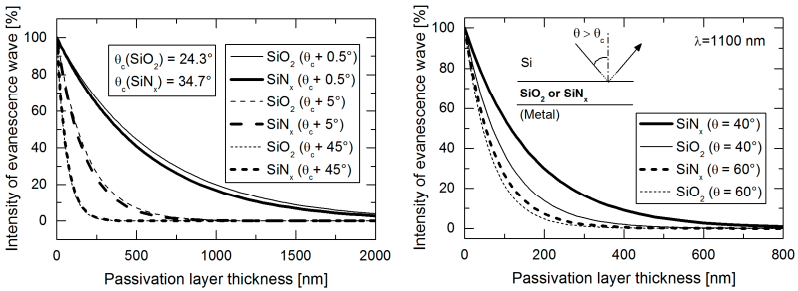

Figure 6.5: The intensity of evanescence wave as a function of passivation layer thickness and angle of incident light while being internally reflected at the rear-side of the solar cell.

In the following section the back-side reflectance dependence of angle of incident light and passivation layer thickness for various rear side reflectors is calculated using the matrix method.

6.1.3 Reflectance of silicon/passivation/metallization-system calculated with the matrix method

The matrix method is widely used to calculate the reflectance or transmission of optical thin films for optoelectronic devices or solar cells [100]. For solar cells applications, it can be employed to develop and optimize anti-reflection coatings, rear side reflectors or in general light trapping [101], [51]. Campbell et al. [87] calculated the reflectance of the back-side of silicon solar cells with planar rear side for various angles of incident for SiO_2/Al rear-side reflector. Since the solar cells developed in this work feature SiN_x rear side passivation, the reflectance is calculated for SiN_x, SiO_2 as well as for multi-layer-stack SiN_x/SiO_2 rear-side passivation. In addition, in order to investigate the impact of rear-side metallization on the internal reflectance of the solar cells, rear-side reflectors featuring Ti and Ag are also considered in the calculations and compared to Al rear-side metallization.

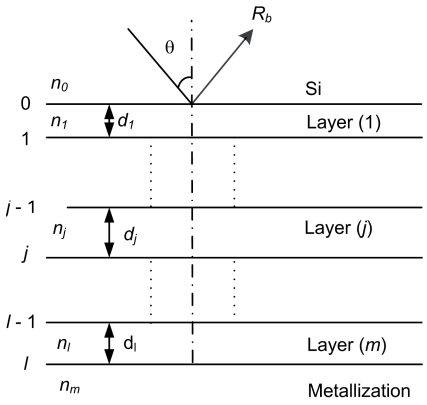

Figure 6.6: Sketch of multi-layer stack of l dielectric layers sandwiched between two semi-infinite materials (silicon and metallization) which is used in the matrix method of the calculation of the reflectance at the rear-side of the solar cell.

A stack of (l) passivation layers deposited between two semi-infinite mediums, here the silicon substrate and rear side metallization (see Figure 6.6), is characterized with an equivalent matrix M_{eq} equals to the product Π_j of matrices associated with each layer:

$$M_{eq} = \begin{pmatrix} M_{11} & iM_{12} \\ iM_{21} & M_{22} \end{pmatrix} = \prod_{j=1}^{l} \begin{pmatrix} \cos\varphi_j & \frac{i}{n_j^{eff}}\sin\varphi_j \\ in_j^{eff}\sin\varphi_j & \cos\varphi_j \end{pmatrix} \quad (6.14)$$

with

$$\varphi_j = \frac{2\pi}{\lambda} n_j \quad \text{and} \quad i^2 = -1. \quad (6.15)$$

Here, φ_j is the phase shift, n_j is the refractive index, and n_j^{eff} is the effective refractive index of the jth layer where

$$n_j^{eff} = n_j \cos\theta_j \quad (6.16)$$

for parallel polarized light and

$$n_j^{eff} = \frac{n_j}{\cos\theta_j} \quad (6.17)$$

for perpendicular polarization.

The reflectance of parallel polarized light $R_p = r_p \cdot r_p^*$ and perpendicular polarized light $R_s = r_s \cdot r_s^*$ can be obtained from the amplitude reflection factor

$$r = \frac{n_{Si}M_{11} - n_m M_{22} + i(n_{Si}n_m M_{12} - M_{21})}{n_{Si}M_{11} + n_m M_{22} + i(n_{Si}n_m M_{12} + M_{21})}, \quad (6.18)$$

where r^* is the complex conjugate of r.

The reflectance R for unpolarized light is the average of both parallel and perpendicular reflectance

$$R = \frac{R_p + R_s}{2}. \tag{6.19}$$

Figure 6.7 shows the calculated reflectance of NIR-light at 1100 nm wavelength by the matrix method for SiO_2/Al and SiN_x/Al rear-side reflectors. The reflectance was calculated for various passivation layer thicknesses and angles of incident. Two optical effects can be observed in the curve shapes of the calculated internal reflectance: frustrated internal total reflection and interferences.

If the angle of incidence is wider than the critical angle, internal total reflection occurs. As shown in the previous section 6.1.2, the internal total reflection will be frustrated (i.e. $R < 100$ %) by the absorbing metal layer if the thickness of the passivation layer is not sufficiently thick due to the propagation of an evanescence wave during reflection. The reflectance increases with increasing passivation layer-thickness and reaches ~ 100 % at thicknesses around the penetration depth of the evanescence wave, so that the reflected wave is not disturbed (frustrated) by the absorbing metal layer. Furthermore, the penetration depth decreases with increasing angle of incident and is higher for SiN_x due to the higher refractive index (Figure 6.5). This explains the reflectance curves in Figure 6.7 for angles of incident wider than the critical angle. Since 70 % of the transmitted light in a solar cell with upright pyramids hits the rear surface at angle of incident around 41° (Figure 6.4), the thickness of rear-side passivation should be around 200 nm for SiO_2 and 400 nm for SiN_x (40°-curves in Figure 6.7) in order to reflect as much as NIR-light possible back into the cell.

For narrow angles of incidence smaller than the critical angle ($\theta < 24.3°$ for SiO_2 and $\theta < 34.7°$ for SiN_x), interference effects take place. In Figure 6.4 it was shown that a non-negligible fraction of transmitted light (~ 9 %) reaches the rear surface at angle of incident of 29.1°. These beams will be totally reflected in the case of SiO_2 reaching near 100 % at thicknesses around 400 nm. For SiN_x

passivation, these beams do not show total reflection behavior and the reflectance is lower due interference effects (because $\theta < \theta_c = 34.7°$). For these rays, the thickness of the passivation must be tuned where constructive interferences occur. The reflection at angles of incident near the critical angle is in general low because the light will travel almost parallel to the metal layer and can suffer more absorption losses there [87].

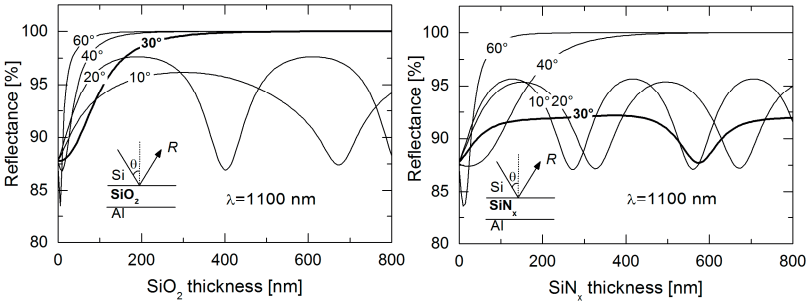

Figure 6.7: The reflectance results of SiO_2/Al (left) and SiN_x/Al (right) reflectors for various angles of incident light (at 1100 nm) calculated with the matrix method.

The enhancement of the back-side reflectance of solar cells with SiN_x rear-side passivation can be done either by increase the thickness of SiN_x to some hundreds nanometers or by deposition of a SiO_2 cap-layer on the SiN_x passivating layer. Figure 6.8 shows the calculated reflectance for SiN_x/SiO_2/Al back-side reflector with 70 nm SiN_x (as usually used in silicon solar cells) and varying SiO_2 layer-thickness. The reflectance improves for all angles of incidence in comparison to only SiN_x passivation, especially for the 30°-curve which shows a total reflection behavior after adding a SiO_2 upon the SiN_x passivation rather than interference effects with low reflectance as for only SiN_x passivation (Figure 6.7).

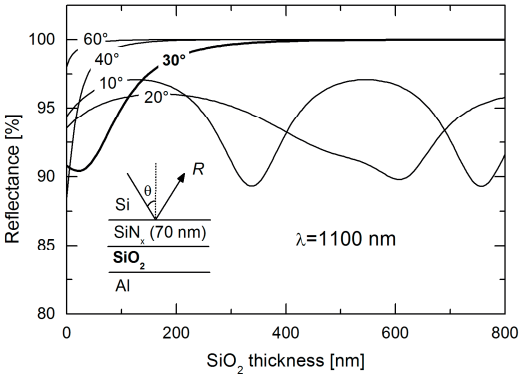

Figure 6.8: The reflectance results of $SiN_x/SiO_2/Al$ reflector for various angles of incident light (at 1100 nm) calculated with the matrix method.

To study the impact of rear side metallization on the reflectance of the back-side, the reflectance is also calculated for Ag and Ti rear side metallization with SiN_x/SiO_2 passivation-stack. The results are shown in Figure 6.9. The impact of the high NIR-reflectivity of Ag and Al and of the poor NIR-reflectivity of Ti can be clearly seen in the calculated reflectance curves at wavelength of 1100 nm for SiN_x/SiO_2 rear-side passivation. For angles of incident where total reflection occurs (30°-, 40°-, and 60°-curves), a thicker SiO_2 layer is needed for Ti than for Ag or Al rear side metallization to overcome frustrated total internal reflectance losses and reach reflectance values as high as 100%. For narrow angles of incident, where interference effects take place (e.g. at 10°), the poor reflectivity of Ti can be overcome only to some extent (from about 50% to 65%) by thickening the passivation layers to values where constructive interferences occur (e.g. 70 nm SiN_x / 120 nm SiO_2 in the case of SiN_x / SiO_2 double stack passivation).

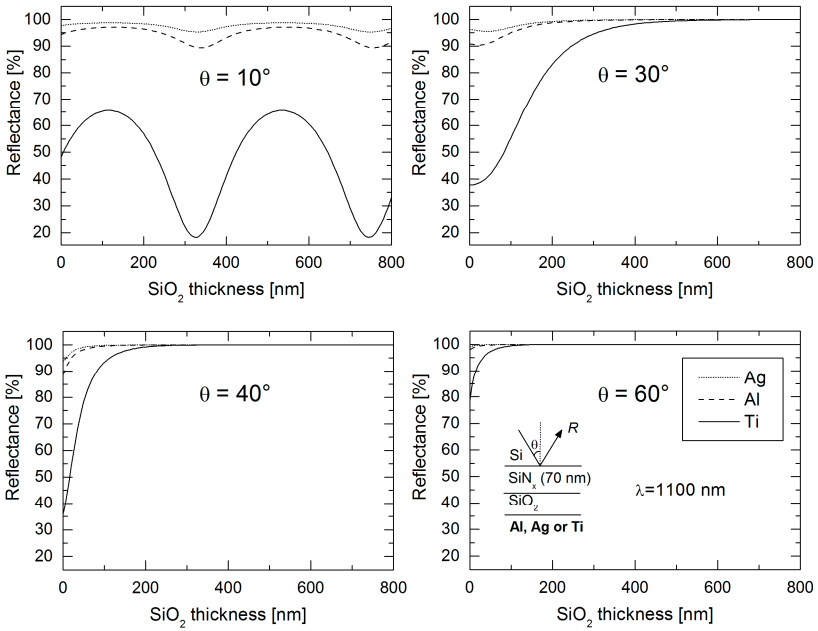

Figure 6.9: The reflectance results of various rear-side reflectors (Ag, Al and Ti) with SiN_x/SiO_2 passivation for various angles of incident light (at 1100 nm) calculated with the matrix method.

The low internal reflectance for narrow angles of incident can be enhanced by using a more sophisticated multi-layer stack (e.g. Bragg-stack). A Bragg-stack consists of dielectric layers with alternating low-high refractive index and a quarter wavelength optical-thickness (λ/4-thickness) between the silicon wafer and the last layer with low-refractive index prior to the metallization (Figure 6.10).

In order to find the optimal layer-thicknesses of a Bragg-stack with SiO_2 as low-n and aSi or SiN_x as high-n materials, the reflectance of a triple Bragg-stack with varying layer thicknesses was calculated using the matrix method for wavelength of 1100 nm and angle of incident of 10° (Figure 6.11). The first constructive interferences occur at about 200 nm for SiO_2, 80 nm for aSi (Figure 6.11, left) and 140 nm for SiN_x (Figure 6.11, right), which are the λ/4-thicknesses for 1100 nm wavelength at 10°. The reflectance at 10° of rear-

side reflector with Ti-metallization can be improved to over 90% by using triple Bragg-stack with aSi as high-n material and to around 80% by using SiN_x as high-n material. This means that the reflectance is higher for larger difference between the low- and high-n materials.

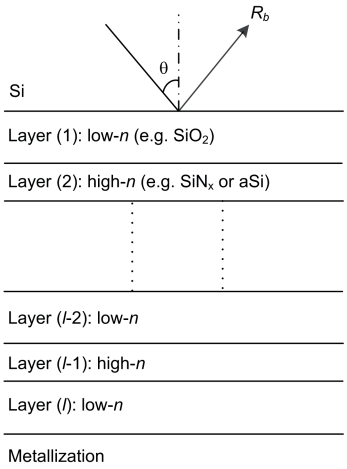

Figure 6.10: Sketch of multi-layer Bragg-stack. A Bragg-stack consists of dielectric layers with alternating low-high refractive index and a quarter wavelength optical-thickness (λ/4-thickness) between the silicon wafer and the last layer with low-refractive index prior to the metallization.

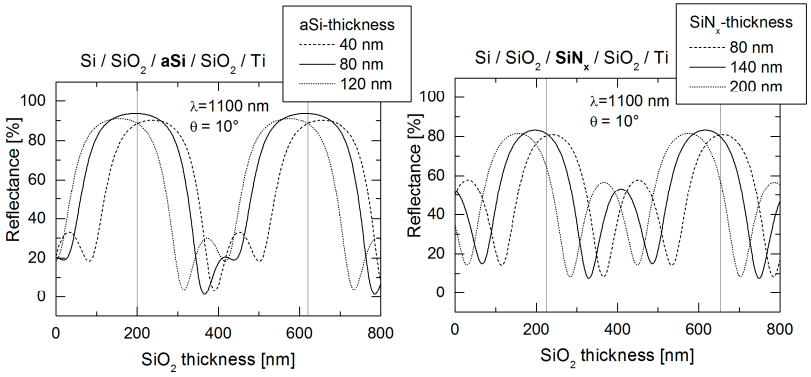

Figure 6.11: The reflectance results of Ti-reflectors with triple-layer Bragg-stack for an angle of incident of 10 ° and wavelength of 1100 nm calculated with the matrix method.

The reflectance can be further improved by using Bragg-stack of higher order (e.g. quintuple or septuple instead of triple stack). The results of triple, quintuple, and septuple Bragg-stack for aSi and SiN_x as high n-material and SiO_2 as low-n material are shown along with single and double layer rear-side passivation in Figure 6.12.

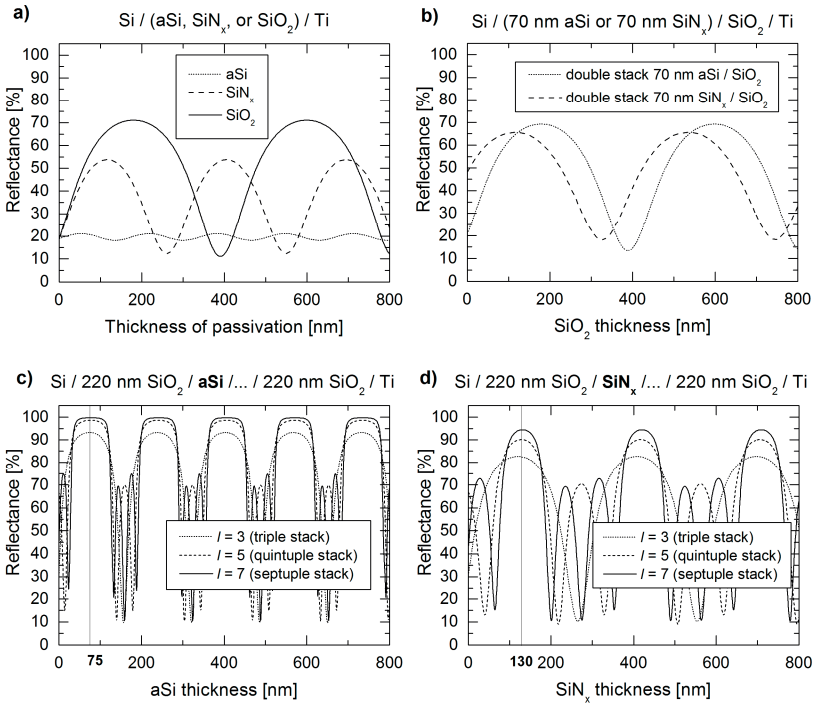

Figure 6.12: The reflectance results of Ti-reflectors with various rear-side passivation schemes for angle of incident of 10 ° and wavelength of 1100 nm calculated with the matrix method. The various rear-side passivation schemes are: single layer passivation (a), double-layer passivation (b), triple, quintuple and septuple Bragg-stack with aSi as a high-n material (c) and SiN_x as high-n material (d).

The reflectance of rear-side reflector with Ti-metallization and aSi as high-n material can be improved to near 100% by using Bragg-stack of order five or higher. This means that the poor reflectivity of Ti might be overcome by using multiple Bragg-stacks if Ti is needed in a specific application due to its superior

contacting properties. Unfortunately, multi-layer stacks are barely implementable for industrial solar cells but might be beneficial for thin solar cells or for achieving very high efficiency laboratory solar cells. For standard industrial solar cells with silicon wafers thicker than 150 µm, the use of a second capping low-n material as SiO_2 can be applied to enhance the reflectance and hence the current generation for SiN_x, aSi or other commonly used passivation layer like Al_2O_3 or SiC (Figure 6.12-b). Since the focus of this work is 150-µm-thick industrial solar cells, Bragg stack of order higher than three are not tested experimentally. These results will be further investigated and confirmed with device-simulations and experiments in the following sections.

6.2 Numerical 3D-device-simulations and experiments on reflection samples

In order to study the impact of different rear-side passivation and metallization layers on the internal back-side reflectance R_b and the generated photocurrent density J_{pb}, numerical ray-tracing simulations using Synopsys TCAD Sentaurus Device [35] and experiments on reflection samples were performed.

Figure 6.13 shows the ray-tracing simulation and experimental approach of the optical investigations of the various rear-side configurations. For these investigations, 150 µm thick *p*-type Cz-silicon wafers with textured front side covered with about 70 nm SiN_x antireflection coating and planar rear side with various passivation and metallization layers were used. The reflection samples do not feature any highly doped regions in order to eliminate the contribution of free carrier absorption [102]. The front-surface of the samples is chemically textured by anisotropic etching in KOH/IPA solution and the rear surface is chemically polished in KOH or HNO_3 solution, which are commonly used processes for industrial solar cell manufacturing. These processes lead to the formation of random upright pyramids on the front and a rough planar surface on the rear side of the experimental samples in contrast to regular upright pyramids on the front and smooth plane surface assumed on the back of the simulated devices. For the simulated devices, a 150 µm thick symmetry element consisting of a quarter of an upright pyramid and a planar rear side was used. By neglecting the roughness of the rear side of the simulated devices, the

simulations overestimate the fraction of the rays which escape after the first internal reflection at the rear through the front of the simulated samples in comparison to the real samples. Therefore the simulated generated photocurrent should underestimate the photocurrents of the real samples.

The planar rear-side is covered with single-, double- or multi-layer passivation of the dielectric materials SiN_x, aSi or SiO_2 of various thicknesses covered with single-layer or multi-layer metallization of the metals Al, Al-Si, Ti, or Ag. For the experimental samples, the SOLARIS 6 multi-layer deposition system was used to sputter the various metal layers. The optical properties and thicknesses of the various passivation layers were measured by ellipsometry.

The experimental reflection samples were characterized by measuring the whole reflection spectrum of the sample using a Perkin-Elmer reflectometer and then determining the rear-side reflectance by fitting of the measured reflection-spectra with PC1D simulation. For the 3D-device-simulations, the generated photocurrent-density of the device was simulated. In these simulations, the transfer matrix method introduced in section 6.1.3 was applied to simulate the various rear-side configurations.

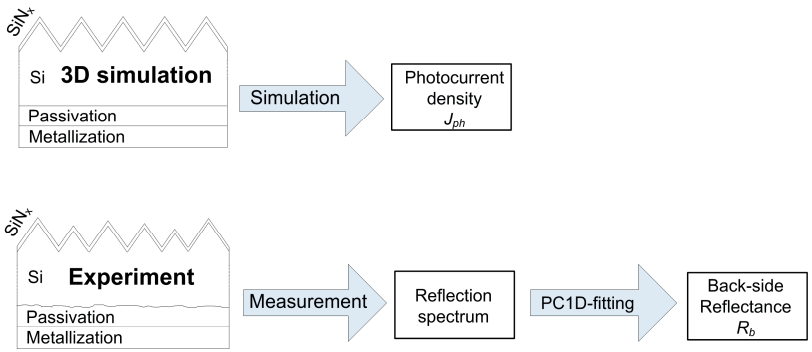

Figure 6.13: Ray-tracing 3D simulation and experimental approach used in this work in order to study the impact of various rear-side reflectors on the optical performance of PERT silicon solar cells.

In the following sections the impact of the rear-side passivation and metallization on the optical performance of the reflection samples is investigated in detail. First, single and double layer passivation combined with Al

metallization is investigated. Afterwards, pure PVD-Al-metallization is compared with Ti-, Ag- and Al-Si-based metallization schemes to study the impact of poor reflective metals as Ti and very high reflective as Ag on the optical performance of the samples.

6.2.1 One-layer Al-metallization with various passivation configurations

In this section the impact of the refractive index and thickness of the rear-side passivation on the optical performance of the reflection samples is first studied with the widely used PVD-Al metallization. Afterwards, Si enriched Al (Al-Si) is compared with Al on reflection samples with optimized rear-side passivation.

- **Ray-tracing simulation results**

The ray-tracing simulation results of Al-metallization on a single-layer passivation with various refractive indices (SiN_x or SiO_2) and various thicknesses are shown in Figure 6.14 (left).

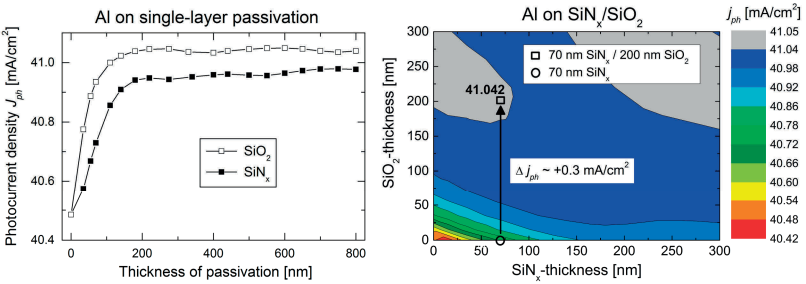

Figure 6.14: Calculation of generated photocurrent density of a symmetry element with Al-metallization on single-layer SiN_x or SiO_2 passivation (left) and on double-layer SiN_x/SiO_2 passivation (right) of various thicknesses obtained by ray-tracing simulation Synopsys TCAD Sentaurus Device.

The generated photocurrent density of a symmetry element with SiO_2 passivation (hollow symbols) is higher than with SiN_x-passivation (filled symbols), which is mainly due to higher fraction of totally internally reflected light. As shown in the previous sections 6.1.2 and 6.1.3, the fraction of transmitted light which will be totally internally reflected at the rear side is about 10 % higher for SiO_2 than for SiN_x passivation, due to the lower refractive index

of SiO_2 and thus smaller critical angle. Furthermore, the thickness-dependence of frustrated total internal reflection shown in Figure 6.5 is also observed in the photocurrent density results. The generated photocurrent increases with increasing thickness of the passivation layer and saturates at a thickness around 200 nm for SiO_2 and 400 nm for SiN_x. These thicknesses correlate very well with the optimal thicknesses obtained from the 40°-curves in Figure 6.7 (remember that about 70% of the transmitted light will be hit the rear side with an angle of incident of 41.4 °, Figure 6.4).

In addition, the ray-tracing simulation results show that interference effects have only a minor influence on the generated photocurrent density. The weak peaks of the photocurrent values at thicknesses around 220 and 550 nm for SiO_2 passivation and at thicknesses around 400 and 700 for SiN_x passivation are due interference effects of the reflected rays at the back side with narrow angles of incident (where no total internal reflection occurs). This low influence of interference effects on the generated photocurrent is due to the fact that the majority of rays reach the rear side at angles of incident wider than the critical angle (about 90.44 % for SiN_x and 99.74 % for SiO_2, see Figure 6.4). The optimal thickness of the passivation layer, where both total internal reflection as well as interference effects are taken into account, is thus at least around 220 nm for SiO_2 and 400 nm for SiN_x.

The ray-tracing simulation results of double-layer SiN_x/SiO_2 passivation-stack are shown in Figure 6.14 (right). The results show that the back-side reflectance of solar cells with SiN_x rear-side passivation can also be enhanced by adding a capping low-refractive-index material as SiO_2 instead of increasing the thickness of SiN_x, as predicted by the analytical simulation results of Figure 6.8. For instance, by adding a SiO_2 layer of thickness higher than 100 nm on the widely used 70 nm SiN_x rear-side passivation, a gain in the generated photocurrent density of more than 0.2 mA/cm^2 can be obtained, which cannot be reached by only thickening the SiN_x-layer.

- **Experimental results**

The experimental results of the reflection samples with Al rear-side metallization are in a very good agreement with the ray-tracing simulation results shown in Figure 6.14. The reflection spectra and the back-reflectance values of the test samples with Al rear-side metallization and single-layer passivation are shown in Figure 6.15. The back-side reflectance increases with increasing the thickness of the passivation layer and is higher for SiO_2-passivation. Furthermore, the rear-side reflectance of 210 nm SiO_2 rear-side passivation is slightly higher than 420 nm due to constructive interferences for 210 and destructive for 420 nm, which correlates very well with the simulation results.

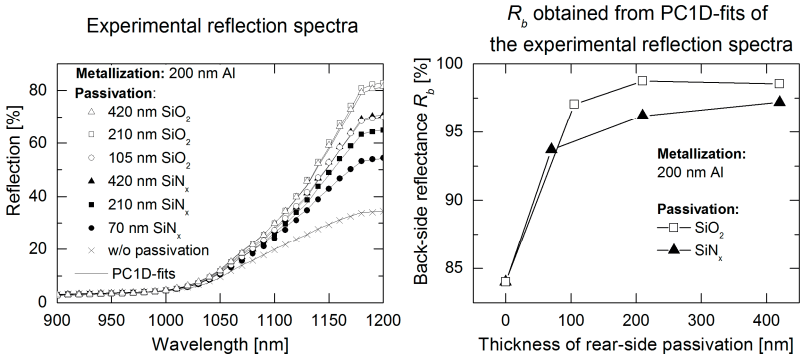

Figure 6.15: Experimental results of the reflection samples with Al rear-side metallization and single layer passivation (SiN_x or SiO_2).

The experimental results of SiN_x/SiO_2-stack are shown in Figure 6.16 along with the results of single layer passivation. As expected from the simulation results, by adding a SiO_2 capping-layer the rear-side reflectance of SiN_x-passivated samples could be enhanced to the level of only SiO_2 rear-side passivation. By doing so, the rear-side reflectance can be enhanced from about 93.6 to more 98.8 $\%_{abs}$. This would result in a gain in short-circuit current density of 0.3 - 0.35 mA/cm² according to (2.31).

The impact of using a capping SiO_2-layer on the whole performance of nPERT solar cells with SiN_x-passivated rear-side will be tested in Chapter 8.

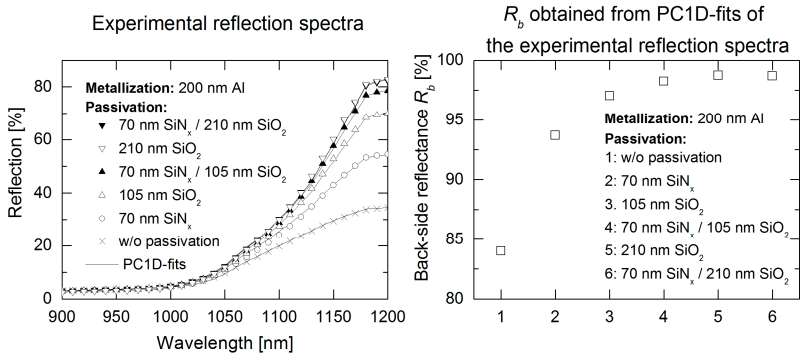

Figure 6.16: Experimental results of the reflection samples with Al rear-side metallization and double layer passivation (SiN_x/SiO_2-stack).

6.2.2 Multi-layer Al-based metallization with first Al-Si layer as a spiking barrier

In the previous chapter it was found that the use of Al-Si/Al-stack instead of pure Al can suppress the Al-spiking. It was shown that the optimal thickness of the first Al-Si layer should be about 400 - 450 nm when 2-µm-thick Al-metallization and contact-formation annealing at 400 °C is needed. Based on this result, the back-side reflectance of the optimized Al-Si/Al-stack on standard passivation of 70 nm SiNx as well as on the optically optimized passivation 70 nm SiN_x / 210 nm SiO_2 is also investigated and compared with the results of pure-Al. The results are shown in Figure 6.17.

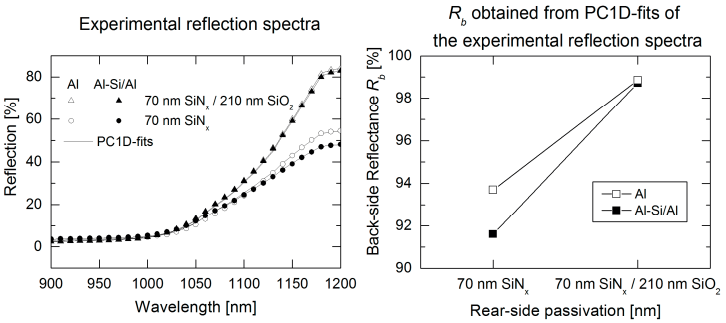

Figure 6.17: Experimental results of the reflection samples with Al and Al-Si/Al-stack on SiN_x- and optically optimized SiN_x/SiO_2-passivation.

The use of Al-Si/Al-stack thus results in only minor optical loss compared to pure Al-metallization, especially when optically optimized rear-side passivation is used.

6.2.3 Multi-layer Al-based metallization with first Ti layer as a low resistance contacting metal

Ti is well-known of its superior contacting properties to highly doped n^+- and p^+-Si. It has very low specific contact resistance to n^+-Si, reduces the native oxide in the contact openings, adheres well to common passivation layers like SiO_2 or SiN_x, and last but not least it can be used as a spiking barrier [38]. Given these advantages, Ti is commonly used as a contacting-metal for front-side PVD-metallization for high efficiency silicon solar cells. However, the poor reflectivity in the NIR spectral range of Ti can be an issue limiting the photocurrent generation and thus the performance of the cell, if Ti is used as a contact metal on the rear-side. For this reason, optical investigations on samples with various rear-side configurations based on Ti as contacting metal were performed and compared with standard pure Al rear-side metallization. Efforts to overcome the poor NIR reflectivity of Ti by optimizing the rear-side passivation or by using very thin Ti layers were carried out. In the following, the results of these investigations are shown and discussed in detail.

- **Ray-tracing simulation results**

The impact of the low NIR-reflectivity of Ti on the generated current density of symmetry elements with single-layer passivation (SiN_x or SiO_2) of various thicknesses is shown in Figure 6.18.

In the non-passivated regions (Figure 6.18, passivation thickness = 0) the loss of the photocurrent density of a symmetry element with Ti compared to Al is very high (more than 1.5 mA/cm^2). The loss declines to about 1 mA/cm^2 for standard 70 nm SiN_x rear-side passivation. The current loss can be further reduced to about 0.25 mA/cm^2 by increasing the passivation layer thickness and it is less if a lower refractive index passivation as SiO_2 is used.

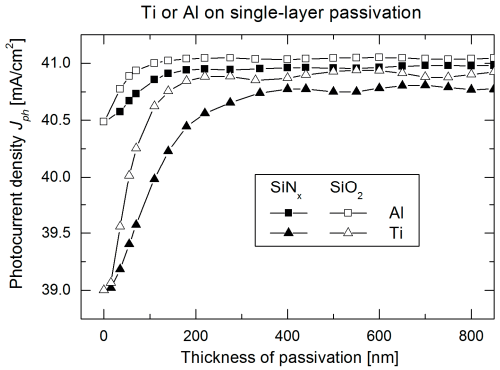

Figure 6.18: Generated photocurrent density of a symmetry element with Ti- or Al-metallization on single- layer SiN_x- or SiO_2-passivation of various thicknesses obtained by ray-tracing simulation Synopsys TCAD Sentaurus Device.

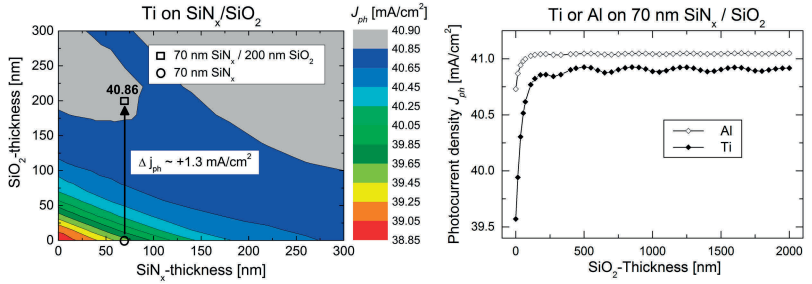

Figure 6.19: Generated photocurrent density of a symmetry element with Ti -metallization on double- layer SiN_x/SiO_2-passivation of various thicknesses obtained by ray-tracing simulation Synopsys TCAD Sentaurus Device. On the right hand side the simulation results of double-layer SiN_x/SiO_2-stack with 70 nm SiN_x and varying thicknesses of the capping SiO_2 are shown for Ti- as well as Al-metallization.

As for Al, the back-side reflection of solar cells passivated with SiN_x rear-side can be also enhanced by using a low-refractive index capping-layer as SiO_2 (Figure 6.19). The generated photocurrent density of a symmetry element with SiN_x/SiO_2-passivation covered with Ti-metallization and can be significantly enhanced in comparison to standard 70 nm SiN_x single-layer passivation ($\Delta j_{ph} > +1.3$ mA/cm^2). However, the improvement of the optical performance of the back-side is still not enough to match the level of symmetry element with Al rear-side metallization even for very thick SiO_2 capping layer as can be seen in Figure 6.19 (right). The reason for this is the fraction of transmitted light

hitting the rear surface at narrow angles of incident below the critical angle where no total internal reflection occurs. By increasing the thickness of the passivation layer only the losses of frustrated totally internally reflected light can be totally overcome (Figure 6.9). The reflection losses for very narrow angles of incident below the critical angle cannot be totally overcome but only by adjusting the thickness of the passivation layer, where constructive interferences occur (e.g. at 220, 600, 950 nm…). Therefore, the optical loss by using Ti metallization on an optically optimized rear-side passivation (i.e. single layer passivation with thickness > 200 nm or 70 nm SiN_x / 200 nm SiO_2 passivation stack) would be around 0.2 mA/cm² and more than 1 mA/cm² by using only 70 nm SiN_x passivation.

In order to enhance the back-side reflectance for the rays with narrow angles of incident and further reduce the reflection losses of the absorbing metal, more sophisticated multi-layer Bragg reflectors can be used, as found in the analytical simulation results in Figure 6.11 and Figure 6.12. An internal Bragg-stack consists of alternating low-high-low refractive index dielectric layers with a quarter wavelength optical thickness ($\lambda/4$-thickness) between the silicon wafer and the metallization (Figure 6.10). The results of the analytical simulations in Figure 6.12 showed that larger difference in refractive index between the low and high refractive index layers as well as higher order of Bragg-stack results in a higher internal reflectance at narrow angles of incident. Therefore, ray-tracing simulations were also done for triple and quintuple Bragg-stack between Ti and Si with SiO_2 as a low-n and SiN_x or aSi as high-n layer. First, simulations of triple Bragg-stack with varied thickness of the high-n passivation layers with 220 nm SiO_2 as low-n material were carried out in order to find the optimal thicknesses for maximal reflectance and hence maximal current generation. Afterwards, the generated current density of symmetry elements with single layer passivation is compared with triple and quintuple Bragg-stack. The results of the generated photocurrent density of symmetry elements with varying thickness of the middle layer of the triple Bragg stack are shown in Figure 6.20 (left).

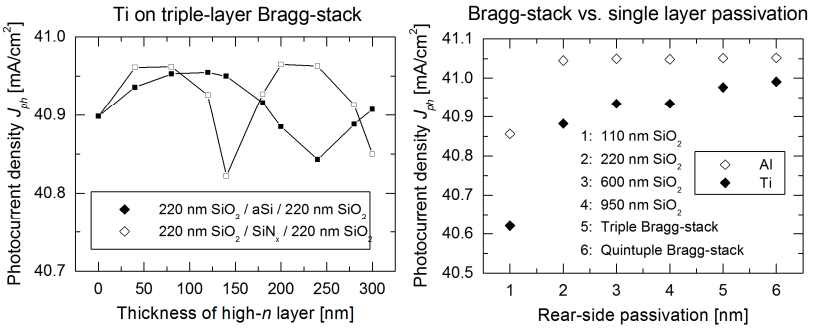

Figure 6.20: Generated photocurrent density of a symmetry element with Ti-metallization on triple-layer Bragg-stack with SiN_x or aSi as high-n layer of various thicknesses obtained by ray-tracing simulation Synopsys TCAD Sentaurus Device is shown on the left hand side. On the right hand side the results of triple and quintuple Bragg-stack are compared with those of single-layer SiO_2-passivation.

The results of the generated current are in a very good agreement with the reflectance results of the analytical simulations shown in Figure 6.11 and Figure 6.12. Depending on the thickness of the middle layer of the Bragg stack, the generated photocurrent density shows maxima and minima due to interference effects of the reflected light at narrow angles of incident. The optimal thicknesses are found to be in the range between 40 and 80 nm for aSi and between 80 and 140 nm for SiN_x. Based on these results, symmetry elements with triple (TBS) and quintuple Bragg-stacks (QBS) with 70 nm aSi as high-n material and 220 nm SiO_2 as low-n material were simulated for both the lowly reflective Ti and the highly reflective Al. The results are shown in Figure 6.20 (right). As expected from the analytical reflectance-simulations, by using Bragg-stack of higher order the generated photo current density of symmetry element with Ti metallization increases, though still not enough to the level of Al metallization. Furthermore, the use of sophisticated Bragg-reflectors brings almost no benefit for highly reflective metals like Al.

As a last effort to overcome the reflection losses of Ti is to combine both approaches: thick first passivation layer in order to minimize frustrated total internal reflection losses for wide angle of incidents combined with Bragg-stack in order to enhance the reflectance for narrow angles of incident. Therefore, 3D device simulations were carried out for the same triple and quintuple Bragg-

reflectors in Figure 6.20, with varying thickness of the first SiO_2 layer. The results are shown in Figure 6.21 against the results of one layer SiO_2 passivation as a reference. Due to frustrated internal total reflection losses, the generated current density at the first peak (i.e. at thickness of the first SiO_2 layer around 220 nm) is lower than at the peaks at higher thicknesses where also constructive interferences occurs (e.g. around 600, 950 nm or 1300 nm). Table 6.1 sums up the results of all simulated devices. The photocurrent density of a symmetry element with Ti rear-side metallization and quintuple Bragg-stack with at least 600-nm-thick first SiO_2 layer is only 0.02 mA/cm² lower than the photo current density of a symmetry element with SiO_2/Al rear-side reflector and 0.04 lower than Al metallization with modified Bragg-stack. With this approach, it could be demonstrated that the reflection losses of a strong absorbing rear-side contact metal in the NIR spectral range like Ti can be minimized to a negligible level. However, this approach is hard to be implemented in an industrial environment and therefore not tested experimentally. With the widely used 70 nm SiN_x rear-side passivation the optical loss by using Ti as a contact metal is more than 1 mA/cm². This optical loss can be reduced to less than 0.2 mA/cm² by using a 220 nm capping SiO_2 layer.

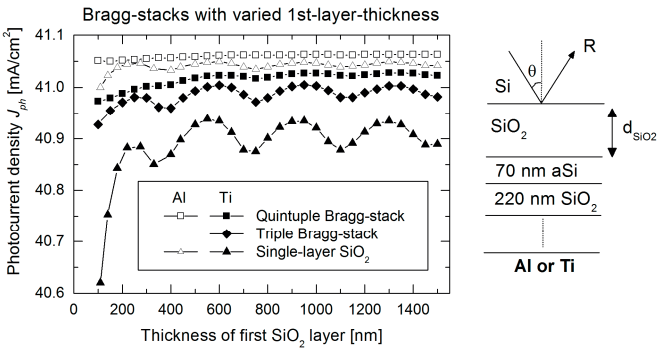

Figure 6.21: Generated photocurrent density of a symmetry element with Ti-metallization on various Bragg-stack with SiO_2 as low-n layer and aSi as high-n layer obtained by ray-tracing simulation Synopsys TCAD Sentaurus Device. The generated photocurrent density is plotted as a function of the thickness of the first SiO_2-layer.

Table 6.1: Ray-tracing simulation results of symmetry element with Ti and Al rear-side metallization and various rear-side passivation configurations.

Rear-side passivation	J_{pb} (mA/cm²)		ΔJ_{pb} (mA/cm²)	Comment
	Ti	Al		
SiNx (70 nm)	39.571	40.73	1.159	Standard SiN_x
SiN_x (400 nm)	40.772	40.96	0.188	SiN_x at first interference peak
SiN_x/SiO_2 (70/220 nm)	40.858	41.042	0.184	SiN_x with optimized cap-layer
SiO_2 (220 nm)	40.882	41.045	0.163	SiO_2 at 1st interference peak
SiO_2 (600 nm)	40.934	41.049	0.115	SiO_2 at 2nd interference peak
SiO_2/aSi/SiO_2 (220/70/220 nm)	40.976	41.051	0.075	Triple Bragg-stack
SiO_2/aSi/SiO_2/aSi/SiO_2 (220/70/220/70/220 nm)	40.991	41.052	0.061	Quintuple Bragg-stack
SiO_2/aSi/SiO_2 (600/70/220 nm)	41.004	41.063	0.059	Triple Bragg-stack with thick 1st layer
SiO_2/aSi/SiO_2/aSi/SiO_2 (600/70/220/70/220 nm)	41.023	41.063	0.04	Quintuple Bragg-stack with thick 1st layer

- **Experimental results**

The impact of Ti rear-side metallization on the optical performance of the test samples was tested experimentally with the rear-side configurations shown in Figure 6.22.

The reflection spectra and the back-reflectance values R_b of the test samples are shown in Figure 6.22. The poor reflectivity of Ti was found to have a huge impact on the back-side reflectance of the test samples, as expected from the analytical and numerical ray-tracing simulations. For the non-passivated samples, which represent the non-passivated regions in a solar cell, back-side reflectance values < 10 % were obtained with Ti metallization. This value is

significantly lower than the back-side reflectance of the samples with Al-metallization. The results of the passivated samples are similar to the simulation results. When only standard 70 nm SiN_x is used as a rear-side passivation, the back-side reflectance loss of the samples with Ti metallization is very high compared to the samples with Al-metallization ($\perp R_b$ > 50%). The optical loss can be significantly reduced to about 7% by using SiO_2 as a rear-side single-layer passivation with a layer-thickness > 200 nm or simply as a cap-layer if SiN_x is needed as a first passivation layer. The experimental results also confirmed the results obtained by the numerical simulations that by using very thick capping layer or more sophisticated triple Bragg-stack only minor gain in back-side reflectance can be obtained for the samples with Ti-metallization. As a thick capping layer, about 4-µm-thick polyimide was used. The stack-configuration 220 nm SiO_2 / 80 nm aSi / 220 nm SiO_2 was used for the triple Bragg-stack. More complex quintuple Bragg-stack or Bragg-stack with a thick first layer were not tested experimentally because they cannot be implanted for industrial solar cells as used in this work.

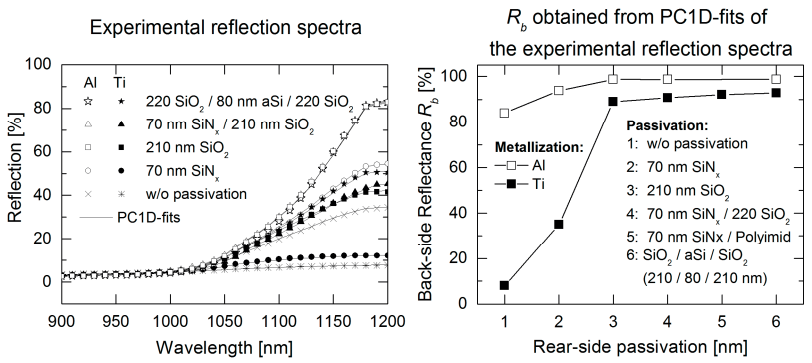

Figure 6.22: Experimental results of reflection samples with Ti and Al rear-side metallization on various rear-side passivation configurations.

Therefore, the use of Ti as a contact layer on the rear-side will result in a huge optical loss, even for optically optimized, in the industry implementable rear-side passivation.

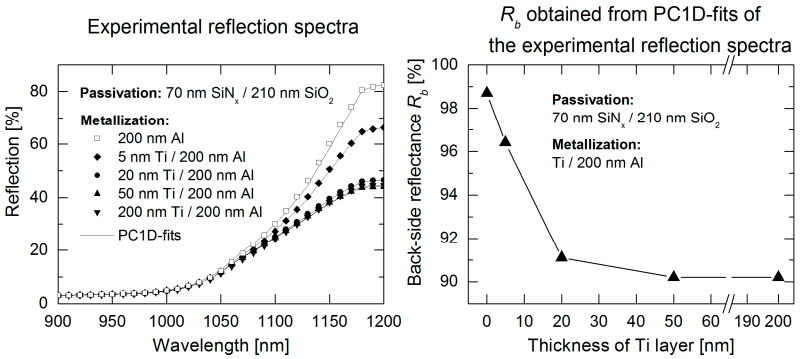

Figure 6.23: Experimental results of Ti/Al-stack of various thicknesses of the Ti-layer.

The use of very thin Ti as a contact layer combined with a thick, high reflective capping Al-layer for sufficient current transport was also carried out. Reducing the thickness of the Ti layer might result in less optical losses due to less absorption in the Ti layer. Therefore the influence of the thickness of Ti in Ti/Al rear side metallization-stack was tested. The penetration depth is about 25 nm for NIR electromagnetic wave of 1100 nm wavelength [88]. This indicates that already a very thin Ti layer of about 10-15 nm (half of the penetration depth) absorbs the majority of the photons, which is also confirmed experimentally as shown in Figure 6.23. Already a very thin Ti layer of a few nm reduces the back-side reflectance of the test samples to a non-negligible level. Thus, using a very thin Ti layer for a higher contact-quality (lower specific contact resistance and higher adhesion than Al) would also result in non-negligible optical losses.

6.2.4 One-layer Ag-metallization on various passivation layers

In Figure 6.3 it was shown that the noble metal Ag has the highest NIR-reflectivity compared to other rear-side metallization materials like Al or Ti. Thus, using Ag on the rear-side might bring optical gain to the cell performance as found out in the analytical simulation results of rear-side reflectance (Figure 6.9). Therefore 3D ray-tracing simulations and experiments on reflection samples with Ag rear-side metallization were carried out. The results of Ag-metallization are compared to the results of Al-metallization in order to estimate the optical gain by using the superior reflective Ag instead of Al.

The impact of the very high NIR-reflectivity of Ag on the generated current density of symmetry elements with single-layer passivation (SiN_x or SiO_2) of various thicknesses is shown in Figure 6.24. In the non-passivated regions (Figure 6.18, passivation-thickness = 0) the difference of the photocurrent density between Ag and Al is about 0.35 mA/cm². When the rear-side is passivated with only 70 nm SiN_x, the photocurrent gain by using Ag instead of Al is about 0.2 mA/cm². By thickening the SiN_x layer to more than 200 nm, the difference in photocurrent density between Ag and Al is only about 0.06 mA/cm². This benefit declines further to only 0.02 mA/cm² when sufficiently thick low-refractive index material as SiO_2 is used (either as a single-layer passivation or as a capping layer for SiN_x-SiO_2 double-layer passivation).

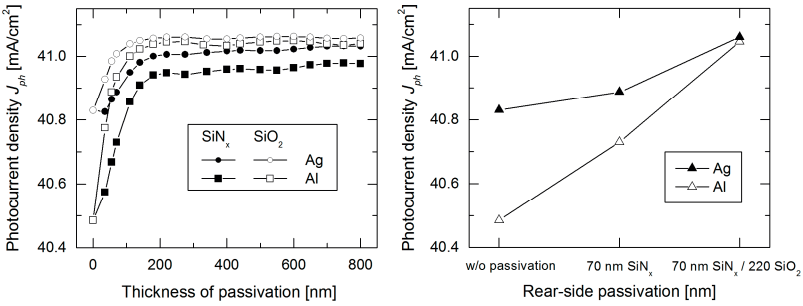

Figure 6.24: Generated photocurrent density of a symmetry element with Ag- and Al-metallization on single- layer SiN_x- or SiO_2-passivation (left) of various thicknesses obtained by ray-tracing simulation Synopsys TCAD Sentaurus Device. On the right hand side the simulation results of standard 70 nm SiNx are compared the optically optimized SiN_x/SiO_2-stack.

The experimental results of the reflection samples with standard single-layer SiN_x-passivation with 70 nm layer-thickness and double-layer passivation-stack consisting of 70 nm SiN_x capped with 210 nm SiO_2 are shown in Figure 6.25. As predicted from the numerical ray-tracing simulations, the high reflectivity of Ag enhances the optical performance of the rear-side, especially for the non-passivated samples (which represents the non-passivated contact-openings in a solar cell). The gain in back-side reflectance for the non-passivated samples is more than 10 $\%_{abs}$ by using Ag instead of Al on the back-side. The gain in back-side reflectance for the samples with 70 nm SiN_x and Ag- instead of Al-metallization on the back is about 4.5 $\%_{abs}$. This would bring about

0.2 - 0.3 mA/cm² gain in short-current density depending on equation 2.31. The optical gain decreases to as low as 0.5 $\%_{abs}$ if an additional 210 nm SiO_2 capping layer is used, which is in a very good agreement with the numerical device simulation results shown in Figure 6.24. The use of Ag instead of Al is thus more beneficial for the standard 70 nm SiN_x than for SiO_2-based passivation.

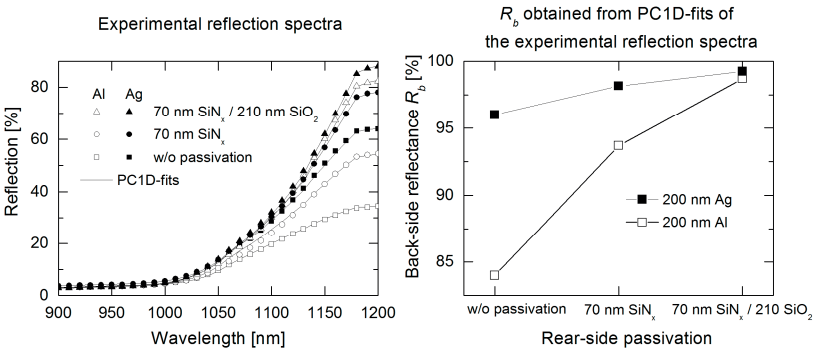

Figure 6.25: Experimental results of the reflection samples with Ag and Al rear-side metallization on standard 70 nm SiN_x passivation and optically optimized double layer passivation (SiN_x/SiO_2-stack).

6.2.5 Multi-layer Al-based metallization with first thin Ag layer as an IR reflector

Since the noble metal Ag is very expensive compared to Al (Figure 2.18), experiments with a thin first Ag-layer as an optical-enhancement layer capped with thick Al-metallization for sufficient current transport were carried out. The aim of these experiments was to find the minimal Ag-thickness needed for considerable optical enhancement in order to spare material costs compared to the high reflecting but expensive single-layer Ag-metallization. The material cost of using optimized metallization based on thin Ag first-layer were also calculated and compared to single-layer Al- and Ag-metallization.

- **Backside reflectance of Ag/Al and Ag/Ti/Al stack with varying Ti thickness**

Silver and aluminum are well soluble in each other and react with each other to form intermetallic compounds even at low temperatures (< 200 °C) as can be

seen from Figure 6.26 (left). The Ag-Al phase diagram indicates two intermetallic phases Ag_2Al and Ag_3Al which can be stable at low temperatures with Ag_2Al is reported to be the main phase [103-105] at low temperatures. From previous investigations of thin-film diffusion couples [103-105], an extremely rapid initial diffusion and phase formation of Ag_2Al is observed (Figure 6.26, right).

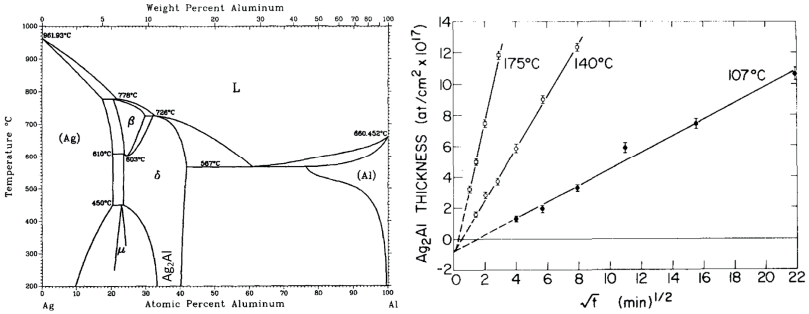

Figure 6.26: Binary phase diagram of Silver-Alumiunum system (left, taken from [106]) and time and temperature dependence of the formation of the main phase Ag_2Al (right, taken from [105]).

Thus, by using a thin Ag layer underneath the Al layer to enhance the back-side reflectance and hence optical performance of the rear side, an intermixing between Ag and Al is expected to occur even during deposition, since the formation of these intermetallic phases already takes place at low temperatures. This intermixing and the formation of the intermetallic phases can have an impact on the back-side reflectance and there would be no benefit from the high reflectivity of Ag. Indeed, a significant drop in reflectivity of Ag-Al diffusion couples is reported at both surfaces (Al or Ag) [103] when intermixing occurs. However, the intermixing of Ag and Al can be overcome by using intermixing barriers similar to spiking barriers between Si and Al presented in Chapter 4. It was shown in Chapter 4 that the use of sacrificial barriers like titanium can prevent intermixing between the two elements by reacting with them and forming intermetallic compounds with the barrier layer. In the case of Ag and Al only titanium alumindes are important at processing temperatures around 400 °C (as for contact formation annealing), since Ti_xAg_y-intermetallics are reported to be formed at significantly higher temperatures [107]. Based on the

results obtained in Chapter 4 (Ti as a spiking barrier between Al and Si), a 50 nm Ti layer between Ag and Al was expected to be thick enough to prevent Al reaching and reacting with Ag for a contact formation annealing at 400 °C for 5 min.

Therefore, reflection samples with Ag/Al and Ag/Ti/Al stack on the rear side with various Ti layer thicknesses and 200 nm thick Ag layer were fabricated and annealed at 400 °C for different times. The back-side reflectance of these samples is shown in Figure 6.27. The back-side reflectance obtained from these samples was compared with the back-side reflectance of the samples with single-layer Al and Ag metallization. A significantly lower back-side reflectance was observed for the samples with Ag/Al-stack indicating the intermixing of Ag and Al layer and the formation of intermetallic phases. Thus, there is no benefit from using thin first Ag layer underneath the thick Al layer to enhance the back-side reflectance of the cell without a barrier layer. The back-side reflectance of the sample with 10 nm Ti degrades significantly after 5 min at 400 °C which indicates the consumption of the barrier and the intermixing of the metals. A 50 nm thick Ti-barrier is consumed after about 100 min and a 100 nm barrier after about 200 min annealing at 400 °C.

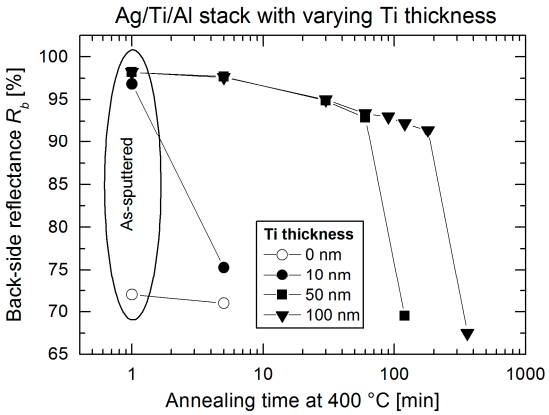

Figure 6.27: Experimental results of multi-layer metallization with Ag as a contact layer.

- **Back-side reflectance results of Ag/Ti/Al stack with varying Ag thickness**

Since Ag is very expensive, the minimal Ag thickness at which the back-side reflectance matches the level of thick Ag is investigated. For this reflection samples with Ag/Ti/Al stack with varying Ag layer thickness were fabricated and the back-side reflectance of these samples was determined. The results are shown in Figure 6.28. The results of the test samples with varying layer-thickness of the first Ag-layer show that at least 50 nm Ag is needed for the triple stack to match the level of pure Ag metallization. Thus, a triple layer stack consisting of 50 nm Ag, a barrier layer and a thick Al can be used instead of single-layer Ag-metallization and material cost can be reduced.

Table 6.2 show the material cost of pure Ag-, pure Al- and Ag/Ti/Al-metallization (calculated as shown in section 2.5). For pure Ag-metallization a layer-thickness of 1100 nm and for pure Al-metallization 2000 nm is assumed due to the lower lateral conductivity of Al. Based on the results of Figure 6.28, layer-thicknesses of 60 nm Ag, 100 nm Ti and 2000 nm Al are assumed for the Ag/Ti/Al metallization-stack. The results in Table 6.2 show that use of thin Ag-layer of only 60 nm are still cost-intensive compared to pure Al-metallization. For this reason, Ag-based rear-side PVD-metallization is not further considered in this work.

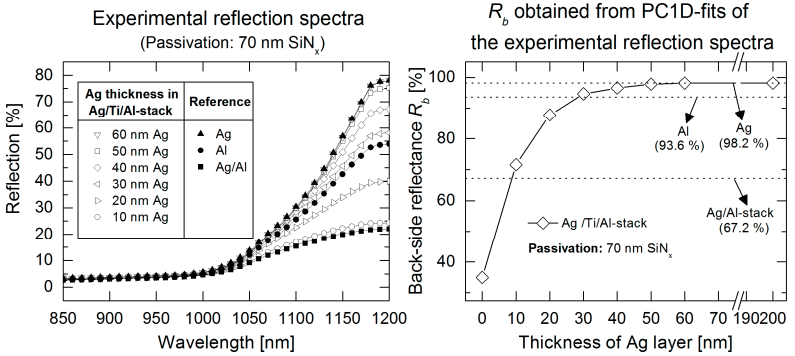

Figure 6.28: Experimental results of multi-layer metallization with Ag as a contact layer with varying Ag layer thickness.

Table 6.2: Comparison of material cost in US cent / wafer for pure Al, pure Ag and Ag/Ti/Al-stack.

	2000 nm Al	1100 nm Ag	60 nm Ag	100 nm Ti	60 nm Ag / 100 nm Ti /2000 nm Al
Material cost (US cent/w)	0.02	19.77	1.08	0.02	1.12

6.2.6 Comparison of the optimized rear-side reflectors

A comparison of the experimental results for all metallization schemes on the standard passivation of 70 nm SiN_x as well as the optically optimized passivation 70 nm SiN_x / 210 nm SiO_2 are shown in Figure 6.29 and Table 6.3.

Table 6.3: Comparison of the various rear-side metallization schemes on standard 70 nm SiN_x and optically optimized SiN_x/SiO_2-passivation. The rear-side reflectance R_b is obtained from the experimental results of the reflection-samples by PC1D fittings of the experimental data. The obtained R_b-values are then used to guess the short-circuit current density J_{sc} for nPERT solar cells, also by PC1D-simulation.

	70 nm SiN_x		70 nm SiN_x / 210 nm SiO_2		Gain through SiO_2 cap	
	R_b (%)	J_{sc} (mA/cm²)	R_b (%)	J_{sc} (mA/cm²)	ΔR_b ($\%_{rel}$)	ΔJ_{sc} ($\%_{rel}$)
Ag/Ti/Al	98.15	39.24	99.25	39.33	1.12	0.23
Al	93.7	38.93	98.85	39.30	5.50	0.95
Al-Si/Al	91.6	38.80	98.72	39.29	7.77	1.26
Ti/Al	35	36.87	92.8	38.87	165.14	5.42

The highest rear-side reflectance and thus short-circuit current density can be obtained by using Ag as a contact metal. However, the material cost of Ag is still too expensive even for very thin Ag contact-layer of 50-60 nm. Therefore, metallization schemes based on Ag as a contact-metal have not been further followed during this thesis. Al-Si-based metallization showed only a minor loss in rear-side reflectance compared to pure Al, especially for optically optimized SiN_x/SiO_2-passivation and therefore can be a promising metallization approach for rear-side silicon solar cells, if a spiking-barrier is needed. The poor NIR-reflectivity of Ti might be a big drawback for the superior contacting metal Ti

and could result in a major optical loss when applied to the rear-side of silicon solar cells even on optically optimized rear-side passivation.

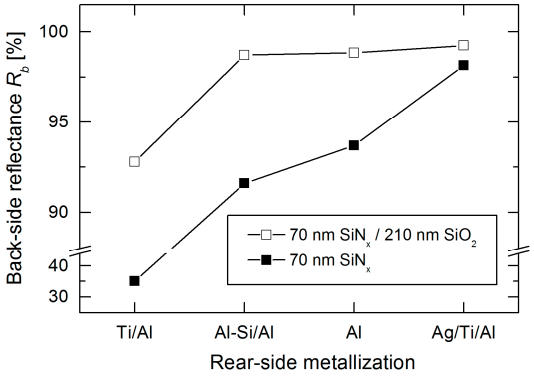

Figure 6.29: Comparison of the various rear-side metallization schemes on standard 70 nm SiN_x and optically optimized SiN_x/SiO_2-passivation.

6.3 Summary and conclusion

In this chapter, the impact of rear-side passivation and metallization layers on the rear-side reflectance and thus on the photocurrent-generation for silicon solar cells was investigated in detail. Various rear-side metallization schemes with Al, Al-Si, Ti or Ag as contact-metals were investigated in combination with various rear-side passivation. The key results of these investigations showed that the use of Al-Si results in only negligible minor optical loss, especially when optically optimized passivation (e.g. SiN_x/SiO_2-stack with about 210 nm SiO_2-layer-thickness) is used. The use of Ti as a contact-layer, however, results in a non-negligible optical loss even if the optically optimized SiN_x/SiO_2-passivation is used, due to the poor reflectivity of Ti in the NIR spectral region. When Ti is used as a contact-metal the difference in back-side reflectance is more than 6 $\%_{abs}$ compared to Al or Al-Si. This loss would result in a photocurrent-density loss of more than 0.3 mA/cm², which will be tested in Chapter 8 (solar cell results). Theoretical efforts by using 3D ray-tracing simulations in order to overcome the poor reflectivity of Ti by using sophisticated multi-layer passivation (e.g. Bragg-stack) were also carried out. The

key result of these investigation showed that Bragg-stack of order higher than five with a thick first layer (~ 600 nm) is needed in order to reduce the optical losses to a negligible level, which is barely implementable in industrial environment and is therefore not examined experimentally. Regarding Ag as a contact-metal, it was shown that at least 50 - 60 nm Ag is required to benefit from its very high reflectivity, which is still cost intensive compared to Al-metallization. Furthermore, the benefit from using thin Ag-layer as a contact-metal is only beneficial for standard 70 nm SiN_x rear-side passivation. When optically optimized rear-side passivation is used (e.g. SiN_x/SiO_2-stack), the enhancement of rear-side reflectance by using Ag instead of Al is very low ($< 1\ \%_{abs}$).

7 Plasma-induced damage of sputtering deposition of metal layers

Sputtering deposition of metal layers is a high vacuum plasma process and can cause plasma-induced damage to the underlying passivated silicon. Damaged silicon-passivation interface after metal deposition will lead to a degradation in the passivation quality of the rear-side of the cell and thus to a degradation in cell performance as shown in section 2.3.4. During sputtering deposition of the metallization the passivated surface of the solar cell is struck by species from the plasma in the deposition chamber which can cause plasma-induced damage. In addition to the sputtered metal atoms the cell is struck with low and high energy neutral sputter gas atoms, negative and positive ions, impurity gas atoms, high energy and thermal electrons and UV and X-ray photons [32] (Figure 7.1 left). The high energetic photons can generate electron-hole pairs in dielectric passivation materials (e.g. SiO_2) by ionization and charge up them and generate interface states and traps causing the plasma-induced damage at the interface [108] (Figure 7.1 right).

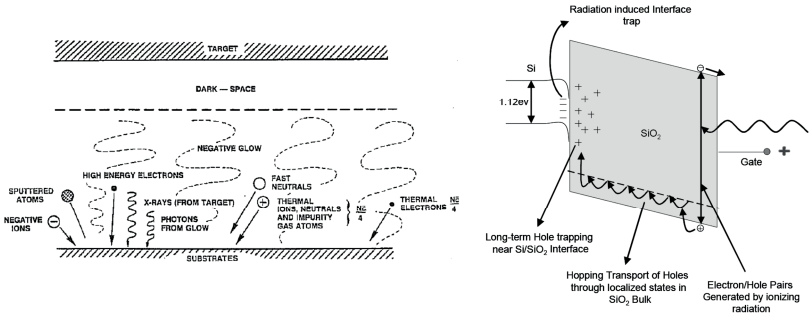

Figure 7.1: Spices that strike the substrate during sputtering deposition (left, taken from [32]) and plasma-induced damage of SiO_2 due to ionizing radiation-induced positive oxide charge as well as interface traps in the oxide (right, taken from [108]).

While the impact of plasma processing on Si-SiO_2 interface is extensively studied by many authors due to its importance in the degradation of MOS devices after

plasma processing (Metal Oxide Semicoductor [109]), not so many works can be found on other silicon-passivation interfaces like Si-SiN_x or Si-Al_2O_3. Since the nPERT solar cells developed in this thesis feature SiN_x rear-side passivation, the impact of sputtering deposition of metal layers on Si-SiN_x interface is investigated in details and compared to other silicon-passivation interfaces as Si-SiO_2 and Si-Al_2O_3. Some of the results of this chapter are published in [52].

7.1 Experimental approach

In order to investigate the influence of sputtering deposition of metal layers on the passivation quality of underlying passivation layers, damage-etched, RCA-cleaned [110] and double-sided passivated Cz silicon wafers were used. After deposition of the passivation layers the passivation was activated by a standard thermal step (a forming gas annealing at 400 °C for thermally grown SiO_2 and a firing step with a peak temperature of 790 °C for SiN_x and Al_2O_3 passivated samples). Afterwards, aluminum was deposited by DC-sputtering on one side of the sample. Figure 7.2 shows a sketch of the test sample.

The impact of sputtering deposition of aluminum on the various silicon-passivation interfaces was investigated by measuring the effective carrier lifetime τ_{eff} as well as by measuring the density of interface states D_{it} and total charge density Q_{tot} before and after sputtering deposition as well as after forming gas annealing at 400 °C. The effective lifetime was measured by Microwave Photoconductance Decay (MWPCD). The density of interface traps and the total charge density were measured by Corona Oxide Characterization of Semiconductor (COCOS). In the following these characterization methods are explained.

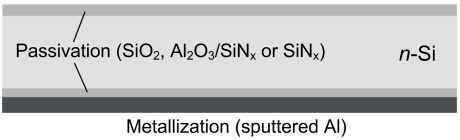

Figure 7.2: The sample structure used in for the investigations on plasma-induced damage.

7.1.1 Microwave photoconductance decay (MWPCD)

Microwave photoconductance decay (MWPCD) is a contactless carrier lifetime measurement technique which uses a microwave system for the determination of carrier lifetime. The carrier lifetime is determined by contactless measuring of photoconductance decay of the sample after optical excitation whereas the photoconductance decay itself is sensed by microwave reflection. The measurement tool used in this work was a WT-2000 from SDI Semilab. The optical excitation of the sample is done by a pulsed infrared semiconductor laser which generates electron-hole pairs in the illuminated area of the sample. The generated electron-hole pairs cause an increase in the conductance of the sample in the illuminated area (thus photoconductance). After excitation the electron-hole pairs recombine and the photoconductance decays to the steady-state level. The decaying photoconductance can be monitored by sensing the microwave reflectivity of the sample, since the reflected microwave power is proportional to the conductivity of the sample. The measured microwave reflectivity decay is afterwards fitted with a multi-exponential function where the time constant of the recorded curve is the measured effective lifetime of the sample in the illuminated area. This procedure is done on various points on the sample and so the effective carrier lifetime of the sample can be mapped. The effective lifetime of the sample is the average of the effective lifetime of the mapped regions of the sample. For detailed description of the MWPCD metrology it can be referred to e.g. [111].

The effective carrier lifetime gives information about the recombination in the silicon wafer as well as at the surfaces as shown in section 2.1.3. Therefore, if the passivation quality of one of the surfaces or in the bulk silicon is changed, the effective carrier lifetime will correspondingly change as well. This means, that if the passivation quality of the deposited surface is damaged after sputtering deposition of aluminum, the effective carrier lifetime of the sample will decrease. Since the detection of the effective lifetime can be done by sensing the microwave reflection of one the surfaces, the measurement can be done either from the deposited surface after back-etching of the metal layer or from the non-deposited surface.

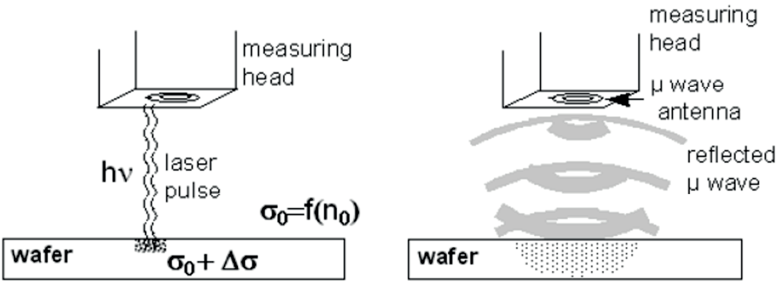

Figure 7.3: Working principle of MWPCD. Electron-hole pairs are generated with infrared laser (left) which leads to an increase in the conductance (σ) of the sample in the illuminated area. The photoconductance decay is sensed by microwave reflection (right). The effective carrier lifetime is extracted from the measured microwave reflectivity (the graphs are taken from [112]).

Figure 7.4 shows measured effective carrier lifetime on various samples with various passivation layers after aluminum sputtering deposition. Every sample is measured twice, one time from sensing the microwave reflection off the non-deposited surface and the other time after back-etching of the aluminum layer.

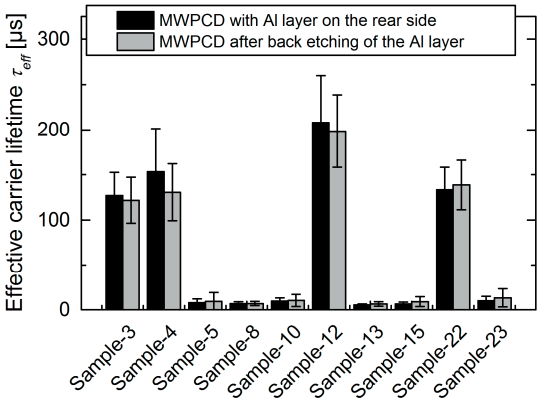

Figure 7.4: MWPCD comparison of various test samples measured from the front with and without Al-metallization on the back.

The results of MWPCD measurements with and without a metalized rear side show no significant difference in the measured effective carrier lifetime

(Figure 7.4). Therefore MWPCD measurements of the test samples used in this work are performed from the front side without back etching of the metal layer.

7.1.2 Corona Oxide Characterization of Semiconductor (COCOS)

Corona oxide characterization of semiconductor (COCOS) is a contactless measurement technique for the characterization of semiconductor-dielectric interface properties, equivalent to those obtained in MOS-CV measurement technique (capacitance-voltage characteristics of metal oxide semiconductor [113]). In comparison to the destructive MOS-CV, COCOS does not require time-consuming and costly fabrication of capacitors and it is also a non-destructive one. The measurement tool used in this work was C.FORS system from Semilab SDI.

While in MOS-CV the capacitance-voltage C-V-characteristics are measured, in COCOS technique the contact potential difference in the dark ($V_{CPD\text{-}dark}$) and after illumination ($V_{CPD\text{-}ill}$) is measured as a function of corona charge placed on the whole wafer. The corona charging is done using SDI whole wafer corona charging method [114]. In this method the whole wafer corona charging is done by using a corona wire moving parallel to the wafer which generates the corona discharge in the air. Thus $(H_2O)_nH^+$ and CO^{3-} are the dominant positive and negative ions in the corona discharge.

The contact potential difference is measured using contact potential difference probe which is placed above the wafer. A vibrating fork directly below a steady reference electrode modulates the probe to wafer capacitance and generates an AC current signal which is monitored [115].

The change of the contact potential difference in the dark ($\Delta V_{CPD\text{-}dark}$) caused by the deposited corona charge is equal to the change in the voltage drop across the oxide (ΔV_{ox}) plus the change in the surface barrier (ΔV_{SB}) (voltage drop across the space charge region) as shown schematically in Figure 7.5

$$\Delta V_{CPD-dark} = \Delta V_{OX} - \Delta V_{SB}. \tag{7.1}$$

Strong illumination collapses the space charge region causing $V_{SB}\approx 0$ (Figure 7.5). Thus, the change of the contact potential difference under illumination ($\Delta V_{CPD\text{-}ill}$) is only the change in the voltage drop across the oxide (ΔV_{ox})

$$\Delta V_{CPD-ill} = \Delta V_{OX}. \tag{7.2}$$

By combining equations (7.1) and (7.2), the change in the surface barrier ΔV_{SB} due to corona deposition can be obtained by measuring the contact potential difference in the dark and under illumination

$$\Delta V_{SB} = \Delta V_{CPD-dark} - \Delta V_{CPD-ill}. \tag{7.3}$$

All interface and oxide charge information is derived through determination of V_{SB} as a function of deposited corona charge. In this work, the output parameters considered are total charge density (Q_{tot}) and interface trap density (D_{it}). Q_{tot} equals the corona charge density that is required to change the surface barrier from the initial condition to the flat-band voltage (i.e. V_{SB}=0) and D_{it} describes the interface trap distribution across the energy gap. For detailed description of the COCOS metrology it can be referred to e.g. [115].

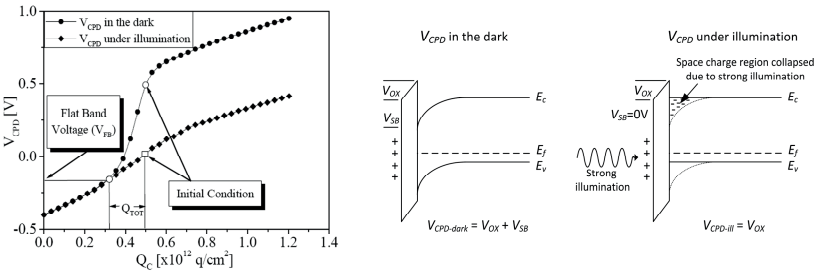

Figure 7.5: Contact potential difference in the dark $V_{CPD\text{-}dark}$ and under illumination $V_{CPD\text{-}ill}$ (after [116]).

7.2 Experimental results

7.2.1 Impact of aluminum sputtering on the electrical properties of Si/SiO_2 interface

The effective carrier lifetimes of thermally-grown SiO_2 passivated samples are fully degraded after sputtering of a 400 nm aluminum at low power of 2 kW (Figure 7.6). The drop of the effective lifetime is due to increased density of interface states (D_{it}) which indicates that the Si/SiO_2-interface is damaged after the sputtering process (Figure 7.7). This damage is attributed to the bombardment of the layer with radiation in the soft X-ray regime mainly in the range between 2.5 and 3.5 nm as extensively investigated and reported by [117]. The sputter-induced damage can be reversed by a post-metallization thermal annealing step at 400 °C as can be seen in Figure 7.6 and Figure 7.7.

Since sputter-induced damage of thermally-grown SiO_2 can be reversed by a post metallization annealing step, a similar behavior is expected when applying a sputtering process where the substrate temperature during sputtering is high enough for an in-situ-annealing process (dynamic annealing). In section 3.2.5 it was shown that the substrate maximal temperature during sputtering increases significantly when aluminum is sputtered at high power of 14 kW in comparison to sputtering at low power of 2 kW. Based on this, a 400 nm aluminum layer is sputtered on SiO_2 passivated samples at a sputtering power of 14 kW. The effective carrier lifetime and the density of interface states were measured before and after sputtering. It is observed that effective carrier lifetimes of the test samples after aluminum sputtering at 14 kW are significantly higher than at 2 kW. The measured density of interface states of these samples after sputtering at higher power also showed a lower density of interface states in comparison to sputtering at low power which indicates less damage to the passivated interface Si/SiO_2 after sputtering.

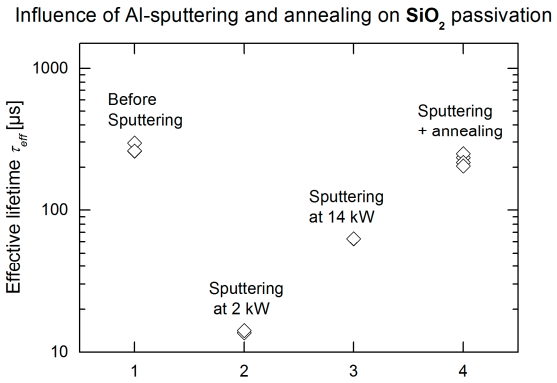

Figure 7.6: Measured effective carrier lifetime of SiO_2 passivated test samples before and after DC-sputtering of 400 nm Al at low and high power and after forming gas annealing at 400 °C.

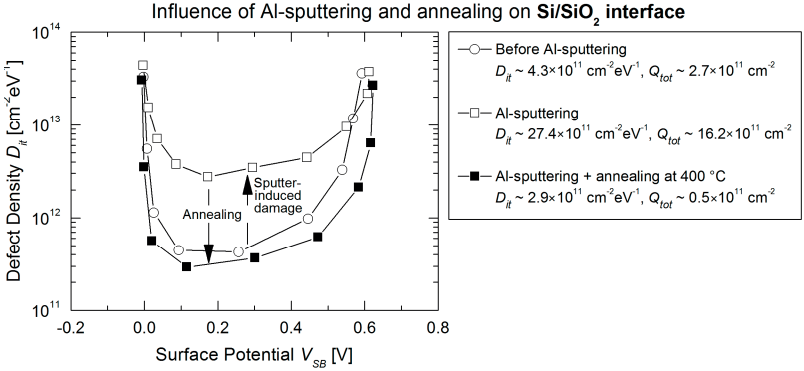

Figure 7.7: Measured defect density as a function of surface potential of SiO_2 passivated samples before and after DC-sputtering of 400 nm at 2 kW and after forming gas annealing at 400 °C.

To further investigate the effect of dynamic anneal a 400 nm aluminum layer is sputtered on SiO_2 passivated samples at low power (2 kW) but with pre- and post-heating as well as at high power (14 kW) without any heating treatment. The samples were heated in a rapid thermal annealing (RTA) chamber next to the deposition chamber at temperatures around 400 °C (no forming gas annealing, since in vacuum) so that no vacuum breakage occurs. It is observed that the damage decreases when the sample is pre- or post-heated (Figure 7.8). The effective lifetime of heated samples at low power is improved to the level

of the non-heated samples sputtered at high power as can been seen in Figure 7.8 which indicates a dynamic in-situ annealing process during sputtering at high power.

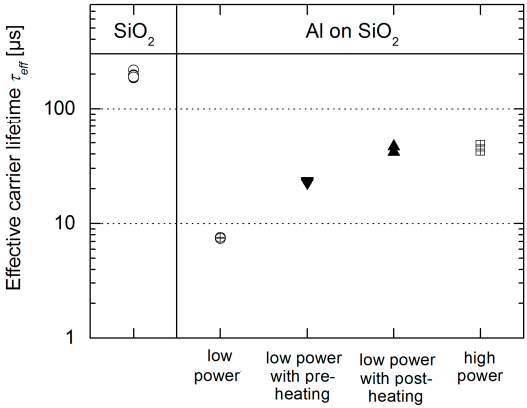

Figure 7.8: Measured effective carrier lifetime of SiO_2 passivated test samples before DC-sputtering of Al and after DC-sputtering at low power with and without heating treatments and at high power [52].

7.2.2 Impact of Al sputtering on the electrical properties of Si/Al_2O_3 interface

Similar to the SiO_2-passivated samples, the effective lifetime of the samples with Al_2O_3/SiN_x passivation suffers a huge degradation after aluminum sputtering. Furthermore, a less degradation after sputtering at higher power is also observed which is due to the dynamic annealing effect explained in the previous section. The effective lifetime degradation also correlates with an increased density of interface states D_{it} after the sputtering process which indicates that the degradation is due to damaged silicon/passivation interface after aluminum sputtering. The plasma-induced damage also generates positive charged traps near the interface (similar to the results of SiO_2 passivated samples) which results in a reduction of the total negative charge density of Al_2O_3 from about -2.4 to -0.6×10^{12} cm^{-2}. Werner et al. [118] reported that a very thin SiO_2 layer of 2-3 monolayers exists at the interface between silicon and Al_2O_3

passivation which is very likely the reason to the similar behavior of sputter-induced damage between Al_2O_3 and SiO_2 passivated samples.

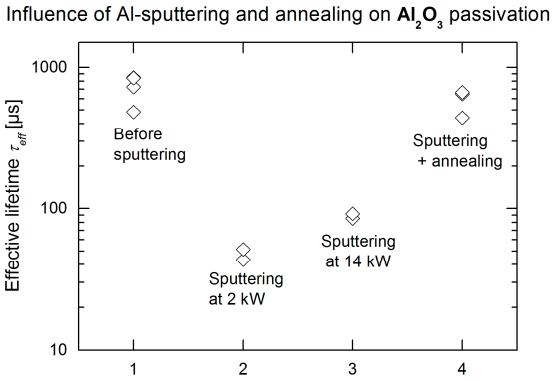

Figure 7.9: Measured effective carrier lifetime of test samples with Al_2O_3/SiN_x passivation stack before and after DC-sputtering of 400 nm Al at low and high power and after forming gas annealing at 400 °C.

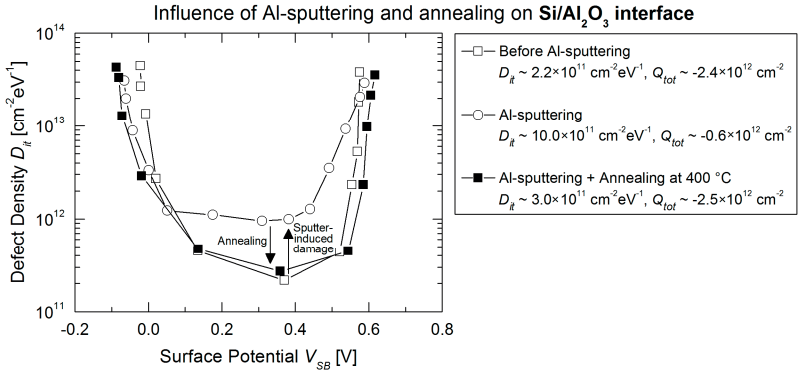

Figure 7.10: Measured defect density as a function of surface potential the samples with Al_2O_3/SiN_x passivation stack before and after DC-sputtering of 400 nm at 2 kW and after forming gas annealing at 400 °C.

7.2.3 Impact of Al sputtering on the electrical properties of Si/SiN_x interface

In contrary to SiO_2 and Al_2O_3 passivated sample, there is only marginal effective lifetime degradation of the SiN_x passivated samples. Furthermore SiN_x

passivation of silicon is not affected by increasing sputtering power unlike SiO_2 and Al_2O_3 passivation. COCOS measurements of the SiN_x passivated samples indicate no significant change in interface defect or charge density before and after sputtering. The Si-SiN_x interface seems to be less sensitive to the damaging radiation present in the sputtering chamber than Si-SiO_2 or Si-Al_2O_3 interfaces. The significantly higher density of fixed charge in the SiN_x layer and the different interface properties of Si-SiN_x might be the reason of this radiation hardness.

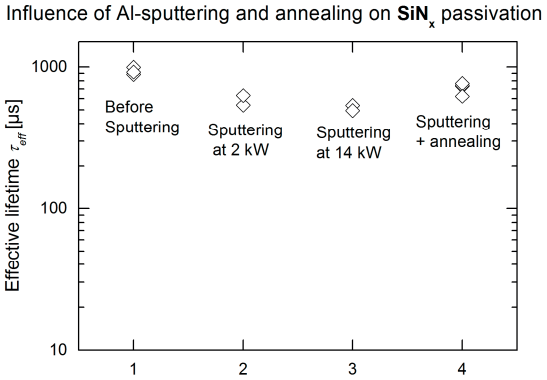

Figure 7.11: Measured effective carrier lifetime of SiN_x passivated test samples before and after DC-sputtering of 400 nm Al at low and high power and after forming gas annealing at 400 °C.

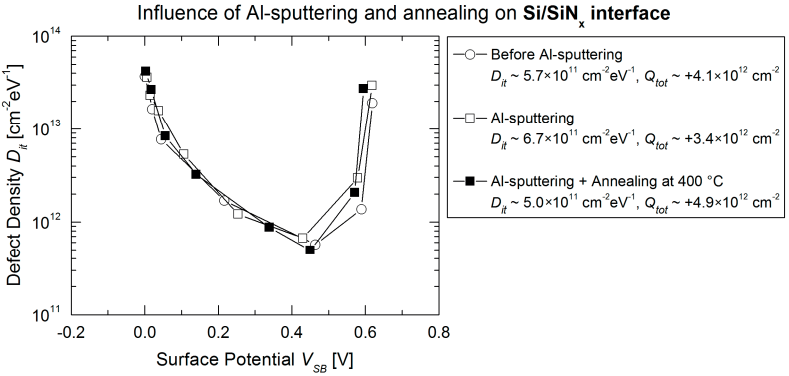

Figure 7.12: Measured defect density as a function of surface potential the samples with SiN_x passivation before and after DC-sputtering of 400 nm at 2 kW and after forming gas annealing at 400 °C.

From these results it can be concluded that by applying SiN_x instead of SiO_2 or Al_2O_3 as a passivation layer (if possible to adapt to the device) the sputter-induced damage can be avoided as in the nPERT solar cells developed in this thesis.

7.3 Summary and conclusion

In this chapter the impact of aluminum sputtering deposition on the passivation quality of SiO_2, Al_2O_3/SiN_x and SiN_x passivation of *n*-type silicon is investigated. This is done by measuring the effective carrier lifetime τ_{eff} by MWPCD method as well as the total charge density Q_{tot} and interface trap density D_{it} by COCOS method. It is observed that the effective carrier life time after sputtering aluminum on SiO_2 and Al_2O_3 passivated samples is fully degraded whereas by sputtering aluminum on SiN_x passivated samples (as for the rear-side of the nPERT solar cells developed in this thesis) there is only marginal degradation. The results of total charge and interface trap density correlates also very well with the effective carrier lifetime results. A significant increase in D_{it} and positive Q_{tot} is observed after aluminum sputtering on SiO_2 and Al_2O_3 passivated samples which indicates that the degradation in effective lifetime is due to a damaged silicon-passivation interface. Furthermore, it is also observed that by sputtering at higher power the degradation decreases due to a dynamic annealing since maximal substrate temperature is higher when the sputtering power increases. The COCOS results of the SiN_x passivated samples show no significant change of the interface properties after sputtering deposition of aluminum which also correlates very well the effective carrier lifetime results. In order to understand the origin of the radiation-hardness of SiN_x passivation, further detailed investigations with another methods such as FTIR or similar methods are needed.

8 Cell results of front-junction nPERT solar cells

In this chapter, cell results of five cell batches of large-area front-junction nPERT solar cells featuring screen-printed front-side and PVD rear-side metallization developed in this thesis are shown. The focus of these cell batches was rear-side metallization issues. The impact of spiking, contact formation, back-side reflectance and lateral conductance of aluminum-based PVD metallization is investigated. The obtained cell results are compared with the simulation and experimental results of test samples shown in the previous chapters.

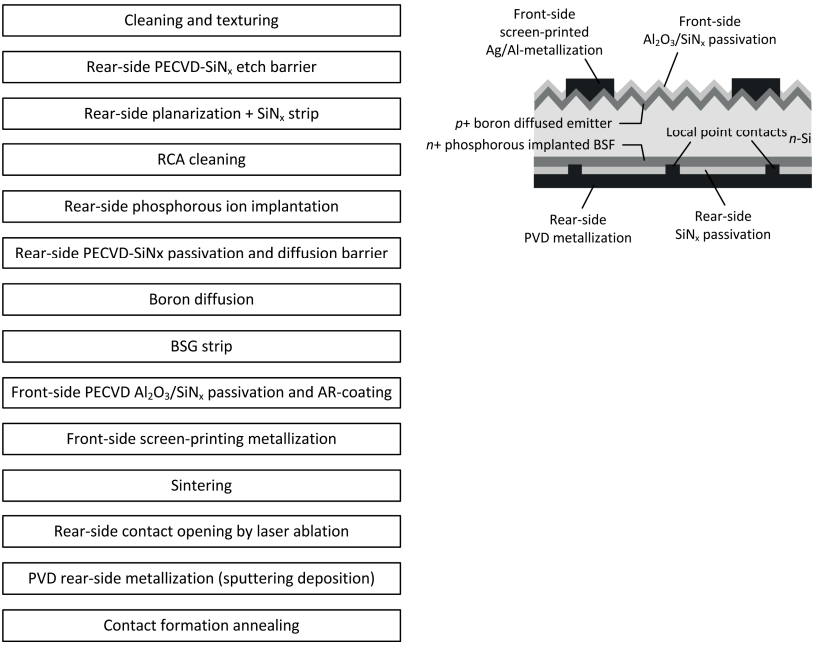

Figure 8.1: Process sequence (left) and cell structure (right) of the large-area front-junction nPERT solar cells developed in this work.

All solar cells are fabricated on 156 × 156 mm² pseudo-square *n*-type Cz-Si wafers with an initial thickness of 180 µm and a bulk resistivity around 4 Ωcm

using the cell structure and process sequence shown in Figure 8.1. The as-cut silicon wafers are first textured and cleaned. Afterwards the front-side is capped with silicon nitride as etching barrier in order to planarize the rear-side in damage-etch solution. After that, the silicon nitride etch barrier is stripped in HF solution and the wafers undergoes standard RCA cleaning sequence. After the cleaning sequence, the rear-side is phosphorous doped by ion implantation and passivated with 70 - 80 nm PECVD SiN_x. The rear-side SiN_x serves also as a diffusion barrier in the following boron diffusion process. After the boron diffusion and the subsequent high temperature co-anneal process the front-side boron emitter is formed. The co-anneal process also causes the implanted phosphorous on the rear-side to be driven-in so that the back surface field is also formed. After the boron diffusion and the co-anneal process the wafers are dipped in HF solution to strip the grown boron silicate glass (BSG) during the diffusion process to order to passivate the front surface. The front surface is passivated with PECVD Al_2O_3/SiN_x stack. After passivating the front surface a silver/aluminum paste is screen-printed on the front-side. Afterwards the screen-printed wafers undergo high temperature firing process in order to sinter the screen-printed front-side metallization as well as to activate the front- and rear-side passivation. After the firing process the rear-side metallization is fabricated. First the point contacts are opened by VIS picoseconds laser ablation and afterwards the metallization is deposited by sputtering deposition technique using the SOLARIS 6 system described in Chapter 3. Finally, the cells are tempered at various temperatures in order form an ohmic metal-semiconductor contact on the rear-side. Selected results of the various cell batches are published in [88], [49] and [76].

8.1 One-layer aluminum rear-side metallization (Batch-1 to Batch-4)

8.1.1 Batch-1: Influence of rear-side capping SiO_2 on current generation

In this batch, the improvement of current generation through capping SiO_2 layer on rear-side SiN_x passivation is investigated. In Chapter 6, it was shown that the internal reflection on the rear surface can be improved by using a 210-nm-thick SiO_2 capping layer on the SiN_x rear-side passivation (Figure 6.16). The results

of the reflection samples showed that the back-side reflectance R_b is improved by about 1.12 $\%_{rel}$ by using a capping 210 nm SiO_2 layer which would result in an enhancement of J_{sc} by about 0.9 $\%_{rel}$ (Table 6.3). To investigate the impact of the capping SiO_2 layer on current generation of large-area front-junction nPERT solar cells, two cell groups were fabricated featuring 70 nm SiN_x and 70 nm SiN_x/ 210 nm SiO_2 rear-side passivation, respectively. The efficiency and short-current density results are shown in Table 8.1. The results show that by applying a capping 210 nm SiO_2 the short current density could be increased by about 0.29 mA/cm² which means a relative improvement of about 0.75 $\%_{rel}$ which is in a good agreement with the predicted 0.9 $\%_{rel}$ of the test samples' results (Table 6.3). The current generation enhancement resulted in an efficiency improvement of about 0.43 $\%_{rel}$.

Table 8.1: Cell results of front-junction nPERT solar cells with and without a capping 210 nm SiO_2 layer on 70 nm SiN_x passivation.

70 nm SiN_x		70 nm SiN_x / 210 nm SiO_2		Gain through SiO_2 cap	
J_{sc} (mA/cm²)	η (%)	J_{sc} (mA/cm²)	η (%)	ΔJ_{sc} ($\%_{rel}$)	$\Delta\eta$ ($\%_{rel}$)
38.51 ± 0.05	18.47 ± 0.09	38.80 ± 0.09	18.55 ± 0.13	0.75 ± 0.03	0.43 ± 0.06

8.1.2 Batch-2: Influence of rear doping profile and thermal stress on cell performance

The aim of this batch was to investigate the contact-formation of aluminum metallization and its influence on cell characteristic for various rear-side back surface fields. Three different back surface fields are used with mainly varying BSF depth. The BSF depth was varied by varying the implant dose. The solar cells featuring these BSF profiles underwent the same co-anneal (drive-in) process. Deeper doping profiles should be less sensitive to spiking damage than shallow ones [48] as aluminum spikes are expected to be formed after contact-formation annealing as observed in the test samples in Chapter 4. The rear-side of the cell was metallized by sputtering deposition of a 700 nm PVD-Al layer at 14 kW using the SOLARIS 6 system with the metallization process 1 of

Table 3.1. Afterwards, contact formation annealing steps from 325 °C to 425 °C in N_2-ambient each for five minutes were progressively applied. The measured cell parameters before and after tempering the cells are presented in Figure 8.3 (average of 4 cells per group).

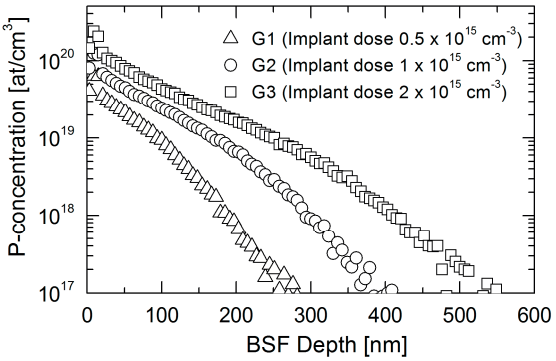

Figure 8.2: Doping profiles of the investigated back surface fields of Batch-2.

Spiking-induced damage

The cell results indicate a degradation of cell efficiency which correlates with increasing thermal stress and reduced back surface field depth (G3 → G1), which is to the knowledge of the author not previously published. The solar cells with the deeper BSF are thermally more stable than the cells with the shallower one. Both aspects (increased degradation with decreased BSF depth as well as with increased contact formation annealing temperature) indicate that the degradation can be due to aluminum spiking through the back surface field. For higher thermal budgets more silicon diffuses into the aluminum layer and forms deeper spikes due to a higher solubility limit or a deeper BSF prevents the spikes from reaching beyond the highly doped region. Therefore, it is assumed that aluminum spikes are the origin of this degradation and the thermal instability. It can be concluded from this batch that using deeper doping profiles can protect the cell from spiking-induced damage. In batch-5 (section 8.2), barrier metallization against spiking-induced damage is investigated (Al-Si/Al and Ti/Al).

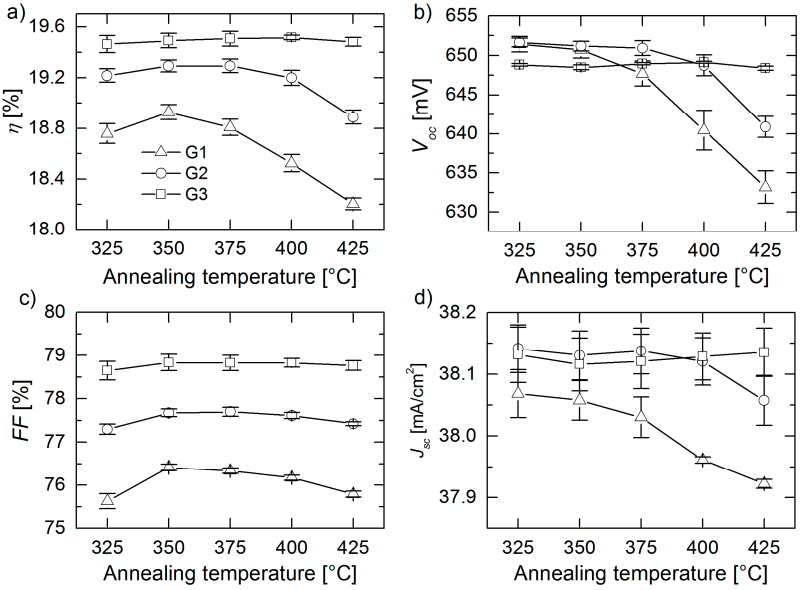

Figure 8.3: (a) Efficiency, (b) open-circuit voltage, (c) fill factor, and (d) shortcircuit current density of the nPERT solar cells of Batch-2.

In order to confirm that the damage under thermal stress is mainly due to J_{01} recombination losses, Suns-V_{oc} measurements [119] were carried out on one thermally stressed damaged cell (V_{oc} ~ 633 mV) and one undamaged cell (V_{oc} ~ 647 mV) both from G1. The JV-characteristic of both cells obtained from Suns-V_{oc} are shown in Figure 8.4. From the fits of these curves it is found out that the recombination current J_{01} – which gives information about recombination in the base, emitter or at the surfaces – is increased significantly after thermally stressing the cell at 425 °C. Therefore, the damage originates from J_{01} recombination losses. SEM images of the rear-side after back etching the aluminum layer shows significantly more spikes on the rear-side of the thermally stressed solar cell in comparison to the not tempered solar cell which indicates that the recombination losses originate from the rear-side and are very likely due to spiking-induced damage.

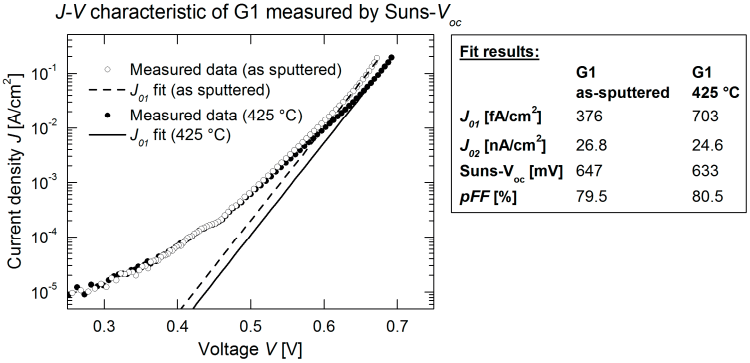

Figure 8.4: Suns-V_{oc} measurement of a non-tempered solar cell (hollow symbols) and a solar cell tempered at 425 °C (filled symbols).

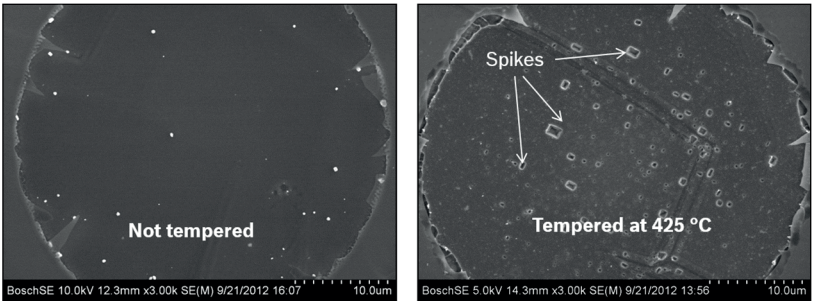

Figure 8.5: SEM images after back etching the aluminum layer of non-tempered solar cell (right) and a solar cell tempered at 425 °C.

Fill factor analysis and contact-formation

In order to verify the fill factor losses of the cells, the quantities (*pFF* - *FF*) and (*FF*$_0$ - *FF*) are calculated from the measured data. The pseudo fill factor *pFF* is the fill factor free of series resistance losses and thus the term (*pFF* - *FF*) is the fill factor loss due to series ohmic losses [120]. The term (*FF*$_0$ - *pFF*) is the fill factor loss due to parallel resistance losses as well as non-ideality losses [120]. Non-ideality losses are recombination losses where the ideality factor does not equals 1 (e.g. in the space charge region of a p-n junction). The fill factor analysis is shown in Figure 8.6.

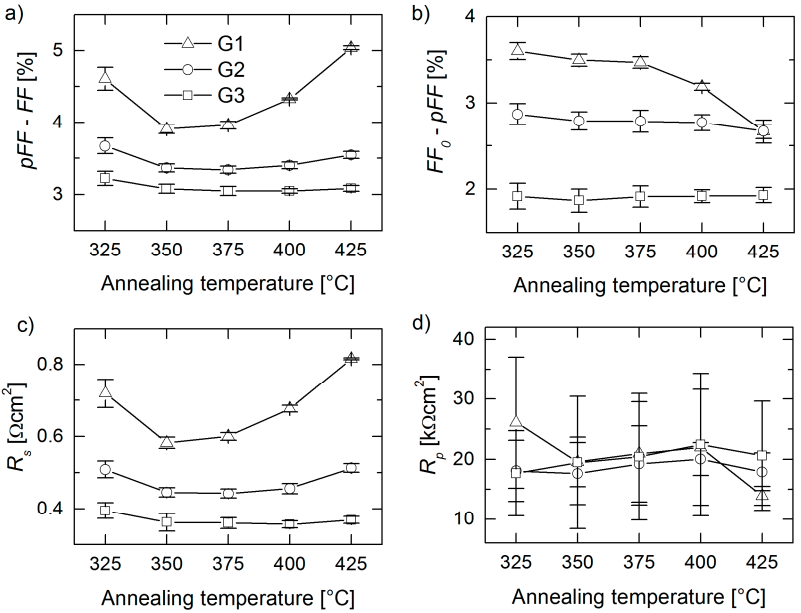

Figure 8.6: Fill factor analysis of Batch-2.

The (*pFF-FF*) and R_s-curves correlate very well with each other and reach sufficiently low minimum values at 350 °C which indicates the formation of a good ohmic contact of the rear-side. However, when the thermal stress increases, R_s and *pFF-FF* increase as well especially for G1 with the shallowest BSF. Thus, aluminum spiking causes also a reduction in contact resistance for very shallow junctions. Furthermore, the difference between the various groups in (*pFF-FF*) is as not high as the difference the difference between them in *FF*. The difference Δ(*pFF-FF*) between G2 and G3 at 350 °C is about 0.3 % (Figure 8.6-a) whereas Δ*FF* between these two groups is about 1.3 % (Figure 8.3-c). In order to find the reason of the high Δ*FF* between the cells with various BSF, the quantity $FF_0 - pFF$ is calculated from the measured data and compared with the parallel resistance results. From these data it is found out that the main fill factor losses are mainly due to non-ideality losses, since the difference Δ(FF_0-*pFF*) between the groups is significant while the parallel

resistance of all groups are more of less the same. $\Delta(FF_0\text{-}pFF)$ between G2 and G3 is almost 1% which is very high and indicates that the co-anneal process is probably not sufficient to anneal all the damage caused to the cell after the implant process of the BSF on the rear especially for less doped ones. This issue was optimized in the following batches where a longer co-anneal process is used. The longer co-anneal process resulted in a significant reduction of the non-ideality losses.

8.1.3 Batch-3: Influence of rear contact spacing on current-voltage characteristic

The aim of this batch was mainly to determine rear specific contact from cell results and compare it to specific contact resistance obtained from the test samples. Therefore, front-junction nPERT solar cells with rear-side Al-PVD metallization similar to the cells of Batch-2 was fabricated. An optimized longer co-anneal process was used in order to anneal the implant damage and reduce non-ideality losses. Furthermore, a long co-anneal process results in a deeper BSF profile which in return means less damage due to aluminum spiking. The resulted new BSF profile with an implant dose of 1×10^{15} cm^{-3} is shown in Figure 8.7 along with the old BSF profile with the same implant dose and thus the same sheet resistance (G2 from Batch-2). Furthermore, a capping SiO_2 layer is introduced to the rear-side of this batch in order to improve current generation.

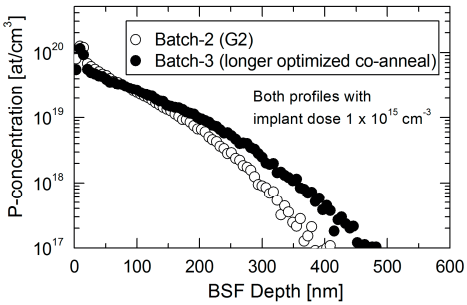

Figure 8.7: Doping profiles of the optimized back surface fields of Batch-3 with a longer co-anneal process along with the old BSF profile of Batch-2 with the same implant dose. The sheet resistance of both profiles is between 75 and 80 Ω/sq.

The cell results are shown in Figure 8.8. Through the optimized longer co-anneal process and the addition of a capping SiO_2 layer to the rear-side, significantly higher cell efficiencies could be obtained. The longer co-anneal process resulted in an improvement in V_{oc} (mainly due to less surface dopant concentration and thus better passivated rear surface) and *FF* (mainly due to less non-ideality losses). The fill factor correlation with the rear-contact spacing is due to ohmic losses. The fill factor decreases with increasing rear contact spacing due to lateral ohmic losses and contact resistance losses of the rear-side. Thus, the specific contact resistance of rear-point contacts can be obtained by fitting the data with simulation. The correlation of rear contact spacing with V_{oc} is the opposite: V_{oc} increases lightly with increasing pitch due to increased passivation area. The best cell results could be achieved at a rear contact spacing between 450 and 560 µm compromising ohmic and recombination losses.

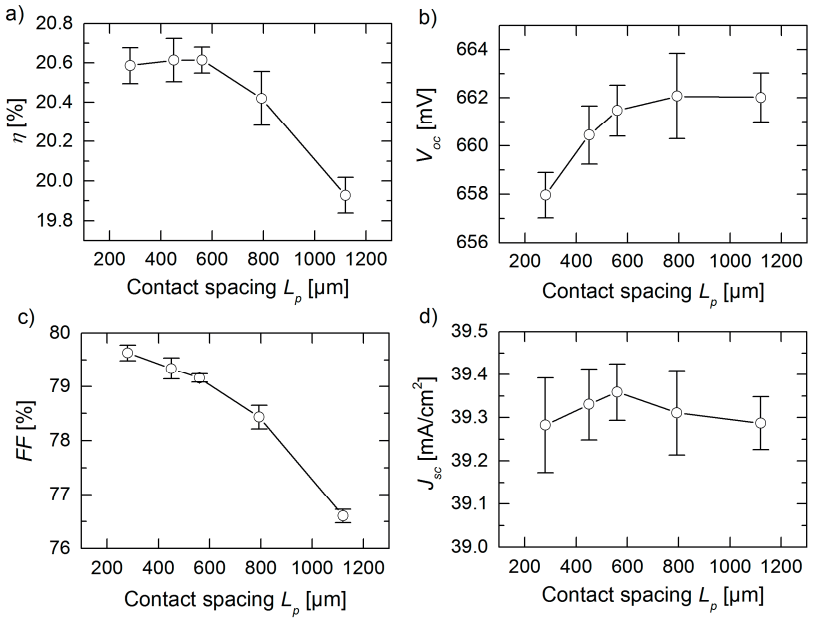

Figure 8.8: (a) Efficiency, (b) open-circuit voltage, (c) fill factor, and (d) short-circuit current density of the nPERT solar cells of Batch-3.

Fill factor analysis

Similar to the fill factor analysis of the previous Batch-2, the quantities (*pFF-FF*), R_s, (FF_0-*pFF*) and R_p are plotted for the cells of this Batch-3 in Figure 8.9. The optimized co-anneal process resulted in a very remarkable improvement of (FF_0-*pFF*) from about 3 $\%_{abs}$ (Figure 8.6) to about 1 $\%_{abs}$ (Figure 8.9) which resulted in the improved cell efficiencies. Furthermore, the fill factor dependency with rear contact spacing correlates very well with (*pFF-FF*) and R_s data which indicates the ohmic losses due to increased rear contact spacing.

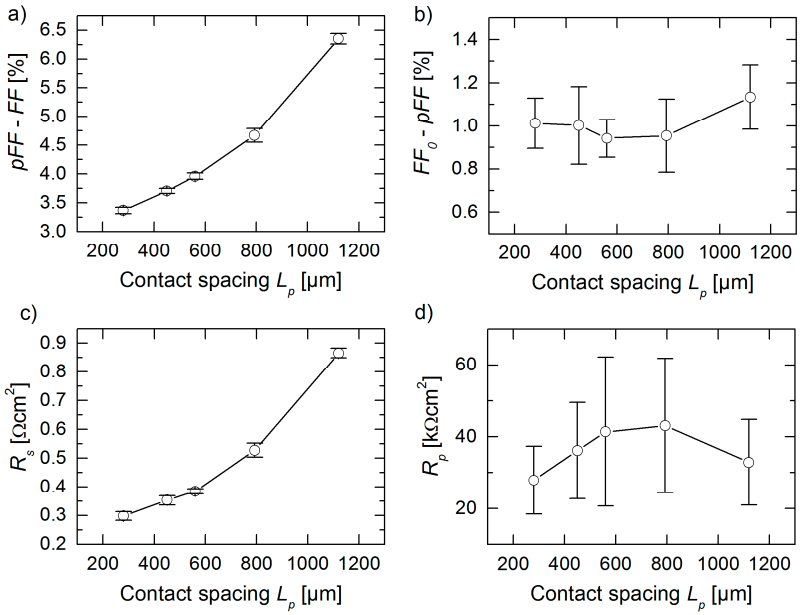

Figure 8.9: Fill factor analysis of Batch-3.

In order to obtain specific contact resistance of the rear side metallization from cell data, the fill factor data are fitted with numerically simulated cell results. For the numerical 3D device simulations, the same cell structure is used and calibrated with the experimental cell data. An external series resistance to the simulated device was included in order to calibrate the fill factor of the simulated device with the cell data. The calibration was done with cells at contact spacing

of 280 µm by varying the external series resistance of the simulated device until the fill factor of the simulated device matches the one of the real solar cells. Afterwards, the external series resistance was kept at the calibrated value and the fill factor of the rest devices was simulated as a function of rear contact spacing. The simulations were done for various rear specific contact resistance values. The simulation results as well as the experimental ones are shown in Figure 8.10. The experimental results could be fitted with numerical simulation results using a rear specific contact resistance value of about 0.15 mΩcm² (Figure 8.10, triangle symbols). This rear specific contact resistance value is in the same order of the one achieved from the test samples (0.09 mΩcm²).

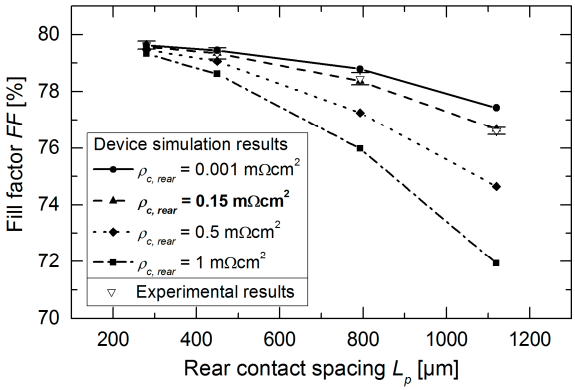

Figure 8.10: Simulated and experimental cell results of nPERT solar cells with screen printed front side metallization and PVD-Al rear side metallization.

8.1.4 Batch-4: Influence of aluminum layer thickness on series ohmic losses

The simulation results of the efficiency loss due to lateral ohmic loss in the metallization layer (section 2.3.1, Figure 2.12) showed that an aluminum layer of about 1.8 µm layer thickness with bulk resistivity of 2.67 Ωcm is required to keep the efficiency loss below 0.05 $\%_{abs}$. Real evaporated or sputtered metal layers of some hundred nanometer layer thickness usually have a slightly higher resistivity than of bulk materials. Physical vapor deposited aluminum layers in this thickness range usually have a resistivity around 3 Ωcm [45] which is also

observed in the aluminum layers deposited by the SOLARIS 6 system (Table 3.1).

In order to verify the simulation results, nPERT solar cells with sputtered aluminum rear-side metallization of various thicknesses were fabricated. The nPERT solar cells were produced with the same process sequence as in Batch-3. The rear contact-radius was about 20 µm and the contact spacing 450 µm. The current-voltage characteristic of the cells as well as the busbar-busbar and the sheet resistance of the rear-side metallization were measured.

The thicknesses of the aluminum layers were about 0.7, 1.4 and 2.1 µm with eight solar cells for each metallization thickness. The thickness of the metal layers were verified by measuring the weight of monitoring wafers before and after the deposition of the metal layers as described in section 3.2. The aluminum layers were deposited using processes 1, 2 and 3 of Table 3.1.

The results of the busbar-busbar and the sheet resistance of the rear-side metallization of the fabricated cells are shown in Table 8.2 for each group. A non-uniformity of about 5 % were obtained for all three groups. The busbar-busbar resistance values of the reference cells with screen printed aluminum (from the production) is higher than the busbar-busbar resistance of G2 and G3 with sputtered aluminum, which shows the higher conductance quality of PVD-Al compared to much thicker (usually about 10 times thicker) screen-printed and sintered aluminum pastes.

Table 8.2: R_{bb} and R_{sh} results of the solar cells.

Cell group	G1	G2	G3	Reference
Metallization process	1	2	3	Standard production
Layer thickness (µm)	0.7	1.4	2.1	20 - 30 µm
Busbar-busbar resistance (mΩ)	13.40 ± 0.05	6.61 ± 0.02	4.40 ± 0.03	9.41 ± 1.42
Sheet resistance (mΩ) (average of 49 points/wafer)	42.43 ± 1.56	21.00 ± 0.72	14.03 ± 0.47	---
Non-uniformity of R_{sh} (%)	5.20 ± 0.14	4.71 ± 0.11	4.66 ± 0.20	---

Figure 8.11 shows fitted curves of the measured busbar-busbar and sheet resistance as a function of layer thickness by using equations (2.16) and (2.17). The obtained resistivity from the fit of R_{bb} data was 2.8 µΩcm and from the fit of R_{sh}-data was 2.96 µΩcm. Compared to literature values of sputtered Al layers [45], the later seems to be more a reliable value and was assumed later for the fits of the series resistance, fill factor and efficiency of the solar cells.

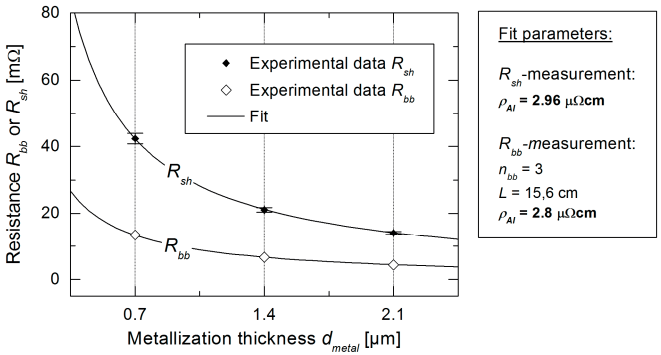

Figure 8.11: Busbar-Busbar and sheet resistance results of the rear-side metallization of the fabricated nPERT solar cells with various rear-side aluminum layer thicknesses.

The measured series resistance, fill factor and efficiency of the solar cells as well as the corresponding fits are shown in Figure 8.12. The series resistance was fitted by using equation (2.24), the fill factor by equation (2.25) and the efficiency by equation (2.26). The results of the series resistance show that the cell data are in a very good agreement with the fitted curves (coefficient of determination R^2 ~ 0.97). Due to measurement fluctuations of the fill factor and efficiency, the coefficient of determination R^2 of the fitted fill factor data is only ~ 0.8 and R^2 of the fitted efficiency data is ~ 0.86.

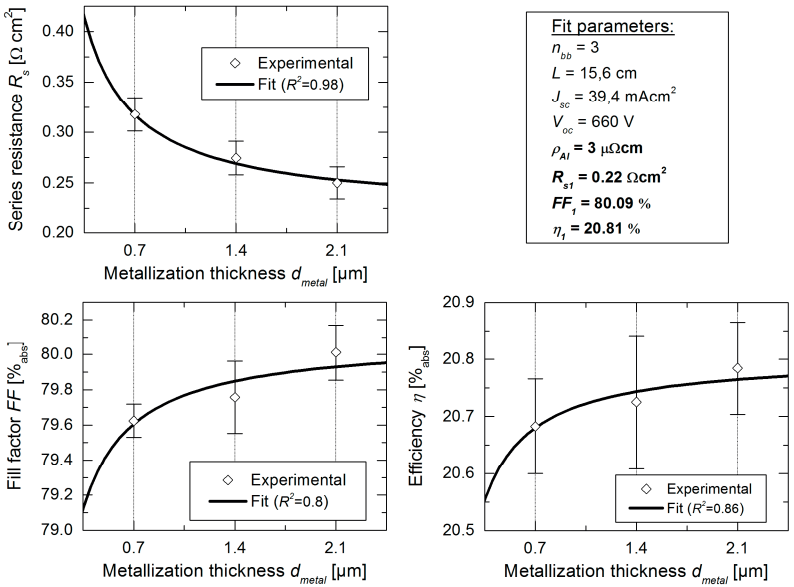

Figure 8.12: Series resistance, fill factor and efficiency results of the front-junction nPERT solar cells with PVD-aluminum rear-side metallization of various thicknesses.

The solar cell with the highest cell efficiency of 20.88 %$_{abs}$ is also independently confirmed by Fraunhofer ISE CalLab PV Cells (Table 8.3). To the knowledge of the author, this is the highest reported cell efficiency for large-area nPERT solar cells featuring at least one screen-printed side.

Table 8.3: Current-voltage characteristics of the best solar cell measured by Frauenhofer ISE CalLab PV Cells.

Cell ID	I_{sc} [A]	V_{oc} [mV]	*FF* [%]	η [%]
G4_1	9.515	663.1	79.96	20.88

8.2 Multi-layer aluminum-based rear-side metallization (Batch 5)

In order to prove the hypothesis of spiking-induced damage of aluminum metallization (section 8.1.2), aluminum-based barrier metallization Al-Si/Al and Ti/Al are investigated. In Chapter 4, it was shown that the use of diffusion barriers as Al-Si or Ti can suppress aluminum spiking. Therefore, three different rear-side aluminum-based metallization variants were used: 2-µmAl, 450-nm Al-Si/1.8-µmAl, and 25-nm Ti/2-µm Al. A thickness of the Al-Si layer of 450 nm was chosen to withstand thermal stress up to 425 °C. The aluminum layer for all cells was sputtered with the high-power sputtering process to ensure in situ contact formation annealing. The solar cells were then thermally stressed at 400 °C and 425 °C for 5 min to study their thermal stability. The measured cell data are shown in Figure 8.13 (average of five cells per group).

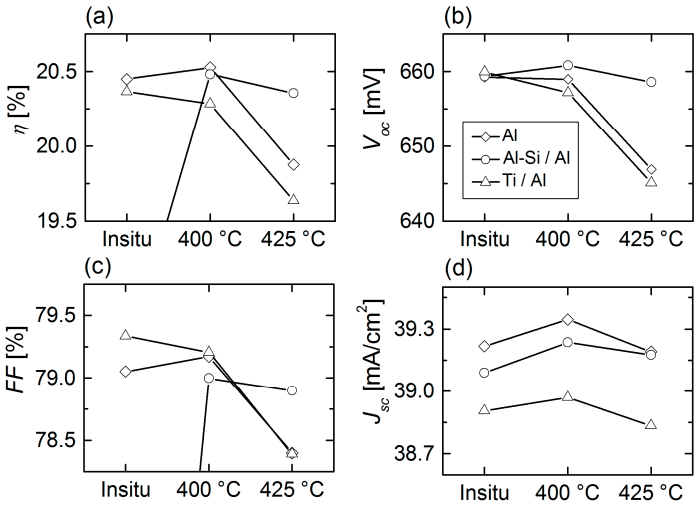

Figure 8.13: (a) Efficiency, (b) open-circuit voltage, (c) fill factor, and (d) shortcircuit current density of the nPERT solar cells of Batch-5.

Because of the optimized deeper BSF profile with the longer co-anneal process, no cell significantly degraded after tempering at 400 °C. However, a slight change to 425 °C causes major damage to the cells (>10 mV degradation of V_{oc}) with Al or Ti/Al rear-side metallization, while the cells with Al-Si/Al remain stable (V_{oc} around 660 mV). To analyze the origin of this degradation, the saturation current density J_{01} from the Suns-V_{oc} measurement using a two-diode fit similar to Batch-2. The results are shown in Figure 8.14 along with SEM images of the rear surface after back etching of the rear-side metallization.

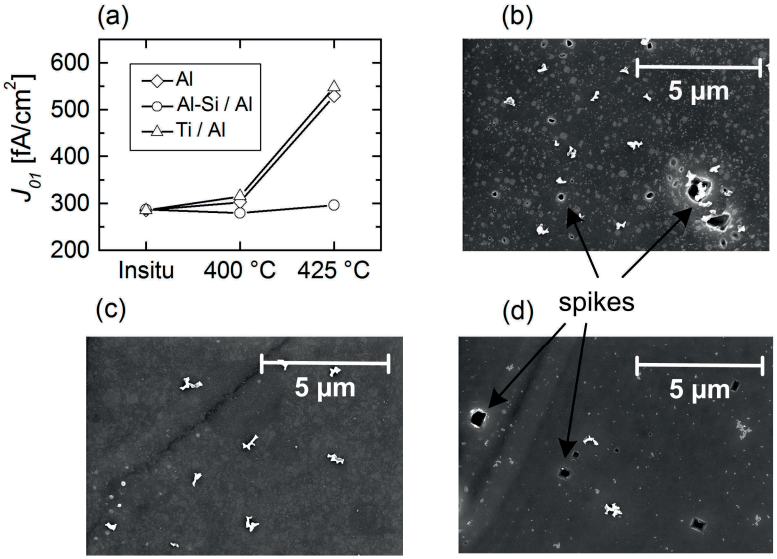

Figure 8.14: (a) Saturation current density of all cells and SEM images after metallization removal of (b) Al, (c) Al–Si/Al, and (d) Ti/Al back-side metallization of the cells used in Batch-2.

The increase in J_{01} of the cells with Al and Ti/Al metallization correlates very well with V_{oc} results. As all cells are identical except for the rear-side metallization, we can conclude that V_{oc} degradation is due to recombination losses caused by the rear-side metallization. SEM images of the rear side of the cells after metal layer removal are also in very good agreement with these results. Spike formation for Al and Ti/Al metallization (Figure 8.14-b and -d) can be seen in contrast to Al–Si/Al metallization, where no spikes were observable

(Figure 8.14-c) after heating the cells up to 425 °C. The thermal instability of the Ti/Al metallization is probably caused by an insufficient Ti layer thickness or layer quality. As predicted by the simulation in Figure 2.14, the fill factor data of the cells with Ti as a contact metal show only a slight benefit of the very low contact resistance of Ti for this device (Figure 8.13-c). Furthermore, the low IR reflectivity of Ti causes a major optical loss and, thus, a low short-circuit current density of the cell (Figure 8.13-d). The fill factor of the cells at 400 °C with Al-Si/Al is slightly lower than that with Al or Ti/Al metallization (Figure 8.13-c) due to a slightly higher contact resistance, which correlates well with the contact resistance obtained from the test samples in Chapter 5.

8.3 Summary and conclusion

In this chapter, cell results of five cell batches of large-area front-junction nPERT solar cells featuring screen-printed front-side and PVD rear-side metallization developed in this thesis were presented. The focus of the cell batches was mainly rear-side metallization related issues. It was shown that aluminum metallization causes spiking induced damage under thermal stress (e.g. during contact formation annealing). This damage can be overcome either by using a deeper doping profiles or by using metal barriers between the aluminum and the silicon wafer to suppress silicon diffusion into the aluminum layer. However, by using Ti as a contact metal, the current generation of the cell decreases significantly which is due to the poor IR reflectivity of Ti which is in an excellent agreement with the results obtained from the test samples. Thus there is no benefit of using Ti as a contact layer despite its very low contact resistance for BSF with N_s~6.9 x 10^{19} cm^{-3} and R_{sh}~75 Ω/sq. The solar cells with Al-Si/Al metallization showed cell results as good as aluminum metallization but with slightly higher V_{oc} and more thermal stability. To the knowledge of the author, spiking-induced damage of nPERT solar cells with PVD metallization and the use of Al-Si/Al stack against aluminum spiking in general is not previously published. Furthermore, the simulation results concerning lateral ohmic losses and contact resistance losses could be confirmed with the cell results. An aluminum layer of thickness around 2 µm is needed to reduce the lateral ohmic losses to negligible level. A specific contact resistance of

1.5×10^{-4} Ωcm^2 could be obtained from cell results which is in a good agreement with the one obtained from test samples (0.9×10^{-4} Ωcm^2). Finally, a best cell efficiency of 20.88 % could be obtained with large-area nPERT solar cells featuring PVD-Al which is also independently confirmed by Fraunhofer ISE CalLab PV Cells. To the knowledge of the author, this is the highest reported cell efficiency for large-area nPERT solar cells featuring at least one screen-printed side.

9 Thesis summary and outlook

This thesis deals with physical-vapor-deposited rear-side metallization for large-area front-junction *n*-type passivated emitter rear totally diffused (nPERT) silicon solar cells as a replacement for the state of the art screen-printing metallization technology. Screen-printed aluminum is perfectly suited to *p*-type solar cells as it forms both the back surface field BSF and the metal-semiconductor contact during sintering. However, for advanced *n*-type cell structures (e.g. nPERT), screen-printed aluminum has its limitation contacting *n*-type silicon. The main drawback of screen-printed aluminum is that it cannot form an ohmic electrical contact to *n*-type silicon because it will form a p^+-doped silicon layer during sintering. Many different ways can be done in order to overcome this issue for double-side contacted *n*-type silicon solar cells as for example by using the expensive screen-printed silver. More promising approach is to replace screen-printing metallization technology with another one such as physical vapor deposition technology (PVD) which is the focus of the thesis.

Rear-side metallization losses and its requirements were defined at the beginning and investigated throughout the thesis for various common PVD metals in order to develop PVD rear-side metallization for high efficiency large-area front-junction nPERT solar cells featuring front-side screen-printed metallization. The main aim of these investigations was to define the best suited PVD materials for rear-side metallization. The impact of the various PVD metal layers on the electrical and optical losses of the device is investigated. The PVD metallization technology used in this thesis was planar magnetron sputtering using an Oerlikon SOLARIS 6 system. The SOLARIS 6 system and the metallization processes used in this work are presented in Chapter 3.

Since lateral conductance is thickness dependent, investigations on **lateral ohmic losses** were carried out at first in order to define the main conducting layer of the metallization. Based on simulations and cost calculations, it was found that aluminum is the most suited material as the main conducting layer of the rear-side metallization for full-area rear-side metallization, since it

compromises well between lateral ohmic losses and material cost (sections 2.3.1 and 2.5). The thickness of the aluminum layer required for sufficient current transport is found to be around 2 μm. Therefore, the rear-side metallization studied and developed in this thesis was an aluminum-based metallization.

After defining aluminum as the main conducting metallization layer of the rear-side metallization, the **contact formation process** of aluminum based metallization is studied in detail in Chapter 4. Spikes formation due to due to the high solubility and diffusivity of silicon in aluminum at 400 °C (contact formation annealing temperature) was observed when pure aluminum is used. Solutions to overcome **aluminum spiking** were presented and discussed. The state of the art approaches to suppress spike formation as the use of the sacrificial barrier titanium or one-layer Al-Si (1 at% Si) as well as a novel approach by using Al-Si/Al stack were investigated. Simulations as well as SEM structural investigations on Cz silicon wafers featuring the rear-side of nPERT solar cells were carried out in order to study the potential of these approaches against aluminum spiking. The results of these investigations showed that aluminum spiking can be overcome by the use of a sufficiently thick sacrificial spiking barrier like titanium. For a contact formation annealing at 400 °C for 5 min, a titanium layer thickness of at least 20 nm is required to suppress spike formation on Cz silicon wafers. SEM images of the samples with one layer 2--μm-thick Al-Si metallization showed a complete absence of aluminum spikes, however, with a strong silicon precipitation. Silicon precipitations are *p*-doped silicon and might cause an increase in contact resistance when applied to an n^+-doped silicon. The use of Al-Si/Al stack instead of one-layer Al-Si metallization resulted in a significant decrease of silicon precipitation combined with a suppression of aluminum spiking. The process simulation as well as the experimental results showed that an Al-Si layer thickness around 400 nm is required to suppress the formation of aluminum spikes as well as silicon precipitations for 2 μm Al metallization and a contact formation annealing at 400 °C. If the aluminum layer thickness or the thermal stress applied is different (e.g. for other applications than the one in this thesis), the thickness of the Al-Si must be adapted.

In Chapter 5, the **specific contact resistance** of the investigated aluminum-based rear-side metallization schemes (Al, Ti/Al stack, Al-Si/Al stack and Al-Si) on n^+-Si point contacts as for the rear side of front junction nPERT solar cells was determined. Two doping profiles and hence surface dopant concentrations were used. In order to determine the specific contact resistance of point contacts, a novel characterization method was developed which is applicable for specific contact resistance values > 0.01 mΩcm². The results showed that for lowly doped n^+-Si with a surface dopant concentration of 3.8×10^{19} cm^{-3} and a sheet resistance of 136 Ω/sq, one-layer Al-Si metallization will result in significant ohmic losses due to a very high specific contact resistance (around 5 mΩcm²). By using Al-Si/Al stack instead of one-layer Al-Si metallization the specific contact resistance can be reduced to about 2 mΩcm². This may result in a fill factor loss around 2 %$_{abs}$. The estimated specific contact resistance of the samples with pure Al metallization on the rear was found to be about five times lower that of Al-Si metallization with specific contact resistance values around 0.4 mΩcm². This may result in a marginal fill factor loss around 0.5 %$_{abs}$. Titanium showed the best results for contacting lowly doped n^+-Si with a specific contact resistance values around 0.15 mΩcm². Thus, for lowly doped n^+-Si, titanium as a contact layer seems to be the best choice. The experimental results of the samples with highly doped n^+-Si with a surface dopant concentration of 6.9×10^{19} cm^{-3} and a sheet resistance of about 75 Ω/sq showed that the estimated specific contact resistance for all metallization variants is lower the required rear specific contact resistance of nPERT solar cells with metallization fraction area as low as 0.5 % (< 0.3 mΩcm²). Furthermore, the results of all samples showed that there is no significant difference between as-sputtered and annealed samples which indicates that the sputtering process of aluminum at high power (14 kW) results in a sufficient dynamic annealing for in situ contact formation.

The **optical losses of rear-side metallization** are investigated in Chapter 6. In this chapter the impact of rear-side passivation and metallization layers on the rear-side reflectance and thus on the photocurrent-generation for silicon solar cells was investigated in detail. Various rear-side metallization schemes with Al, Al-Si, Ti or Ag as contact metals were investigated in combination with various

rear-side passivation layers. The results of these investigations showed that the use of Al-Si results in only negligible minor optical loss, especially when optically optimized passivation (e.g. SiN_x/SiO_2-stack with about 210 nm SiO_2 layer-thickness) is used. The use of Ti as a contact-layer, however, results in a non-negligible optical loss even if the optically optimized SiN_x/SiO_2 passivation is used, due to the poor reflectivity of Ti in the NIR spectral region. When Ti is used as a contact-metal the difference in rear-side reflectance is more than 6 $\%_{abs}$ compared to Al or Al-Si. This loss would result in a photocurrent-density loss of more than 0.3 mA/cm². Theoretical efforts by using 3D ray-tracing simulations in order to overcome the poor reflectivity of Ti by using sophisticated multi-layer passivation (e.g. Bragg-stack) were also carried out. The key result of these investigation showed that a Bragg-stack of order higher than five with a thick first layer (~ 600 nm) are required in order to reduce the optical losses to a negligible level, which is barely implementable in an industrial environment and is therefore not examined experimentally. Regarding Ag as a contact metal, it was shown that at least 50 - 60 nm Ag is required to benefit from its very high reflectivity, which is still cost intensive compared to Al metallization. Furthermore, the benefit from using thin Ag-layer as a contact metal is only beneficial for standard 70 nm SiN_x rear-side passivation. When optically optimized rear-side passivation is used (e.g. SiN_x/SiO_2 stack), the enhancement of rear-side reflectance by using Ag instead of Al is found to be very low (< 1 $\%_{abs}$).

The **recombination losses due to plasma irradiation** present in the sputtering chamber was investigated in Chapter 7. In this chapter the impact of aluminum sputtering deposition on the passivation quality of common passivation layers as SiO_2, Al_2O_3/SiN_x and SiN_x was investigated. This is done by measuring the effective carrier lifetime by MWPCD method as well as the total charge density and interface trap density by COCOS method. It is observed that the effective carrier life time after sputtering aluminum on SiO_2 and Al_2O_3 passivated samples is fully degraded whereas by sputtering aluminum on SiN_x passivated samples (as for the rear-side of the nPERT solar cells developed in this thesis) there is only marginal degradation. The results of total charge and interface trap density correlated very well with the effective carrier lifetime

results. A significant increase in total charge density and positive total charge density is observed after aluminum sputtering on SiO_2 and Al_2O_3 passivated samples which indicates that the degradation in effective lifetime is due to a damaged silicon passivation interface. Furthermore, it is also observed that by sputtering deposition of aluminum at higher power the degradation decreases due to a dynamic annealing, since maximal substrate temperature is higher when the sputtering power increases. The COCOS results of the SiN_x passivated samples show no significant change of the interface properties after sputtering deposition of aluminum which also correlates very well the effective carrier lifetime results.

Finally in Chapter 8, the **cell results of large-area front-junction nPERT solar cells** featuring screen-printed front-side and PVD rear-side metallization developed in this thesis were presented. The focus of the cell batches was mainly rear-side metallization related issues. It was shown that aluminum metallization causes spiking induced damage under thermal stress (e.g. during contact formation annealing). This damage can be overcome either by using deeper doping profiles or by using metal barriers between the aluminum and the silicon wafer to suppress silicon diffusion into the aluminum layer. However, by using Ti as a contact metal, the current generation of the cell decreases significantly which is due to the poor IR reflectivity of Ti which is in an excellent agreement with the results obtained from the test samples. Thus there is no benefit of using Ti as a contact layer despite its very low contact resistance for back surface field with a surface dopant concentration of 6.9×10^{19} cm^{-3} and a sheet resistance of about 75 Ω/sq. The solar cells with Al-Si/Al metallization showed cell results as good as the results with pure aluminum metallization but with slightly higher V_{oc} and significantly more thermal stability. To the knowledge of the author, spiking-induced damage of nPERT solar cells with PVD metallization and the use of Al-Si/Al stack against aluminum spiking is not previously published. Furthermore, the simulation results concerning lateral ohmic losses and contact resistance losses could be confirmed with the cell results. An aluminum layer of thickness around 2 μm is needed to reduce the lateral ohmic losses to negligible level. A specific contact resistance of about 1.5×10^{-4} Ωcm^2 could be obtained from cell results which is in a good agreement with the one obtained from test

samples (0.9×10^{-4} Ωcm^2). Finally, a best cell efficiency of 20.88 % could be obtained with large-area nPERT solar cells featuring PVD-Al which is also independently confirmed by Fraunhofer ISE CalLab PV Cells. To the knowledge of the author, this is the highest reported cell efficiency for large-area nPERT solar cells featuring at least one screen-printed side.

Future work may aim at carrying out more investigations on plasma-induced damage of passivation layers in order to understand the origin of the radiation-hardness of SiN_x passivation. Furthermore, the various aluminum-based PVD-metallization schemes may be tested on other solar cell types. In addition, future works on module level such as studying the interconnecting of solar cells with aluminum-based rear-side metallization and screen-printed front-side metallization may be carried out. Interconnecting techniques such as bonding or anisotropic conductive films (ACF) might be interesting to investigate for aluminum-based PVD-metallization, since aluminum is not solderable with conventional soldering techniques. In soldering techniques additional solderable capping layers (e.g. NiV/Ag) are required which can be spared by other interconnecting techniques.

10 Deutsche Zusammenfassung (German summary)

Diese Arbeit befasst sich mit der physikalischen Gasphasenabscheidung (PVD) als alternatives Herstellungsverfahren einer Rückseitenmetallisierung für industrielle nPERT Siliziumsolarzellen (engl.: *n*-type passivated emitter rear totally diffused). Für *p*-Typ Siliziumsolarzellen wird – so der Stand der Technik – Siebdruck eingesetzt, um eine Aluminiumschicht als Rückseitenmetallisierung herzustellen. Aluminium bildet während des Hochtemperatur-Sinterprozesses sowohl das p^+ hochdotierte Rückseitenfeld (engl. back surface field, BSF) als auch einen ohmschen Metall-Halbleiter-Kontakt auf der Rückseite der Solarzelle. Für *n*-Typ Siliziumsolarzellen hingegen ist eine gedruckte Aluminiumschicht nicht immer geeignet. Eine gedruckte Aluminiumschicht kann wegen der p^+-Schicht keinen ohmschen Kontakt zu n^+-Silizium bilden. Um einen ohmschen Kontakt zwischen einer gedruckten Metallisierung und n^+-Silizium zu gewährleisten, müssen andere Pasten verwendet werden wie z. B. teure Silberpasten. Ein anderer vielversprechender Ansatz, um n^+-Silizium zu kontaktieren, ist der Einsatz anderer Metallisierungstechnologien wie z. B. die physikalischen Gasphasenabscheidung (PVD); diese Technologie bildet den Schwerpunkt der vorliegender Arbeit.

Am Anfang der vorliegenden Arbeit wurden die relevanten Verluste bei der Konzeption einer Rückseitenmetallisierung analysiert, um die geeignetsten PVD-Materialien für eine effiziente Rückseitenmetallisierung einer nPERT-Solarzelle zu finden. Dazu wurden die Auswirkungen der verschiedenen PVD-Metallschichten auf die elektrischen und optischen Verluste der Solarzelle untersucht. Das verwendete PVD-Verfahren war das Magnetron-Sputtern.

Untersuchungen an lateralen ohmschen Verlusten wurden zunächst durchgeführt, um die hauptleitende Schicht zu definieren. Auf Grundlage von Simulationen und Kostenkalkulationen wurde festgestellt, dass Aluminium sich am besten dafür eignet, da Aluminium sich als ein guter Kompromiss zwischen lateralen ohmschen Verlusten und Materialkosten erwies. Die Untersuchungen

zeigten, dass die erforderliche Schichtdicke für eine vollflächige PVD-Al Rückseitenmetallisierung 2 μm sein sollte.

Nach der Definition von PVD-Al als die hauptleitende Schicht der Rückseitenmetallisierung wurde in Kapitel 4 der Kontaktbildungsprozess von aluminium-basierten PVD-Metallisierungen untersucht. Wenn reines Aluminium verwendet wurde, wurde die Bildung von Aluminium-Spikes beobachtet, die aufgrund der hohen Löslichkeit und dem hohen Diffusionsvermögen von Silizium in Aluminium bei 400 °C (Kontaktbildungstemperatur) entstehen. Lösungsansätze zur Vermeidung von Aluminium-Spikes wurden vorgestellt und diskutiert. Die Ansätze der Stand-der-Technik wie der Einsatz einer Titanschicht als Diffusionsbarriere oder einer Aluminium-Silizium-Legierung Al-Si (1 at% Si), als auch neue Ansätze wie die Verwendung eines Al-Si/Al Schichtstapels wurden untersucht. Die Wirksamkeit dieser Ansätze wurde mit Simulationen analysiert und durch REM-Untersuchungen (Raster-Elektronen-Mikroskopie) charakterisiert. Die Ergebnisse zeigten, dass Aluminium-Spiking durch die Verwendung einer hinreichend dicken Barriereschicht wie Titan überwunden werden kann. Für einen 5-minütigen Kontaktbildungstemperprozess bei 400 ° C ist eine Titanschichtdicke von mindestens 20 nm erforderlich, um die Spike-Bildung auf Cz-Silicium-Wafer zu unterdrücken. REM-Bilder der Proben mit einer Al-Si Metallisierung zeigten eine vollständige Abwesenheit von Aluminium-Spikes, stattdessen jedoch mit stark ausgeprägten Silizium-Präzipitaten. Silizium-Präzipitate sind *p*-dotiert und können einen ohmschen Kontakt zu n^+-Silizium beeinträchtigen. Die Verwendung eines Al-Si/Al Schichtstapels statt einer Al-Si-Metallisierung führte zu einer signifikanten Abnahme der Silizium-Präzipitate und einer Unterdrückung der Aluminium-Spikes. Die Simulationen sowie die experimentellen Ergebnisse zeigten, dass für die Metallisierung einer 2 μm Aluminiumschicht (5-minütiger Temperprozess bei 400 °C) eine 400 nm dicke Al-Si Schicht notwendig ist, um die Bildung von Aluminium-Spikes und Silizium-Präzipitate zu unterdrücken. Für andere Aluminiumschichtdicken oder andere thermische Belastungen, muss die Dicke der Al-Si-Schicht angepasst werden.

In Kapitel 5 wurde der spezifische Kontaktwiderstand zwischen den untersuchten aluminium-basierten Rückseitenmetallisierungssystemen (Al, Ti/Al Schichtstapel, Al-Si/Al Schichtstapel und Al-Si) und n^+-Siliziumpunktkontakten bestimmt. Zwei Dotierungsprofile und damit zwei Oberflächendotierungskonzentrationen wurden dabei untersucht. Um den spezifischen Kontaktwiderstand von Punktkontakten zu bestimmen, wurde eine neuartige Charakterisierungsmethode entwickelt, die Kontaktwiderstandswerte größer als 0,01 $m\Omega cm^2$ auflösen kann. Für niedrig-dotiertes n^+-Silizium mit einer Oberflächendotierungskonzentration von etwa $3{,}8\times10^{19}$ cm^{-3} und einem Schichtwiderstand von etwa 136 Ω/sq zeigte die Al-Si-Metallisierung einen hohen spezifischen Kontaktwiderstand (ca. 5 $m\Omega cm^2$), was zu signifikanten ohmschen Verlusten der Solarzelle führen kann. Durch den Einsatz eines Al-Si/Al Schichtstapels anstatt einer Al-Si-Metallisierung konnte der spezifische Kontaktwiderstand auf etwa 2 $m\Omega cm^2$ reduziert werden. Dies bedeutet ein Füllfaktorverlust um etwa 2 $\%_{abs}$. Der spezifische Kontaktwiderstand der Proben mit reiner Al-Metallisierung war etwa fünfmal niedriger als der mit Al-Si-Metallisierung (spezifischer Kontaktwiderstand um 0,4 $m\Omega cm^2$). Dies entspricht einem niedrigen Füllfaktorverlust von 0,5 $\%_{abs}$. Der Einsatz von Titan auf niedrig dotiertem n^+-Silizium hingegen führte zu einem sehr niedrigen spezifischen Kontaktwiderstand (um 0,15 $m\Omega cm^2$). Titan als Kontaktschicht scheint somit die beste Wahl für das Kontaktieren von niedrig-dotiertem n^+-Silizium zu sein. Die Auswertung der Proben mit der höheren Dotierung (Oberflächendotierkonzentration ~ $6{,}9\times10^{19}$ cm^{-3}, Schichtwiderstand ~ 75 Ω/Sq) führte zu dem Ergebnis, dass alle Metallisierungssysteme den für die Rückseite einer nPERT Solarzelle erforderlichen spezifischen Kontaktwiderstand (< 0,3 $m\Omega cm^2$) erreichten. Darüber hinaus zeigten die Ergebnisse aller Proben, dass es keinen signifikanten Unterschied zwischen der nicht getemperten und der getemperten Proben gab. Dies bedeutet, dass der Sputterprozess von Aluminium bei hoher Leistung zu einem ausreichenden dynamischen Kontaktbildungsprozess führt.

Die optischen Verluste der Rückseitenmetallisierung wurden in Kapitel 6 untersucht. Dabei wurde die Auswirkung verschiedener Passivierungs- und Metallisierungsschichten auf das Rückseitenreflektionsvermögen und damit auf

die Stromerzeugung in der Solarzelle untersucht. Verschiedene Rückseitenmetallisierungssysteme mit den Kontaktmetallen Al, Al-Si, Ti und Ag wurden in Kombination mit verschiedenen Rückseitenpassivierungsschichten untersucht. Die Ergebnisse dieser Untersuchungen zeigten, dass die Verwendung von Al-Si zu vernachlässigbaren geringfügigen optischen Verlust führte, insbesondere wenn eine optisch optimierte Rückseitenpassivierung (beispielsweise SiN_x/SiO_2 Schichtstapel mit 210 nm SiO_2 Schichtdicke) verwendet wurde. Die Verwendung von Ti als Kontaktschicht hingegen führte zu großen optischen Verlusten, selbst wenn eine optisch-optimierte Passivierung wie SiN_x/SiO_2 verwendet wurde. Der Grund dafür ist die sehr niedrige Reflektivität von Ti im nah-infraroten Spektralbereich. Wenn Ti als Kontaktmetall verwendet wurde, ist die Rückseitenreflexion mehr als 6 $\%_{abs}$ niedriger im Vergleich zu Al oder Al-Si. Dies bedeutet ein Stromverlust von mehr als 0,3 mA/cm². Um die niedrige Reflektivität von Ti mit Hilfe anspruchsvoller Mehrfachschicht-Passivierung (z. B. Bragg-Stapel) zu überwinden, wurden zusätzlich 3D-Ray-Tracing-Simulationen durchgeführt. Die Ergebnisse zeigten, dass ein aufwendiger fünfschichtiger Bragg-Stapel mit einer dicken ersten Schicht (~ 600 nm) notwendig ist, um die optischen Verluste auf ein vernachlässigbares Niveau zu reduzieren. Dies ist allerdings in einem industriellen Umfeld kaum umsetzbar und wurde daher nicht experimentell überprüft. Die Ergebnisse mit Ag als Kontaktmetall zeigten, dass mindestens 50 bis 60 nm Ag erforderlich ist, um von der sehr hohen Reflektivität von Ag zu profitieren. Der Einsatz von Ag führt jedoch noch immer zu zu hohen Kosten im Vergleich zu den anderen Metallisierungssystemen. Darüber hinaus zeigten die Ergebnisse, dass die Verwendung von dünnen Ag-Schicht als Kontaktmetall nur für eine Standard-70 nm SiN_x-Rückseitenpassivierung von Vorteil ist. Wenn eine optisch-optimierte Rückseitenpassivierung (z. B. SiN_x/SiO_2 Schichtstapel) verwendet wurde, war der Vorteil sehr gering ($\Delta R_b < 1\ \%_{abs}$).

In Kapitel 7 wurden die Auswirkungen der Plasmastrahlung in der Prozesskammer der Sputteranlage auf die Passivierungsqualität verschiedener Passivierschichten wie z. B. SiO_2, Al_2O_3/SiN_x und SiN_x untersucht. Dies wurde durch die Messung der effektiven Ladungsträgerlebensdauer mit MWPCD-Verfahren sowie durch die Bestimmung der Grenzflächeneigenschaften mit der

COCOS-Methode charakterisiert. Es wurde beobachtet, dass die effektive Lebensdauer der Proben mit SiO_2- und Al_2O_3-Passivierung nach der Al-Metallisierung stark degradierten. Die Proben mit SiN_x-Passivierung (wie für die Rückseite der in dieser Arbeit entwickelten nPERT Solarzellen) degradierten hingegen nur geringfügig. Die Ergebnisse der Gesamtladungsdichte und die Grenzflächendefektdichte korrelierten sehr gut mit den Ergebnissen der effektiven Ladungsträgerlebensdauer.

In Kapitel 8 wurden abschließend die Zellergebnisse von großflächigen nPERT Siliziumsolarzellen mit einer siebgedruckten Vorderseitenmetallisierung und einer PVD-Rückseitenmetallisierung vorgestellt. Der Fokus der Zellchargen war vor allem die PVD-Rückseitenmetallisierung. Es wurde gezeigt, dass eine reine Aluminium-Metallisierung nach einem Temperprozess Schädigung aufgrund von Aluminium-Spiking verursacht. Diese Schädigung kann entweder durch ein tieferes n^+-Dotierungsprofil oder durch die Verwendung von Metallbarrieren zwischen der Aluminiumschicht und dem Siliziumwafer überwunden werden. Es konnte festgestellt werden, dass der Strom der Solarzelle stark abnimmt, wenn Ti als Kontaktschicht verwendet wurde. Der Grund dafür ist die geringe IR-Reflektivität von Ti, was mit den Ergebnissen der vorherigen Kapitel übereinstimmt. Somit kam der Vorteil von Ti aufgrund des sehr niedrigen Kontaktwiderstands nicht zum Tragen. Die Solarzellen mit Al-Si/Al Rückseitenmetallisierung zeigten ähnliche Zellergebnisse wie die mit reiner Aluminiummetallisierung, jedoch mit einer etwas höheren Leerlaufspannung und einer deutlich höheren thermischen Stabilität. Des Weiteren konnten die Simulationsergebnisse der lateralen ohmschen Verluste sowie der Kontaktwiderstandsverluste mit den Zellergebnissen bestätigt werden. Eine Aluminiumschicht mit 2 µm Schichtdicke ist notwendig, um die lateralen ohmschen Verluste auf ein vernachlässigbares Niveau zu reduzieren. Ein spezifischer Kontaktwiderstand von ungefähr $1{,}5\times10^{-4}$ Ωcm^2 konnte aus den Zellergebnissen bestimmt werden, welche mit dem Ergebnis der Widerstandsproben ($0{,}9\times10^{-4}$ Ωcm^2) übereinstimmt. Schließlich konnte ein Wirkungsgrad von 20,88 % erreicht werden, der vom unabhängigen Fraunhofer ISE CalLab PV Cells bestätigt wurde. Soweit dem Autor bekannt, war dies der

bislang höchste Wirkungsgrad einer großflächigen nPERT Solarzelle mit mindestens einer Siebdruckseite.

Abschließend soll hier ein Ausblick gegeben werden: Um mehr über die Ursache der Strahlungsresistenz von SiN_x Passivierung zu erfahren, sollten im Anschluss an die vorliegende Arbeit mehr Untersuchungen an Plasma-induzierten Schäden der Passivierschicht durchgeführt werden. Ferner könnten die verschiedenen aluminium-basierten PVD-Metallisierungssysteme auf anderen Solarzellentypen getestet werden. Zusätzlich sollten sich zukünftige Untersuchungen mit der Verschaltung der Solarzellen mit aluminium-basierte PVD-Rückseitenmetallisierung und siebgedruckten Vorderseitenmetallisierung durchgeführt werden. Dabei könnten Verbindungstechniken wie Bonden oder anisotrope leitfähige Filme (ACF) für aluminium-basierte PVD-Metallisierung interessant sein, die keine zusätzlichen lötbaren Deckschichten erfordern wie z. B. NiV/Ag.

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