High-precision Analog Interfaces for Low-latency PC-in-the-loop Controller

Gunter Krapf, Folker Schwesinger, Thomas Fröhlich

Technische Universität Ilmenau, Institute for Process Measurement and Sensor Technology

ABSTRACT

Digital controllers offer enormous advantages regarding the flexibility, adaptability and implementation of complex controller structures. Here, especially PC-in-the-loop concepts are worth to mention, which provide almost infinite computing power, memory resources and prototyping capabilities. However, these systems reveal a specific weakness: Their interfaces to the analog world often have high latencies or insufficient metrological characteristics. That is why analog-to-digital converter (ADC) as well as digital-to-analog converter (DAC) modules were developed, which meet the requirements of high-speed and high-precision control systems.

Against this background, basic principles and problems are presented, which relate to the development of corresponding modules. In this connection, the design process and the resulting technical compromises are described. In Addition, first measurements concerning latencies, closed-loop frequencies and metrological characteristics are presented and discussed. Finally, the potential for further improvements is introduced.

Index Terms - PC-in-the-loop, Digital Control, ADC, DAC, EMFC balance

1.   INTRODUCTION

High-dynamic feedback control problems are typical fields of application for analog circuits. Especially in corresponding high-precision control systems, analog electronics are state of the art. A prime example for high-dynamic and high-precision controlled systems are electro-magnetic force compensated (EMFC) balances (see fig. 1).
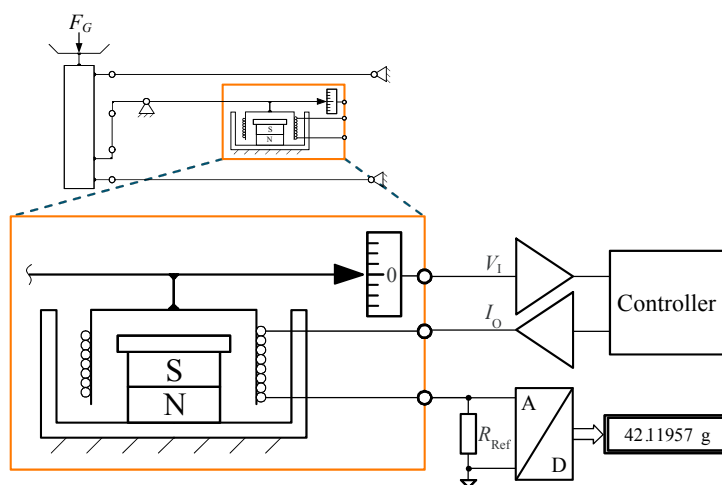

***Figure 1:*** *Typical principle of an analog controlled electromagnetic force compensated balance*

Here, a zero position indicator provides a position signal V_I. This amplified voltage signal acts as an input signal for a controller whose output signal is amplified by an output driver. Hereby, this driver provides a current I_O which flows through the electromagnet of the EMFC balance. This current flow causes a force action, which counteracts the weight force F_G of the weight load. The resulting positional deviation of the electromagnet is detected by the position indicator and is controlled to be zero by this closed-loop. The load's weight force F_G is directly represented by the current flow I_O, which can be quantized by an ADC using a reference resistor R_{Ref}.

Complex electromechanical systems, like the above described EMFC balance, often show multiple parasitic oscillations or rather characteristic frequencies in the range of several hundred Hertz. Thus, complex controller structures with closed-loop frequencies in the kilohertz range are needed for a reliable control. In addition, excellent metrological characteristics concerning short- and long-term stabilities, resolution or noise are required in these applications. Though the last points are comparatively easy to realize in analog electronics, it is all the harder to implement control strategies for systems of higher order in all-analog circuits. In contrast to this, digital controllers offer enormous advantages regarding the realizability and moreover the flexibility as well as adaptability of complex controller structures.

A typical digital controller is shown in figure 2. It consists of at least one ADC, a digital processing unit and at least one DAC. The processing unit is often a microcontroller (µC) or a field programmable gate array (FPGA). The related ADCs and DACs are usually connected by serial peripheral interfaces (SPI) or are an integral part of the processing unit's circuit. The latter arrangement is known as digital signal processor (DSP). A personal computer (PC), connected to this system, has usually monitoring, logging or display functions.
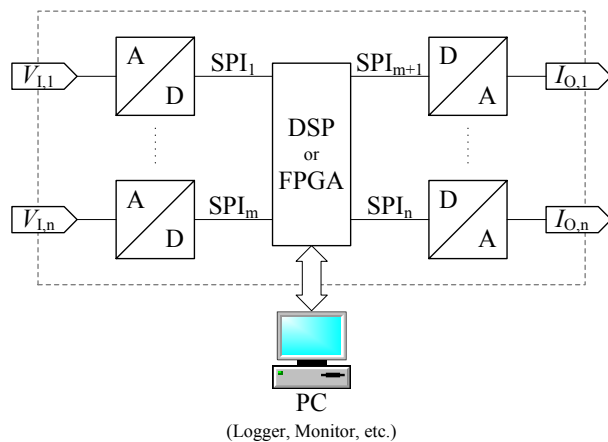
Figure 2: *Block diagram of a common DSP- or FPGA-based digital controller*
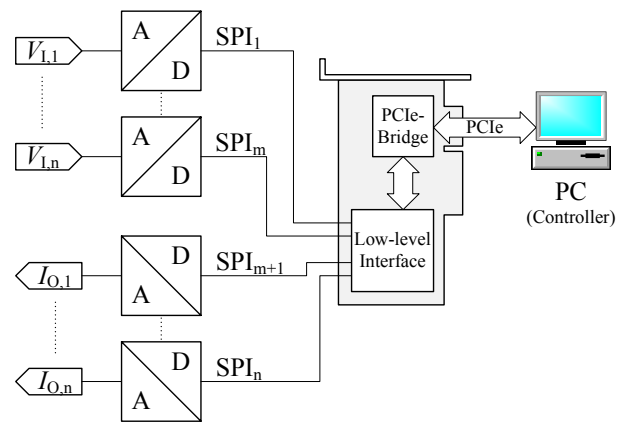
Figure 3: *Block diagram of a universal PC-in-the-loop control system*

Another approach to implement a digital controller is the "PC-in-the-loop" concept (fig. 3). Here, the digital processing unit consists of a standard PC, which is equipped with a real-time operating system and a low-latency, low-level interface to external ADC and DAC modules (see e.g. [1]). In contrast to solutions on the basis of µCs, DSPs or FPGAs, these PC-based systems provide the advantage of almost infinite computing power, random access memory, storage space and prototyping as well as monitoring capabilities.

To utilize these advantages for development, implementation and application of controllers for high-precision applications like EMFC balances, analog interfaces are required, which meet the outstanding dynamic and especially advanced metrological requirements. However, corresponding analog interfaces are not commercially available at present.

Certainly, one could utilize precision voltmeters like the Agilent 3458A or precision current sources like the HP 3245A for this task. But putting these setups into practice, closed-loop frequencies of only a few hundred Hertz were achieved. As an alternative, it is also thinkable to use commercial PC-in-the-loop systems like National Instruments' PXI platform. However, analysis disclosed that the metrological and the dynamic performance of PXI devices are constrained in PC-in-the-loop applications [2]. In consequence, a proprietary development with consideration of highest possible sample rates, minimal latencies, maximal resolutions and the best possible metrological performance was necessary which will be presented and discussed in the following.


2. DESIGN OF ANALOG INTERFACE MODULES

To realize precision ADC and DAC modules on condition of a preferably high degree of integration, the usage of integrated converter circuits and voltage references is inevitable. A corresponding market research revealed a limited number of suitable high-speed, high-resolution and particularly high-precision circuits. A selection of potentially suitable converters can be taken from table 1.
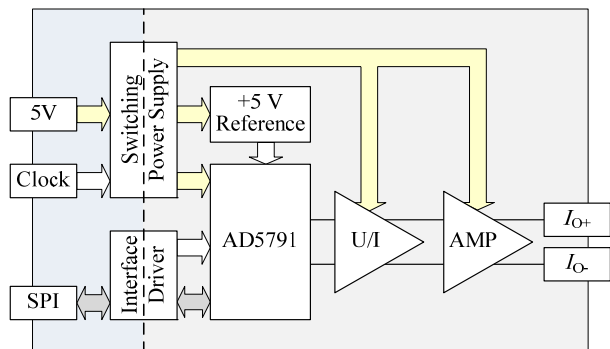
Table 1: *Selection of high-speed, high-resolution, high-precision converters*

ADC			DAC		
Name	Nominal resolution	Conversion time (at sample rate)	Name	Nominal resolution	Measured step response
ADS1281	31 Bit	21 µs (64 kS/s)	AD5791	20 Bit	1 µs
AD7767-1	24 Bit	63 µs (64 kS/s)	DAC9881	18 Bit	10 µs
CS5560	24 Bit	20 µs (50 kS/s)	ADS1280	24 Bit	>>10 µs

Using evaluation boards of these circuits, test measurements were taken which identified the ADS1281 and AD5791 as most appropriate for our application. In addition, several voltage references and amplifier circuits were metrological analyzed. In consequence, the LT1027 was chosen as voltage reference. Furthermore, INA114 instrumentation amplifiers were selected to serve as signal conditioners. LT1010 buffers will be used as power amplifiers. Moreover, every module is fully galvanically isolated using opto-couplers and external clocked switching power supplies. The block diagrams of these designed ADC and DAC modules can be seen in figures 4 and 5. Here, both modules are interfaced by a low-level SPI.
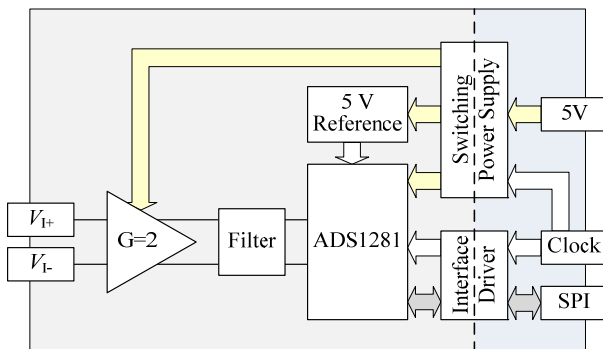

Figure 4: *Block diagram of the realized ADC module* **Figure 5:** *Block diagram of the realized DAC module*

On this basis, printed circuit boards (PCB) for the ADC and DAC modules were designed, put into operation and metrological investigated. Selected results of these experiments are presented in the following section.

3. RESULTS

As mentioned above, one of the most important design parameters is the closed-loop frequency of the controller to develop. While conversion times and thus minimal step response times of clocked ADCs can be considered as determined (see [3]), in practice the dynamic performance of the ADC module's analog input stage depends on various factors. That is why the step response of the realized input stage (fig. 6) was measured using an Agilent DSO-X 2004A oscilloscope with integrated function generator. The resulting step response of this input amplifier plus anti-alias filter can be seen in figure 7. Here, 99 percent of the final step value is reached after approximately $t_{99\%}$=25 µs.
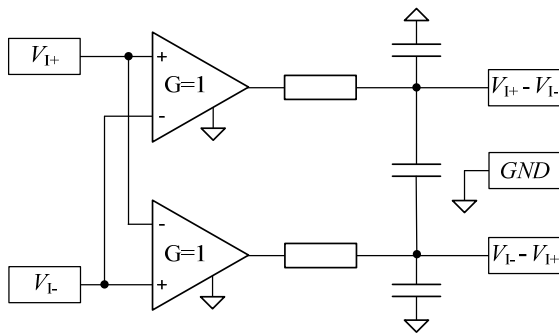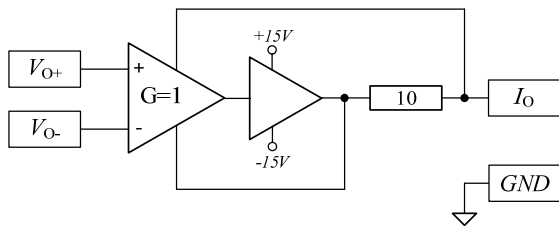

Figure 6: *Simplified block diagram of the input stage without protection circuits*
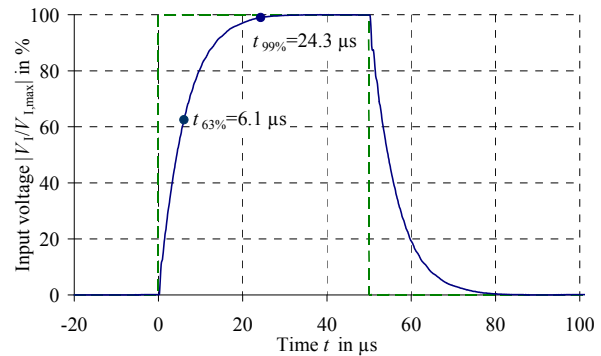
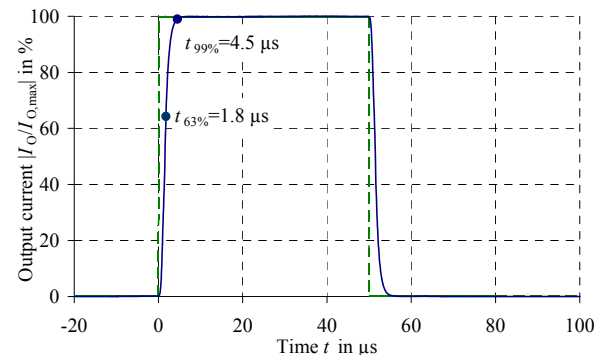
Figure 7: *Normalized step response of the analog input stage to a $|V_I|=|V_{I,max}|=1.25$ V step*

In the same way, the step response of the output stage (fig. 8) was measured while it was driving a 100 Ω resistive load. In this case, 99 percent of the final step value were reached after $t_{99\%}$=5 µs as shown in figure 9.


**Figure 8:** *Simplified block diagram of the output stage*

Figure 9: *Normalized step response of the analog output driving a resistive load ($|I_{O,max}|=100$ mA)*

In addition, the step response of the AD5791 DAC was measured using the same equipment. Here, the datasheet's value of approximately 1 µs response delay could be confirmed (cp. tab. 1, [4]). The same point can be made for the ADS1281 ADC where a response delay of approx. 21 µs could be observed (cp. tab. 1, [3]).

To sum up these results, one can conclude that using these modules closed loop frequencies of at least 10 Kilohertz can be achieved. The condition for this is a 24 bit SPI data transfer with clock frequencies of 2 MHz and maximum PC processing times of 5 µs (see [1]), as clarified by figure 10.
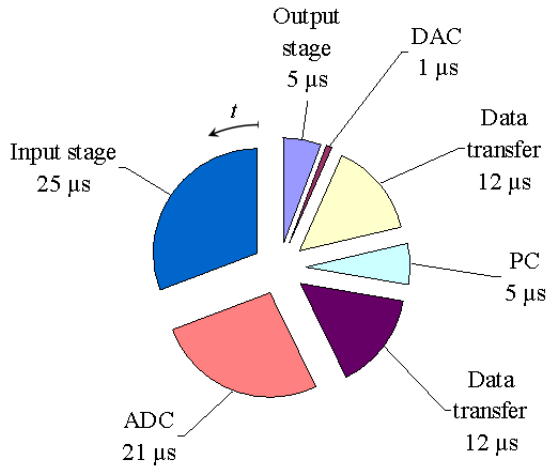
Figure 10: *Estimated delays of the single PC-in-the-loop components (see also [1])*
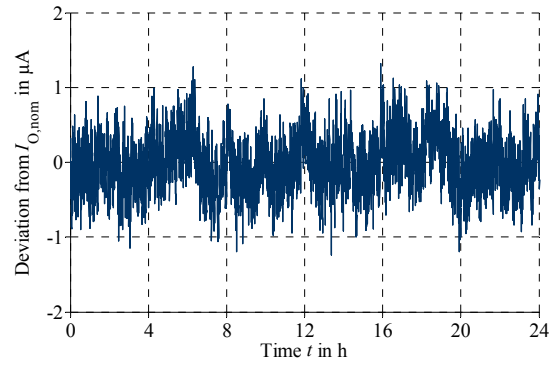
Figure 11: *DAC module driving a nominal current of $I_{O,nom}$=45 mA through an EMFC balance simulator of approx. 75 mH/150 Ω*

To characterize the direct current (DC) performance of the DAC modules, a fixed inductance with parameters typical for EMFC balances was energized. The flowing current was measured using an Agilent 3458A (10 V range, integration time 1 s) and a reference resistor of 100 Ω. Here, a standard deviation of $S(I_O)$=0.4 µA (8 ppm) was observed as can be seen in figure 11. Even though achieving a negligible long-term drift, the noise of this output stage represents a starting-point for further improvements. Here, especially the signal's low frequency components can be assigned to temperature effects as recorded in separate measurements.

The measurement of the input module's DC performance is exemplarily shown in figure 12. Here, the module's input is shorted and sampled with a rate of 64 thousand samples per second (64 kS/s). To allow a comparison, the measured values were filtered (mean of 32 values) and decimated to an effective sample rate of 2 kS/s. Here, a standard deviation of $S(V_I)$=6 µV was achieved in this case. Apart from low frequency temperature drifts, the measured signal can be regarded as Gaussian distributed. When performing this measurement for several days, a zero point drift of ±3 µV per 24 hours was observed.
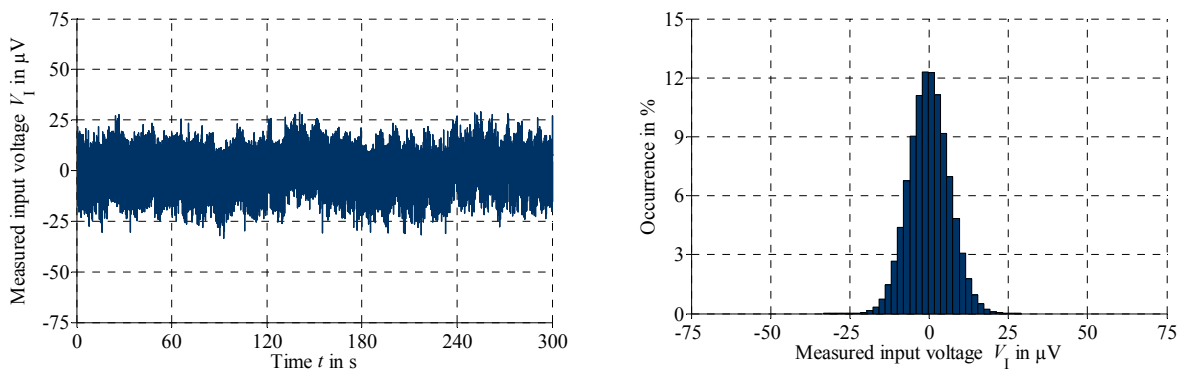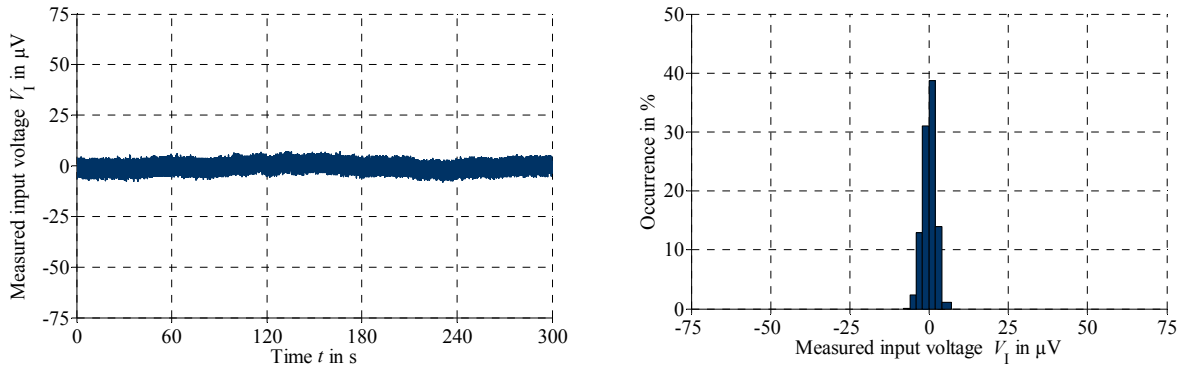

Figure 12: *Input module sampling its shorted input (V_I=0 V) with 64 kS/s, shown data is filtered and decimated to 2 kS/s*

If this measurement are repeated using a commercially available analog I/O module for PC-in-the-loop applications, like the PXI-6289 from National Instruments, we obtain the results in figure 13. Here, a standard deviation of $S(V_I)$=12 µV can be observed at a sample rate of 2 kS/s in the 1 V range. If this measurement is taken continuously, zero point drifts in the range of ±10 µV per day occur. They are mainly caused by temperature drifts.
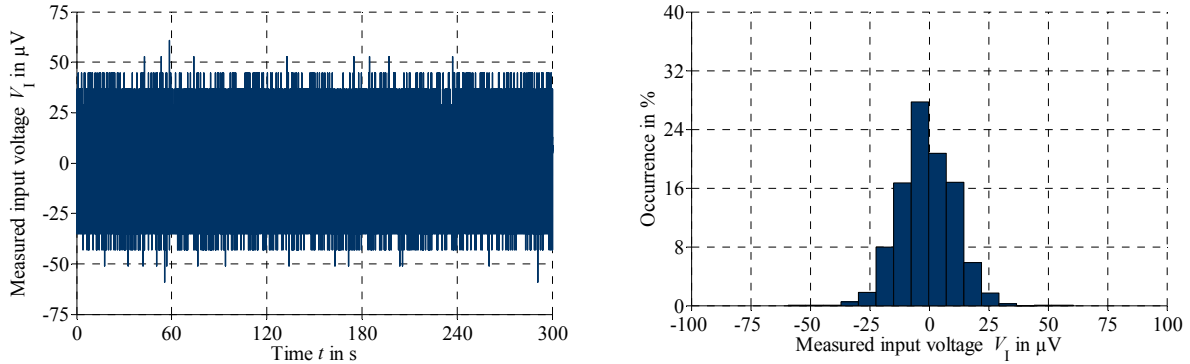
Figure 13: *PXI-6289 measuring a shorted input (V_I=0 V) with 2 kS/s in the 1 V range*

The goal of our development is to achieve a noise and DC performance similar to the renowned Agilent 3458A multimeter. When this multimeter is measuring its shorted input with a sample rate of 2 kS/s in the 1 V range, a standard deviation of below $S(V_I)$=2 µV (figure 14) and long term drifts in the lower ppm range can be observed. Approaches to achieve these outstanding parameters are discussed in the following.

Figure 14: *Agilent 3458A sampling its shorted input (V_I=0 V) with 2 kS/s in the 1 V range*

4. DISCUSSION

At the time of publishing this paper, the described modules were still under intensive development. Due to this, given latencies, drifts and noises should be regarded as preliminary. But, these results allow the conclusion that the proposed concept is suitable to achieve the aim of a low-latency, high-precision, high dynamic PC-in-the-loop controller.

As has been demonstrated, we were able to achieve or rather exceed the parameters of a comparable system. However, the largest challenge will be the reduction of described noise effects in further developments, which obscure or interfere with higher frequency components of desired signals. Although, noise is a well-known and well describable phenomenon in electronics (see [5]), it is hard to overcome its impact on a high-dynamic precision system. The main reason for this is that most design techniques, which optimize the DC performance, frequently result in higher noise (see [6]). Noise reduction by filtering is not an option either, as this degrades the systems' dynamic performance. In addition, the circuit's noise is often highly influenced by surrounding components or its wiring. All these points require both an optimization of the circuit and the PCB partly by iterative prototyping methods.

But there are other approaches to consider: For example, the use of thermostatically controlled modules or on-board temperature measurements would allow a compensation of thermal drifts. In addition, humidity effects could be reduced by encapsulating or sealing

sensitive components (see [7]). Besides, dynamic performance could be improved by higher output driver voltages or an active filtering of input signals. However, these points are part of further investigations.

5. ACKNOWLEDGMENT

REFERENCES

[1] Schwesinger, F.; Krapf, G.; Fröhlich, T.: PC-based Low Latency Controller for Dynamic Mechatronic Systems. Conference Proceedings: 58th Ilmenau Scientific Colloquium, September 2014, Technische Universität Ilmenau, 2014

[2] Weis, H.; et al.: Investigation on Digital Control Concepts for Dynamic Applications of Electromagnetic Force Compensated Balances. Conference Proceedings: NCSLI International Workshop and Symposium, July 2013, Nashville (Tennessee, USA), NCLS International, 2013

[3] Texas Instruments Inc.: ADS1281 – High-Resolution Analog-to-Digital Converter (Rev. D). Dallas (USA), June 2010

[4] Analog Devices Inc.: AD5791 – 1ppm 20-Bit Voltage Output DAC Datasheet (Rev. D), Norwood (USA), July 2013

[5] Motchenbacher, C. D.; Connelly, J. A.: Low Noise Electronic System Design. New York: John Wiley and Sons, 1993

[6] Rich, A.: Noise Calculations in Op Amp Circuits – Design Note 15. Linear Technology Corporation, 1988

[7] Hilbrunner, F.: Ein Beitrag zur Feuchtekompensation von Präzisionsmeßgeräten (Contribution to the humidity compensation of precision measurement devices). Doctoral thesis, TU Ilmenau, 2005 (in German)

CONTACTS

Dipl.-Ing. Gunter Krapf   gunter.krapf@tu-ilmenau.de
M.Sc. Folker Schwesinger   folker.schwesinger@tu-ilmenau.de
Univ.-Prof. Dr.-Ing. habil. Thomas Fröhlich   thomas.froehlich@tu-ilmenau.de