THIN-FILM CAPABLE CERAMICS FOR HUMIDITY AND TEMPERATURE SENSING APPLICATIONS

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ABSTRACT

In this paper we present methods to achieve thin-film capable substrates made of Low Temperature Co-fired Ceramic (LTCC) without grinding or polishing processes. Two planarization methods are explained and discussed. The first is based on a thin sol-gel layer which is dip coated. The second planarization method utilizes a screen printed glass paste to smoothen the surface of the substrate. The emerging advantage of the modified LTCC surfaces is that thin-films like gold can be deposited and structured with small feature sizes and good electric properties.
We will demonstrate the benefit of thin-film capable ceramics utilizing an innovative temperature and humidity sensor. The sensor comprises two interdigital capacitors and two resistors which form an AC bridge circuit. Depended on the external temperature and humidity the bridge is detuned and the amplitude and phase of the output voltage is changed.

Index Terms – Thin film, planarization, LTCC, temperature, humidity, sensor

1. INTRODUCTION

Low temperature co-fired ceramics (LTCC) are advantageous for sensor applications in harsh environments with high temperatures because of their stable mechanical and chemical material properties. Additionally, the screen printed conductive pastes are solderable which allows an integration of sensor structures and signal processing circuits on a shared substrate [1].
Nevertheless, disadvantages of the LTCC technology compared to silicon micromachining are the low resolution of structure dimensions and the high specific resistance of the screen printing materials. Recent research is focusing on resinate pastes or sputtered and evaporated thin-films to achieve smaller dimensions and better reproducibility [2]. However, the specific resistance of the non-reinforced thin-film is high as a consequence of the rough surface of the LTCC[1]. Additionally, the structural resolution is limited by the roughness and waviness of the substrate, because the thin films are structured by UV-lithography. Limiting issues for the UV-lithography resolution are:

- diffuse reflection at the rough surface which leads to an exposure of the masked areas,
- bad resist adhesion for structures smaller than 10 µm,
- diffraction errors which are caused by a proximity distance between mask and substrate.

[1] A higher layer thickness and therefore a reduced sheet resistance can be obtained by electroplating. However, thick galvanic films can only be applied by electroplating if the entire surface area is electrically contactable. This is not the case for every substrate or device.

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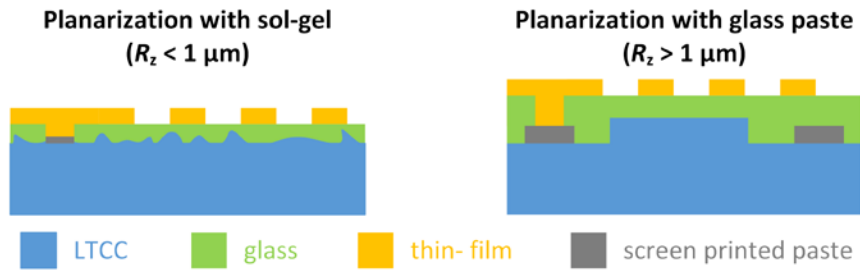

Figure 1: Principle of a planarization utilizing sol-gel or glass paste

In this paper, we present methods to achieve thin-film capable LTCC surfaces without grinding or polishing processes. The main idea is to use a glass layer on the top of LTCC substrates which locally smoothens the surface. On this planar area thin-films like gold can be deposited and structured with small feature sizes and good electric properties. Two planarization technologies are shown in Figure 1: Sol-gel [3] and screen printing technology [1]. A dip coated sol-gel layer is suitable for initial smooth surfaces without structured features. For three-dimensional substrates the glass paste DP9615 is suitable because screen printing can be done on structured surfaces [1]. The electric contact to the LTCC layer below is realized by a through hole connection which can be etched into the glass layer or directly structured by screen printing. Therewith, a small electric connection with a low line resistance can be achieved.
The thin-film capable LTCC substrate enables small structures which are typically used on silicon based micromechanical sensors. For instance, humidity and temperature sensors utilize interdigital capacitors and/ or meandered resistors to increase the functional integration and decrease the sensor dimensions [4-5]. These structures with dimensions down to 5 µm can be applied directly on LTCC substrates with our planarization technologies. The emerging advantages using LTCC instead of silicon are the availability of solderable thick film materials, the possibility to integrate functions inside the substrate (e.g. heaters), the high isotropic young's modulus and the high temperature stability without surface oxidation. In addition, the lower thermal conductivity of LTCC is beneficial for applications where thermal isolation of circuit structures is necessary.

2. PLANARIZATION TECHNOLOGIES FOR LTCC SUBSTRATES

The material DuPont 951 [1] is utilized to demonstrate the effect of our planarization technologies. Therefore, different sintered substrates (t_{LTCC} = 500 µm, □80 mm) were fabricated and characterized to get an orientation for the reachable surface properties without surface planarization. Table 1 and Figure 2 show the measurement results which were received utilizing a tactile profilometer (Dektak 150, [6]).
The measurements demonstrate that a variation of the sintering process improve the surface roughness and waviness of the LTCC substrate. Nevertheless, the roughness is still too high for fine structured thin film conductors or capacitors, because the resist mask does not adhere well and the thin film resistivity is too high (cf. section 3).

Table 1: Characterization of different sintered ceramic substrates and comparison with a standard silicon wafer

Material	DP951	DP951	DP951	DP951	Silicon
Sinter technology	free	constraint	pressure	free and polished	-
Roughness R_z (l = 5 mm)	2.3 µm	1.3 µm	1.6 µm	0.4 µm	0.01 µm
Waviness (Peak-Peak, l = 5 cm)	8.9 µm	8.8 µm	8.0 µm	4.2 µm	< 2 µm

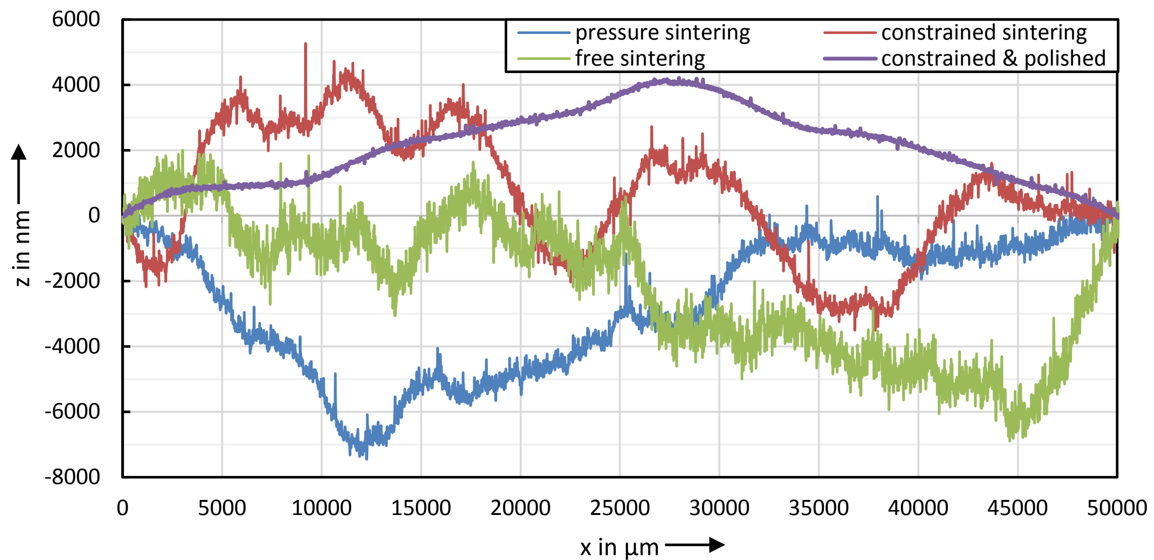

Figure 2: Surface topography of different sintered ceramic substrates DP951

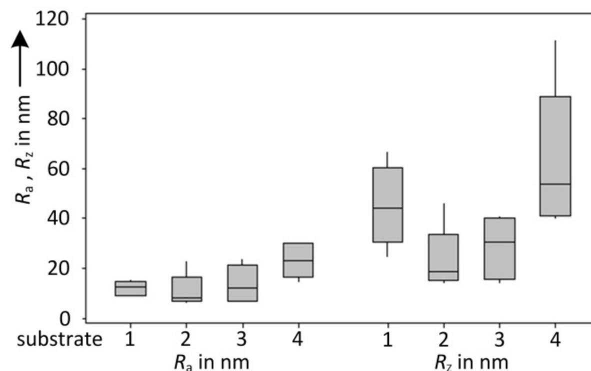

Figure 3: Roughness of LTCC substrates (DP951, constrained sintered) which were smoothen with sol-gel

An extra polishing step leads to a smother surface but requires much more processing time. Additionally, a polishing step is only possible with an empty substrate because it would eliminate printed components (e. g. conductors, pads, resistors). A structured surface or a surface with sintered conductors is not suitable for polishing. Thus, current research focuses on possibilities to smooth the surface of a LTCC-substrate in a cost efficient and flexible way.
The first planarization technology utilizes a sol-gel mixture which consists of silica particles and water in the ratio 1:1, the average diameter of the primary silica particles is 35 nm (Köstrosol 3550, *Chemiewerk Bad Köstritz GmbH*). The sol-gel layer is dip coated with a thickness of one micrometer on a constrained sintered DP951 substrate. Free sintered substrates are not suitable for a planarization with the thin sol-gel layer, because of the initial high roughness R_z of the free sintered surfaces (cf. Table 1). The drying of the substrates with sol-gel layer was done in a climate cabinet over seven days under variation of humidity and temperature. The special drying regime is necessary to get dense and crack free surfaces. A characterization of the surface with a tactile profilometer shows that the roughness R_z of constrained sintered LTCC substrates can be decreased to 100 nm utilizing sol-gel technology. Nevertheless, the sol-gel layer is deposited over the full surface of the substrate). Thus, an etching step with a reactive ion etching plant is necessary to open the sol-gel layer and contact the LTCC surface (cf. chapter 3). Disadvantages of the sol-gel planarization are the limited application on initial smooth surfaces (constrained and pressure sintered surfaces), the long drying regime and the additional etching process which are cost-intense and time-consuming. However, the sol-gel layer leads to very smooth surfaces with a roughness below those of polished substrates.

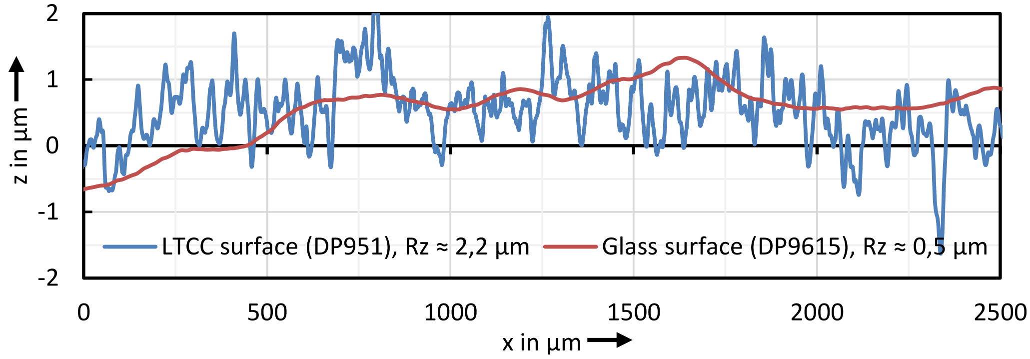

Figure 4: Topography of a free sintered LTCC surface with and without a glass paste

A second planarization technology was investigated to get a cheap alternative to the sol-gel technology which can also be applied on free sintered surfaces. The planarization technology is based on a LTCC glass paste DuPont 9615 [7] which is deposited during a standard screen printing process (glass thickness approximately 12 µm). After the deposition, the glass paste is sintered in a co-fire process with the LTCC tapes and conductive pastes. The results of the planarization are shown in Figure 4. Roughness and waviness of the surface are decreased utilizing the glass paste. Nevertheless, the sol-gel technology enables much lower roughness values. However, the structured deposition with screen printing, the integration in standard LTCC processes and thus the cheap fabrication are the advantages of the glass paste planarization compared to the sol-gel planarization.

3. STRUCTURED THIN FILMS ON PLANARIZED LTCC SUBSTRATES

A 100 nm thin film of gold with a 10 nm chrome adhesion promoter was evaporated on the LTCC substrates to investigate the behavior of the glass surfaces. A comparison between the thin films directly evaporated on the LTCC surface and the thin-film on the glass surface shows that the specific resistance is decreased by both planarization methods (Table 2). Nevertheless, the specific resistance on constrained sintered surfaces is much higher, because of surface defects caused by the fabrication (Figure 5). The specific resistance on free sintered surfaces prepared with glass paste is near to a gold thin-film of 100 nm on a silicon wafer [8-9]:

$$\rho_{\mathrm{Au}}(d = 100\mathrm{nm}) \approx 3.2 \cdot 10^{-8}\Omega\mathrm{m} \qquad (1)$$

Table 2: Specific resistance of a gold thin-film (AuTi, t_{Au} = 100 nm, t_{Ti} = 50 nm) on different surfaces

	Substrate 1 (DP951, const. sintering)		**Substrate 2 (DP951, free sintering)**	
Surface	LTCC	Sol-Gel	LTCC	DP9615
ϱ_{Au} in Ω·m	$2.7 \cdot 10^{-7}$	$2.5 \cdot 10^{-7}$	$5.3 \cdot 10^{-8}$	$4.1 \cdot 10^{-8}$

A wet etching process with potassium iodide was chosen to structure the gold layer [10] and a hydrofluoric-water solution (c_{HF} = 1%) to structure the titanium layer [10]. The etch mask was the spray coated photoresist AZ®9260 (t = 17 µm) which resolution was improved dramatically by the planarization methods. The structure resolution was decreased from 10 µm to 5 µm utilizing the glass paste and to 4 µm utilizing the sol-gel. Therewith, lines and spaces of gold down to 5 µm can be generated on LTCC substrates utilizing one of the established planarization methods (cf. Figure 6).
An important design issue is the electric connection between the glass layer and the LTCC surface where conductors or vias are located. The glass paste is advantageous concerning the electric connection to subjacent layers because it is applied utilizing screen printing. Thus, the glass paste is structured with vias which realizes through hole connections (cf. Figure 7).

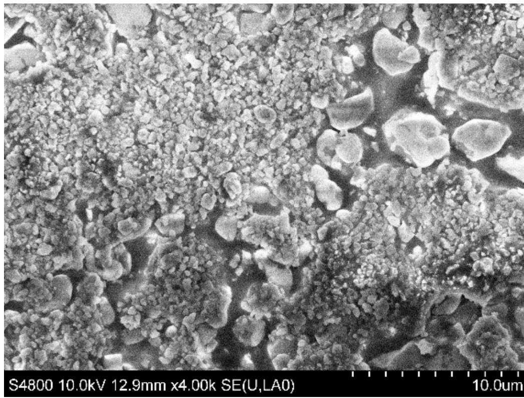

Figure 5: Cracks and blow-outs on a surface of a constrained sintered substrate

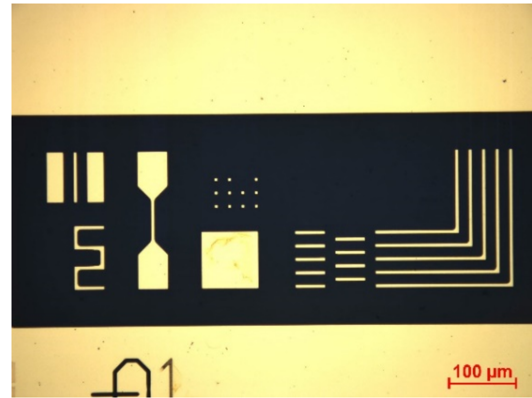

Figure 6: Etched gold lines and spaces (pitch=10 µm) on a planar LTCC surface

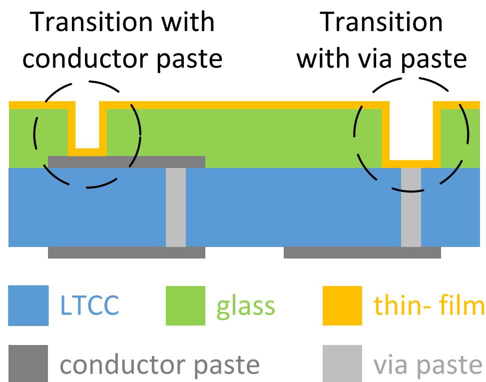

Figure 7: Principle of transition between the glass surface and the LTCC surface

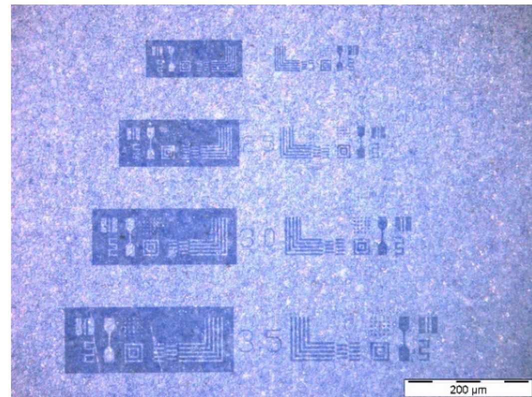

Figure 8: Dry etched sol-gel layer on LTCC with a structure resolution down to 5 µm

Table 3 shows the transition resistance for different openings in the glass layer. Additionally, the contact material and geometry on the LTCC were varied. The investigations demonstrate that the transition resistance to the gold paste is increased with a decreasing opening in the glass layer. This behavior is explained by the decreasing area around the hole. Nevertheless, the transition resistance is very low (R < 45 mΩ) for glass hole diameters bigger than 100 microns. In contrast to the gold paste, the transition resistance to the gold via decreases with a decreasing hole diameter in the glass paste. This is caused by the good flow behavior of the glass paste on the via material which leads to a continuous and homogeneous deposited transition. Nevertheless, the resistance is bigger than the one on the gold paste.

The transition resistance through the sol-gel layer was not investigated yet. However, a dry etching process was established utilizing a Reactive-Ion-Etching plant which can realize through hole connection with diameters down to 5 µm (cf. Figure 8). Therewith, compact designs are possible which will be investigated during future research activities.

Table 3: Investigation of the transition resistance through a glass paste (DuPont 9615, d = 12 µm) utilizing a gold layer (AuTi, t_{Au} = 200 nm, t_{Ti} = 50 nm) and a via (DuPont TC701 [1], d = 200 µm) or a gold paste (DuPont 5742 [1], t = 15 µm) respectively.

Opening in glass layer	Transition resistance with gold (AuTi) and gold paste	Transition resistance with gold (AuTi) and gold via
200 µm	30 mΩ	130 mΩ
150 µm	40 mΩ	100 mΩ
100 µm	45 mΩ	30 mΩ
50 µm	110 mΩ	No contact

Through hole connection

500 µm

4. EXAMPLARY APPLICATION: A TEMPERATURE AND HUMIDITY SENSOR

In this chapter, the benefit of thin-film capable ceramics is demonstrated utilizing a temperature and humidity sensor. The sensor comprises two interdigital capacitors and two meandered resistors which are integrated into an AC bridge circuit (cf. Figure 9).
The substrate of the sensor is made of a standard LTCC tape material (DuPont 951 [1]) which is planed on the surface with a glass paste (DuPont 9615 [7]). Through hole connections and vias lead to four pads on the backside of the substrate. Gold and chrome were deposited with a thickness of 200 nm on the top of the substrate and structured with a resist mask and potassium iodide [10]. The fabricated sensor is shown in Figure 10 and 11.
The function of the sensor is based on the change of the capacitance and the resistance ($C \approx 10$ pF, $R \approx 2$ kΩ). If the temperature changes the bridge is detuned because of the different thermal coefficients of resistance of gold and chrome [8,11-12].

$$\alpha_{\mathrm{R\,Cr}}(d = 200\mathrm{nm}) = -1 \cdot 10^{-4}\frac{1}{K} < \alpha_{\mathrm{R\,Au}}(d = 200\mathrm{nm}) = 17 \cdot 10^{-4}\frac{1}{K} \qquad (2)$$

If the humidity of the surrounding air increases, the dielectric constant of the sensitive material polyvinyl alcohol (PVA) increases because of the water absorption [13-15]. Thus, the capacitance is changed which is measured by the amplitude and phase shift of the output voltage.

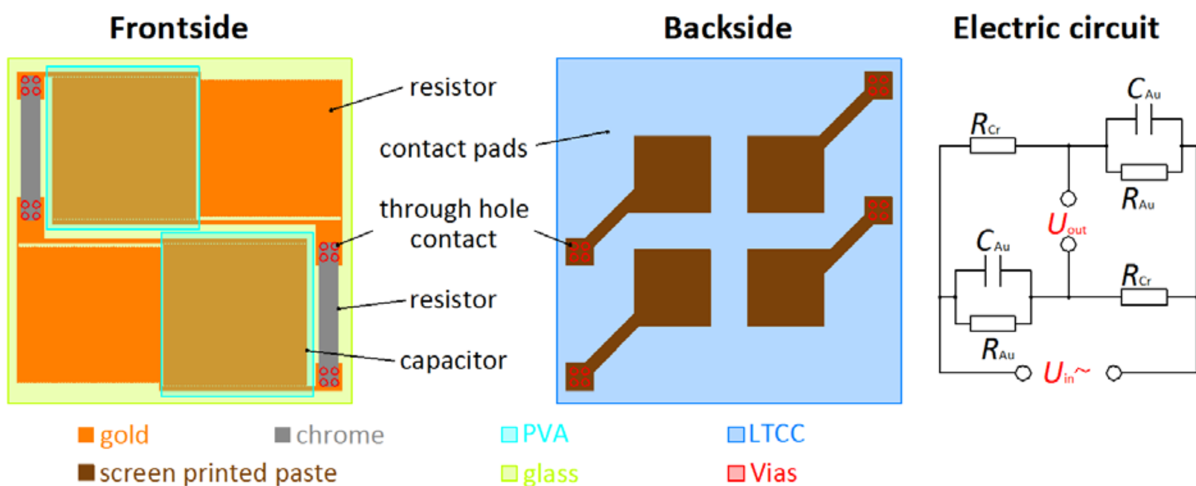

Figure 9: Principle design of the temperature and humidity sensor

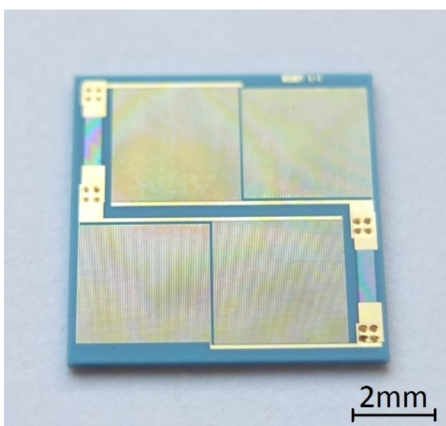

Figure 10: Fabricated temperature and humidity sensor in LTCC

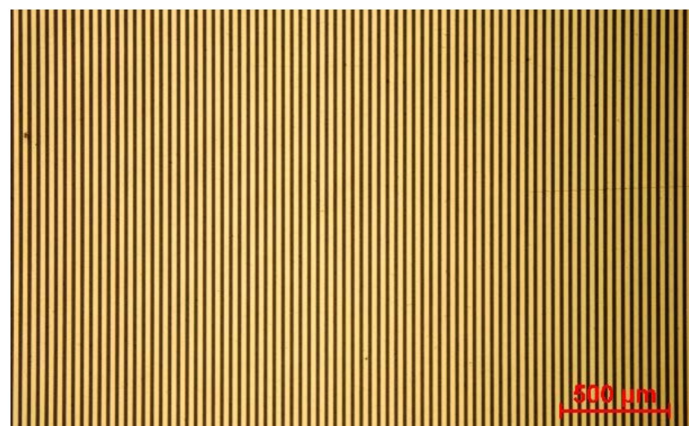

Figure 11: Defect-free interdigital structure of the temperature and humidity sensor (20 µm lines and spaces, A ≈ 20 mm²)

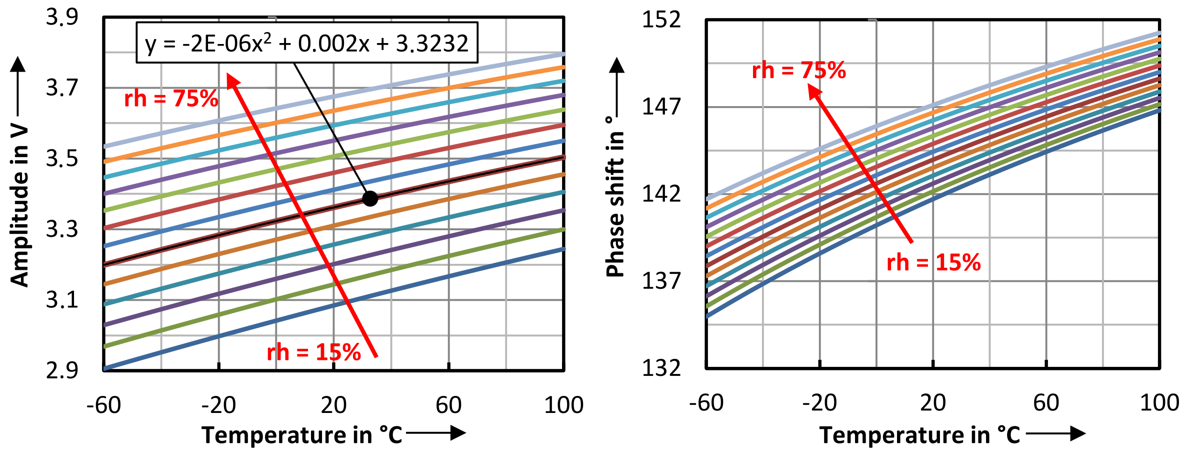

Figure 12: Amplitude and phase shift of the sensor output voltage depended on the temperature

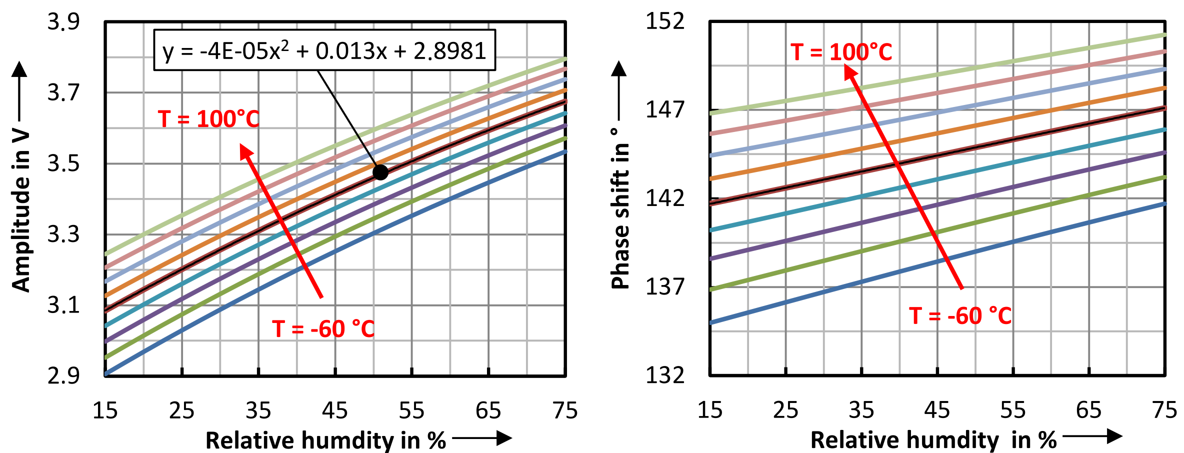

Figure 13: Amplitude and phase shift of the sensor output voltage depended on the humidity

The sensor is operated with a 5 V sine voltage at 12 MHz. In Figure 12 and 13 the calculated sensor characteristic is shown. The calculation demonstrates that every pair of humidity and temperature values has exactly one pair of phase shift and output voltage. Thus, a very simple sensor system can be set up with an oscillator and an evaluation unit for phase and amplitude of the output voltage, only. The possible integration of electronic components on the sensor substrate is an advantage of the LTCC technology. Hence, a compact and monolithic sensor system can be set up in the future.

5. SUMMARY AND OUTLOOK

We presented cost-efficient and flexible technologies to plane surfaces of LTCC-substrates. Therewith, the roughness R_z and the specific resistance of a thin gold layer were decreased from 2 µm to approximately 100 nm and from $5.3 \cdot 10^{-8}$ Ωm to $4.1 \cdot 10^{-8}$ Ωm respectively. Thus, new sensor applications for the LTCC technology are possible which are based on small interdigital or meandered structures.

An innovative humidity and temperature sensor was introduced to demonstrate the achievement of the planarization technologies. The sensor utilizes a glass paste to get a plane and thin-film capable surface. Therewith, functional structures down to 20 µm were generated over a large area up to 100 mm².

Future works will concentrate on the characterization of the sensor in a climate cabinet, the integration of the sensor in fabrication plants (dry etch plants, sputtering plants etc.) and the functionalization of the sol-gel and glass layers with electric or magnetic conductive particles.

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