Field programmable gate array based digital lock-in amplifier for highest resolution heterodyne interferometer

Sebastian Strube[1]*, Gabor Molnar[1], Hans-Ulrich Danzebrink[1]

[1]Physikalisch-Technische Bundesanstalt, Bundesallee 100, D-38116 Braunschweig, Germany

ABSTRACT

In this work the electronics for a highest resolution heterodyne interferometer is presented. It comprises an analog front-end, a high speed dual channel analog-to-digital converter and a field programmable gate array for high speed, low latency signal processing. The gate array contains a system on chip (formulated in a hardware description language), consisting of the main processing block (lock-in algorithm) combined with a 32 Bit CPU and additional periphery controllers. Output data is streamed over a high speed serial bus, USB2 or a fiber link. For different uses the firmware and the main processing block may be substituted, while the rest of the system (hardware & software) may remain the same. The underlying electronic-platform and evaluation concept is very versatile and can be used for many different interferometric (homodyne and heterodyne alike) concepts or completely different signal acquisition tasks.

Keywords: digital Lock-In Amplifier, FPGA, ADC, SoC

1. INTRODUCTION

Interferometric measurement systems are a preferred choice whenever highest resolution displacement or angle measurements are required.

The achievements in integrated circuit design of the last decades allowed for a reduction in structure size and ever cheaper and faster digital circuits to be built. This also tremendously changed the situation in measurement and control electronics design. After a migration from purely analog solutions to application specific integrated circuits and digital signal processor based systems, the rise of field programmable integrated circuits allows for even higher processing rates and lower latency.

The requirement for low latency also often prohibits the use of a general purpose CPU (like a desktop PC). This has latencies of interrupt handlers/overhead of the operating system and caching strategies in the case of a context change, despite the availability of high speed processing units for digital signal applications (like SSE2 on x86, or NEON on ARM). In addition, the complex power saving modes in current CPUs which are only partially documented and cannot be switched of completely pose a limit for a system reaction with low latency [1].

DSPs on the other hand are optimized for low latency stream processing. They come with hardware support for floating point operations as specified in IEEE 754 [2]. Furthermore the architecture is optimized for common DSP algorithm requirements as special addressing modes used e.g. for fast Fourier transform (FFT) calculation [3]. These features combined with fast interfaces made them the prime choice for signal processing in the past.

Programmable logic, consisting of small logic cells whose final specific connection can be selected by the user, emerged from glue logic for interfacing ICs to sensor data conditioning/pre-processing technology and beyond.

The combination of a signal processing unit into the programmable logic, was made possible due to ever increasing gate counts, either as hardwired blocks or formulated in a hardware description language (HDL). This saves the additional complexity in circuit design of combining an FPGA with a DSP and makes it possible to tailor a system specifically targeted to the problem.

Programmable hardware provides a degree of flexibility in connecting to external periphery and in parallelized execution rivaled only by application specific integrated circuits (ASIC).

Whenever an update option to adapt the system to new tasks is necessary or the number of units is too low to justify the initial costs of an ASIC design, FPGA based signal processing is the preferred choice for demanding applications.

To overcome the limitations mentioned and to fulfill the desired specifications the presented electronics system utilizes a fast dual channel analog-to-digital converter combined with a high-gate count FPGA, which contains an embedded system formulated in an HDL to implement a highest resolution heterodyne interferometer.
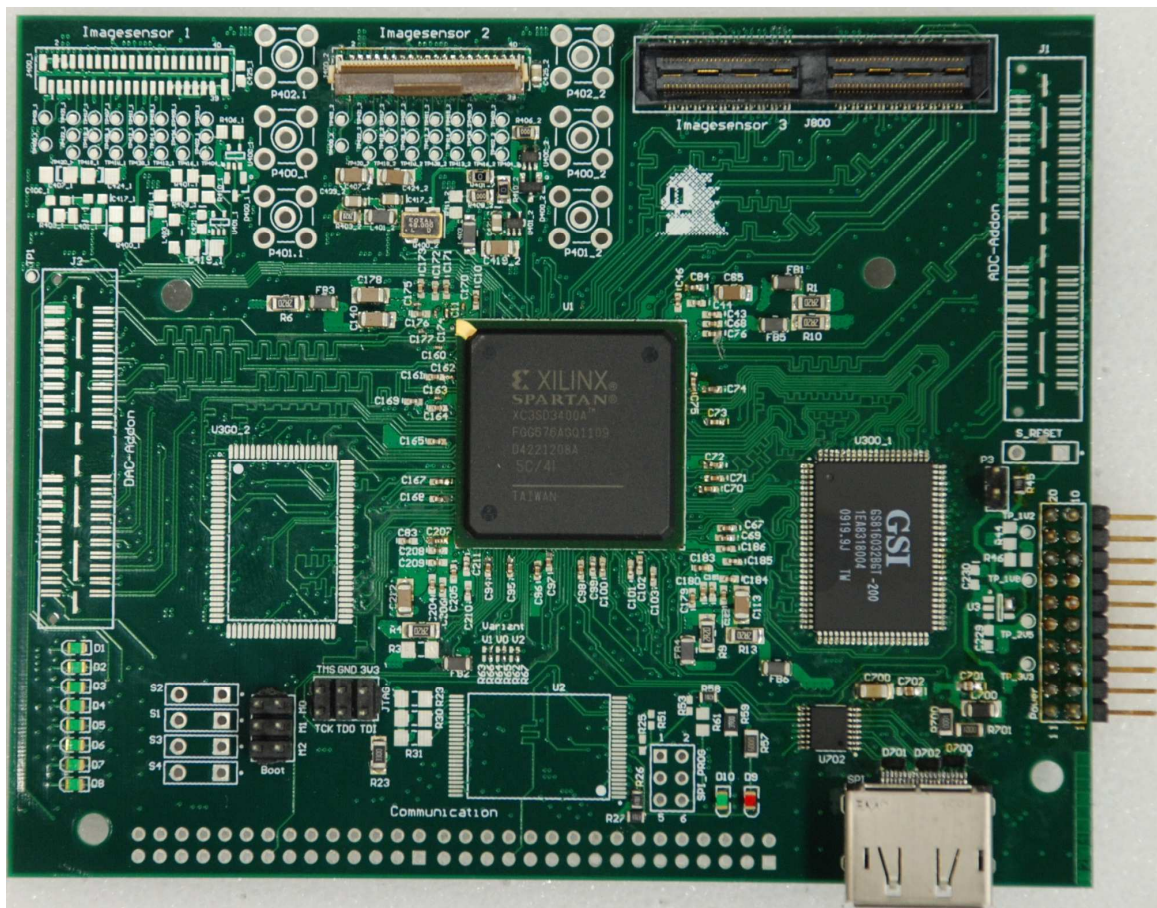
2. FPGA MAINBOARD

Figure A: FPGA mainboard (in partially assembled state)

The ten layer main FPGA board (Figure A) is based on a Xilinx Spartan 3ADSP3400 FPGA in a 676 pin BGA package with 1mm pitch. The FPGA configuration is read from an EEPROM (XCF16P) at startup. The system contains two independently addressable 512k x 32 Bit SRAM blocks (GS816032) with 32 Bit data bus width each, clocked at 150 MHz. Two interfaces for EV76C560 camera sensors (used in a different interferometric setup [4]), three high density extension connectors (Samtec QTH060-01-L-D-DP-A high density 50 Ohm connectors) for add-on boards, a differential serial high speed bus and a connector for a glass

fibre or USB interface card are available. The FPGA configuration memory and EEPROM content can be programmed over JTAG. The system was hand assembled and soldered in a reflow oven.

3.   ANALOG FRONT END & PHOTODIODE AMPLIFIER

Figure B: dual channel ADC board

In every digital signal processing system there is necessarily a stage, which converts a real world analog signal into the digital, time- and value discretized domain, where the signal may be processed further. In low noise measurement systems the input stage requires special attention. A differential transmission of the input signal is beneficial, because it reduces the coupling of common mode noise. However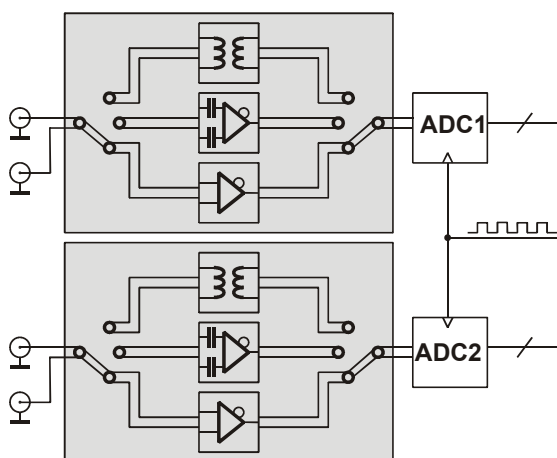, because not all first stage signal conversion units (like photodiode receivers) supply a differential output signal, the input stage of the discussed system can be configured into single ended mode.

The presented system offers two different input paths, either AC or DC coupled, to be used, selectable by relay. Depending on the measurement task (for instance in homodyne interferometry) it may be necessary to supply a DC coupled input-voltage. However, this passes the higher 1/f noise of the operational amplifiers into the input path.

If it is possible to guarantee a minimum carrier frequency, as in heterodyne interferometry, an AC setup can be used. The amplification and isolation from the input can either be done through

Figure C: Input channel selection

an operational amplifier or (in the AC case) through a signal transformer. The signal transformer, if properly applied, has the advantage of not adding any noise to the input signal, while stepping it up or down appropriately. However, stray magnetic fields may couple into the ferrite core and degrade the input signal unexpectedly. Thus, depending on the setup, a shielding with high permeability material (mu metal) may be necessary. The current setup offers the use of a transformer input path instead of the operational amplifier path by jumper selection.

In low noise applications the input impedance of the front end needs to be low (50 Ohm is a common choice) to reduce Johnson noise in the input resistor. This requires the driver in the previous stage (driving the front end) to be strong enough to not introduce nonlinearities due to saturation effects. For out photodiode-amplifier we used an LMH6714 as output driver, which (with an additional serial termination of 50 Ohm) can drive up to +/- 2.5V into a 50 Ohm load. The IV converter Op-amp (OP1) and the output driver (OP2) are spatially separated to minimize thermal drift. The basic circuit is shown in Figure D. Depending on the application either a bipolar (low gain) LMH6624 or a FET opamp (high gain) OPA657 is used as IV converter.

Input offset and amplitude might need to be adjusted to fit the ADC's input range. The ADC used in this setup has a selectable input range of either 1 or 2 Volt.
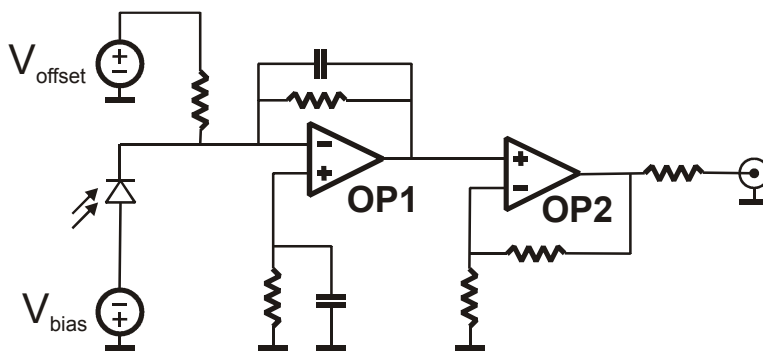

Figure D: photodiode IV converter setup

In our setup the offset correction is done in the photodiode amplifier through addition of an offset voltage. This eases further analog signal processing, because the ADC input stage does not need to have an additional offset correction scheme.

The incoming signal, routed as a 50 Ohm microstrip, is buffered and optionally converted from single ended to differential using a fully differential operational amplifier (LTC6409). The standard gain is unity, but can be optimized for different applications by changing the feedback resistors (0.1% tolerance). The feedback capacitor needs to be placed as close as possible to the amplifier, otherwise parasitic oscillations may occur.

The buffered differential signal passes through an optional first degree low pass filter. While this may seem problematic in regard to aliasing at first, it should be noted, that depending on the setup only small noise amplitudes may be present in the spectrum above the cutoff frequency.
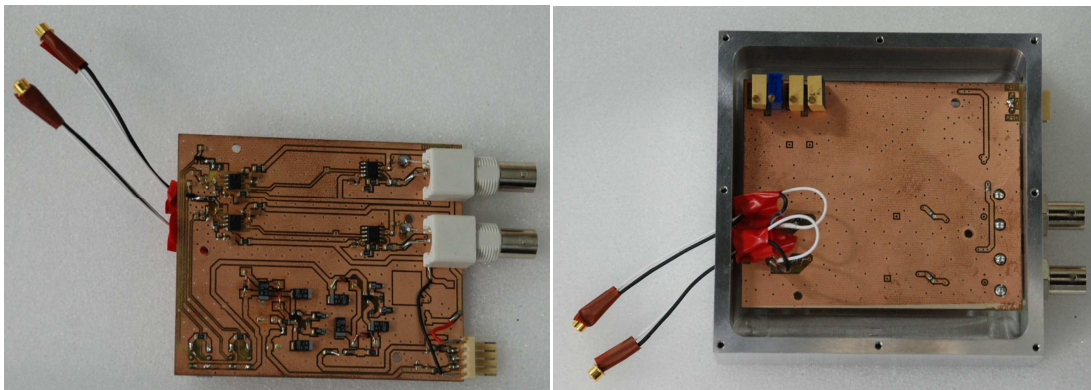
Figure E: photodiode IV converter assembly in massive case to minimize thermal drift

The signal afterwards passes an isolation resistor which is necessary to limit the effect of the switching transient of the ADC input on the buffer stages output. If omitted, the transient might cause the input stage to ring, which disturbs the input signal. This resistor together with the input capacity of the ADC forms an additional low pass filter.

The preprocessed analog signal is fed into the input of the 16Bit 100/125Msps ADC (LTC2184/ LTC2185). Because the simultaneous sampling of both signals (reference and measurement channel) is mandatory for the given task, a dual channel ADC is employed.

The presented system uses the internal reference (which is specified to have a gain error of +/-1.5%FS and a full scale drift of +/-30ppm/°C [5]) of the ADC, because the use in a heterodyne interferometer requires an equal gain on both channels, while the absolute gain is a less important factor. For different system requirements an external reference can be connected through an SMA connector.

Figure F: DDR LVDS transmission to FPGA

The encoder clock jitter directly affects the signal-to-noise ratio due to sample time uncertainty. In the presented system a precision voltage controlled crystal oscillator (Crystek CVD-950) is used, whose signal is applied to the ADC in single-ended form,. Optionally an external single-ended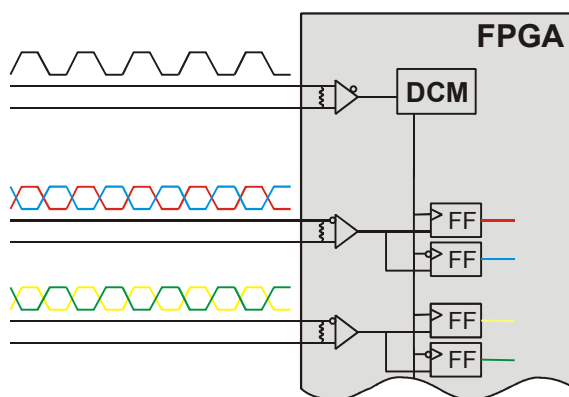 or differential encoder clock can be supplied. The ADC is controlled over its serial peripheral interface (SPI) port to take full advantage of its available features. The SPI lines are buffered (NC7SV125). The converter is configured to transmit the two channels output data in double data rate (DDR) mode as low voltage differential signals (LVDS) to minimize noise. The output stage is additionally buffered by differential buffers (FIN1108 & FIN1101) to decouple the ADC from the FPGA's inputs. These are prone to contain switching noise from internal processes in the FPGA which could in return disturb the ADC's conversion process. All differential lines are compensated for length differences to maximize the window of valid data. The differential lines are terminated inside the FPGA (using the DIFFTERM feature).

The ADC outputs the clock change simultaneously to the data change. Because the FPGA has differing timing requirements the input data is phase-shifted compared to the clock in the

FPGA input stages through the use of a digital clock manager (DCM) function block to comply with the requested setup and hold times.

4. DIGITAL COMPUTATION ALGORITHM

While on general purpose computers there is support of mathematical coprocessors and libraries presenting an abstract layer to the programmer, which considerably eases the implementation of algorithms, this is not the case in FPGAs.

The FPGA itself only contains rudimentary function blocks, like clock management, hardware multipliers, multiply-accumulate units, block RAM and provisions for fast adders. All more complex functions (division, square root, trigonometric functions, transforms) need to be implemented by the user in a hardware description language (HDL). While common functionality is also available as a preprogrammed intellectual property block by the FPGA manufacturer or third parties (for free or through a license fee), the use is often limited, because only the interface is exposed (no option to adapt the HDL code) and migration to different FPGA architectures is not supported. Because of this an own implementation is often necessary.

Figure G shows the lock-in algorithm block employed in the presented system, which processes the simultaneously obtained data from the two ADC channels. It consists of four hardware multiply/accumulate units (MACs) which are fed by waveforms (sine/cosine) from internal block RAMs. The frequency of the internal reference wave (equivalent to the beat frequency of the heterodyne interferometer) is fixed in this setup. The differential sine/cosine pair is created and the arctangent of it is calculated (employing the CORDIC algorithm) to get the phase information.
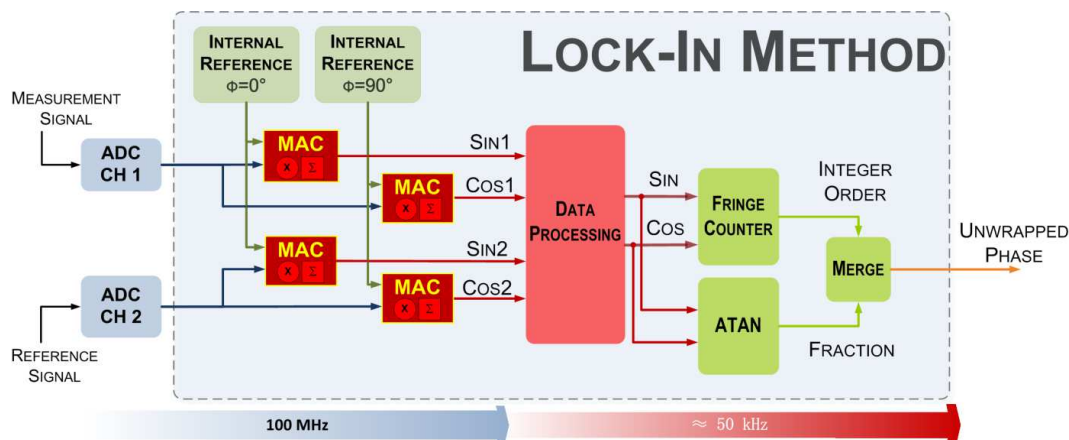

Figure G: Lock-In Amplifer function block

5. SYSTEMS ON CHIP

While FPGA systems in the past tended to mainly provide sensor signal conditioning and preprocessing of high rate input data, which then was passed to a DSP for post-processing, the density of modern FPGAs allows to contain a whole system on chip, consisting of the calculation blocks and a microprocessor with periphery for control and data transport. Figure H shows the embedded system used in the presented setup.

The core of the system is a 32 Bit MIPS CPU running at 25 MHz [6]. It is accompanied by peripheral controllers for USB2 or fiber link, a fast serial interface controller, controllers for the external SRAM and an UART for debugging. The lock-in algorithm processing block is represented as an additional peripheral, which can be controlled by the CPU.
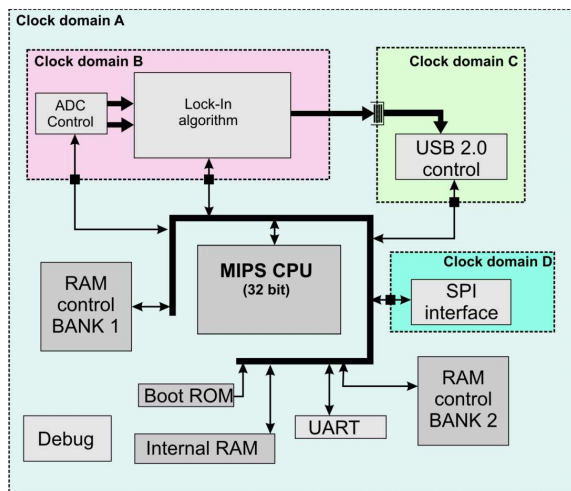
The system uses multiple clock domains and can store the input data in SRAM at full speed (up to 125 MHz) for evaluation. The SRAMs and the control registers of the peripherals are memory mapped into the address range of the CPU, which runs a control program written in standard C to ease control and debugging. The high clock rate of the SRAM allows for zero delay read/write-access from the CPU to the external memory.

Figure H: embedded system as used in the presented setup

While the CPU currently does not have hardware support for floating point operations, such an addition was presented elsewhere [7]. Besides housekeeping applications the CPU can be used for non-time-critical tasks like the evaluation of correction parameters (used for a Heydemann correction or the compensation of environmental changes). The current software libraries for the CPU can calculate single precision floating point operations (word size 32 Bit). Furthermore, calculation of trigonometric functions is supported through the use of Taylor series expansion [6]. Output data is transferred to the host computer without the need of CPU intervention.
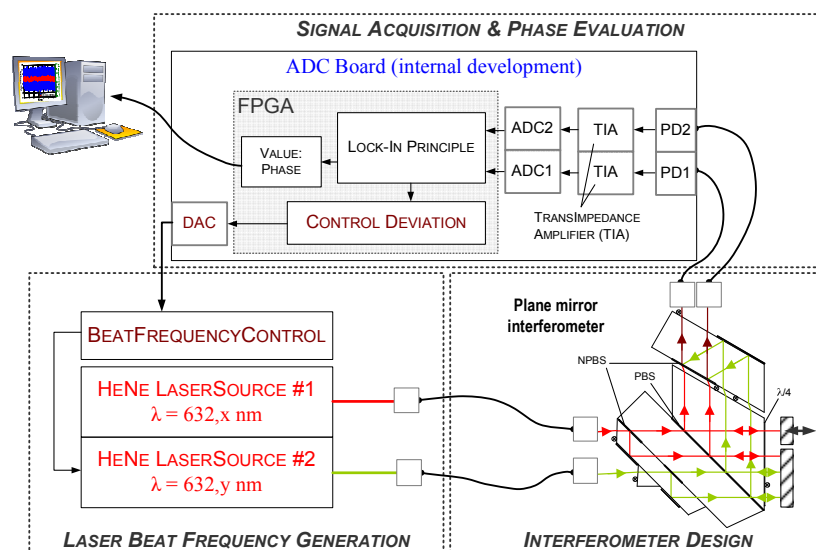
6. IMPLEMENTED SYSTEM AND USAGE EXAMPLES

Figure I: proposed interferometric system setup

Figure I: shows the mentioned heterodyne interferometer setup the presented system was designed for. The original version of the system [8] used a commercially available FPGA card [9] and photodiode amplifiers [10].

This was substituted by the presented system. Figure K shows the complete FPGA processing system consisting of the analog front-end stage, the ADC and the FPGA board.
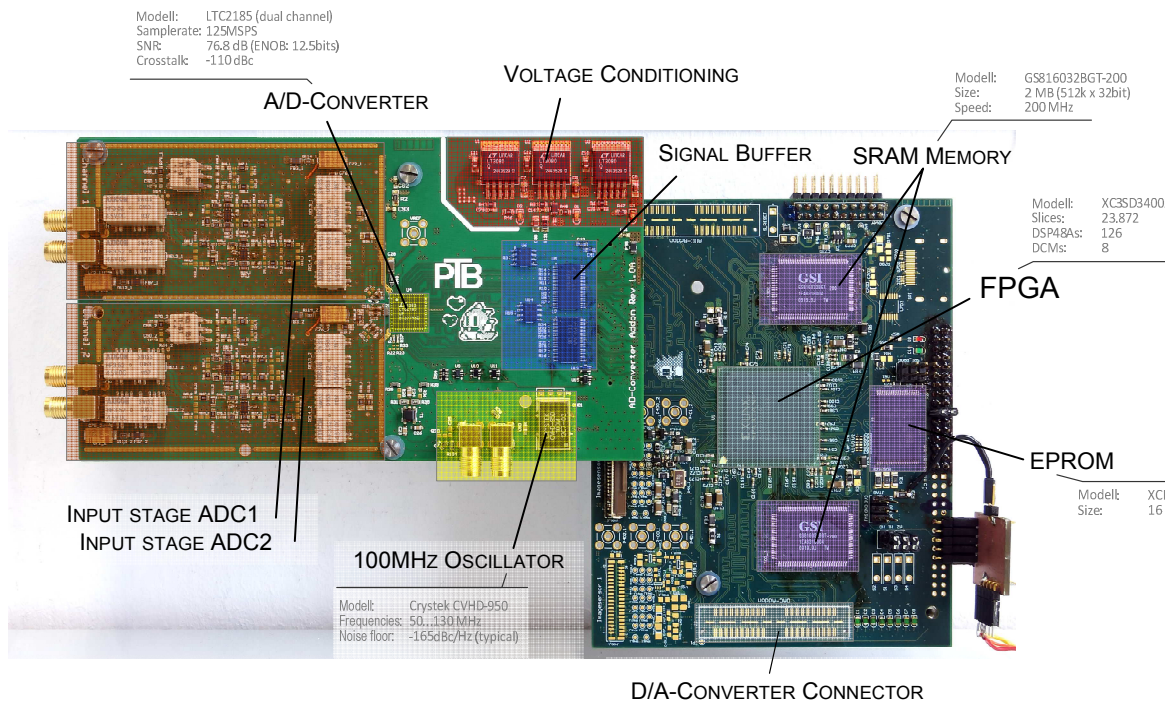

Figure K: signal & acquisition electronics

The system was characterized according to the IEEE-1057-1994 Standard for ADC dynamic performance characterization [11]. A low noise function generator (SRS DS360) with an SNR of 100dBc was used to create a 200 kHz low noise test carrier. This signal was digitized by the presented system at 100 mega-samples per second and the raw data was stored in the external SRAMs.

Afterwards the values were transmitted to the host PC over USB to characterize the system with the aforementioned protocol. A standard deviation of 10.97 digits at a modulation amplitude of 64682 values peak to peak was determined, which equals an ADC resolution of 12.52 Bit.
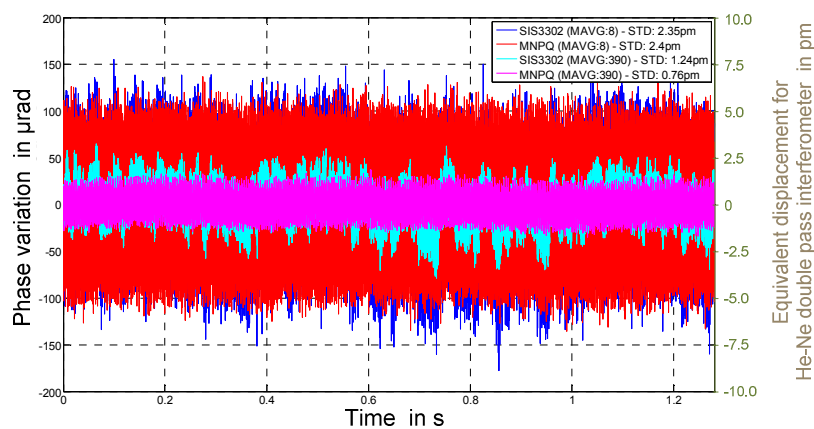

Figure M: comparison measurement between the original setup based on an SIS3302 FPGA card and the newly designed system

The available output pseudo randomization and noise shaping features of the ADC were tested but did not influence the achievable resolution in the given setup. The complete results are presented in Figure L.
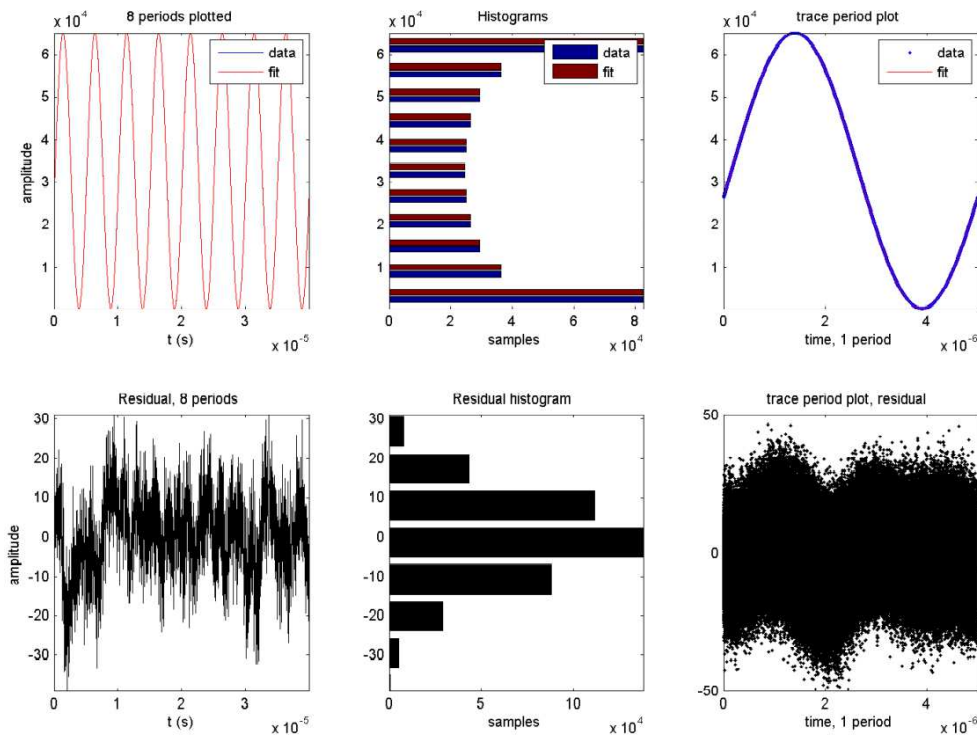

Figure L: analog input stage characterisation results according to IEEE-1057-1994

The systems demodulation capabilities for phase extraction were compared to the already implemented system based on an FPGA board, Model SIS3302 [9].

Both systems used an identical demodulation scheme. Results with a fixed beat frequency of 4 MHz are presented in Figure M. The systems show an equivalent performance at a data rate of 48 kHz. When the values are averaged to generate an output rate of 1 kHz, the presented system shows a significantly lower (see Figure M for detail) standard deviation compared to the previous setup.

ACKNOWLEDGEMENTS

REFERENCES

[1] Carsten Emde, How to cope with the negative impact of a processor's energy-saving features on real-time capabilities?, Proceedings of the 13th Real Time Linux Workshop, 2011

[2] IEEE 754-2008: Standard for Floating-Point Arithmetic, IEEE Standards Association, 2008, doi:10.1109/IEEESTD.2008.4610935

[3] Rulph Chassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, ISBN 0471690074, Wiley-Interscience, 2005

[4] Sebastian Stube, Gabor Molnar, Hans-Ulrich Danzebrink, Compact field programmable gate array (FPGA)-based multi-axial interferometer for simultaneous tilt and distance measurement in the sub-nanometre range, 2011, doi:10.1088/0957-0233/22/9/094026

[5] Datasheet LTC2185/LTC2184/LTC2183, http://cds.linear.com/docs/en/datasheet/218543f.pdf

[6] Steve Rhoads, Plasma CPU, http://opencores.org/project,plasma

[7] Taciano A. Rodolfo, Ney L. V. Calazans, Fernando G. Moraes, "Floating Point Hardware for Embedded Processors in FPGAs: Design Space Exploration for Performance and Area," reconfig, pp.24-29, 2009 International Conference on Reconfigurable Computing and FPGAs, 2009

[8] C Weichert *et al* 2012 *Meas. Sci. Technol.* **23** 094005, A heterodyne interferometer with periodic nonlinearities smaller than ±10 pm

[9] Struck SIS3302 8 Channel 100MS/S 16-BIT ADC, http://www.struck.de/sis3302.htm

[10] Femto HCA-10M-100K, HCA photodiode amplifier series, http://www.femto.de/en/products/current-amplifiers/fixed-gain-up-to-400-mhz-hca.html

[11] IEEE-1057-1994, IEEE Standard for Digitizing Waveform Recorders

CONTACTS

Sebastian Strube   Sebastian.Strube@ptb.de
Gabor Molnar   Gabor.Molnar@ptb.de
Hans-Ulrich Danzebrink   Hans-Ulrich.Danzebrink@ptb.de