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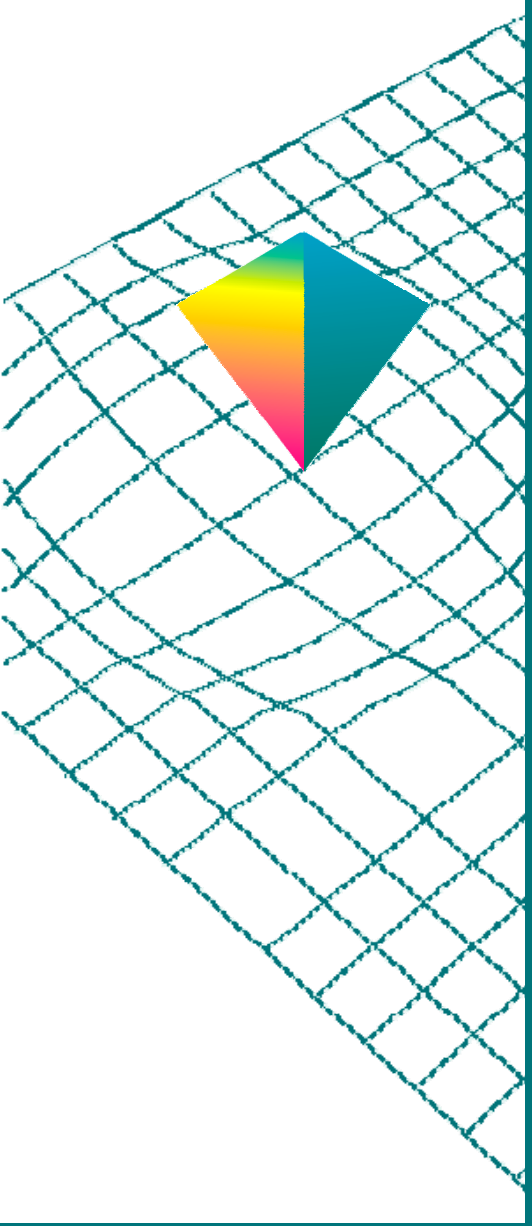

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50. Internationales Wissenschaftliches Kolloquium
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Modeling and simulation of CMOS image sensor with VHDL

ABSTRACT

Optoelectronic systems, used for measuring of light spot's coordinates, are widely used in the industry. During the design of such system became the modeling of VHDL model for signals from CMOS image sensor were necessary. With this model various algorithms for image processing can be tested. The virtual image sensor is being used successfully like a substitute for real CMOS image sensor.

The software model consists of a management bock and a memory block – in which information about the frames is stored. Management block reads data from the memory and generates impulses for synchronization simultaneously with the output data. The virtual sensor can output a piece of the frame; which is an analog to "windowing" function in the real CMOS image sensors.

VHDL model can be implemented in FPGA development kit. This allows it to be used as a physical source of CMOS image sensor signals. The size of the frame is limited only by the capacity of the used FPGA.

The software model is written in Quartus IV by Altera.

Using the virtual image sensor allows the repeated generation of each frame. This is impossible with real CMOS image sensor.

CMOS IMAGE SENSORS DESCRIPTION

Silicon is light-sensitive material and this property is used in CMOS image sensor. In the crystal lots of photodiodes are realized, arranged in a rectangular matrix. When a photon hits the photodiode (the pixel) drives out an electron. The quantity of these electrons is proportional to the quantity of the absorbed photons.

The color CMOS image sensors have pixels for each of the three basic colors: blue, green and red. There is a color filter in front of each pixel, corresponding to the "color" of the pixel. The pixels of every color have an even distribution on the crystal surface. Monochrome CMOS image sensors do not have color filters. In the CMOS image sensors there is an analog to digital converter. Output data are eight or ten bits binary numbers. The output digital value is proportional to the color intensity of the corresponding pixel. Simultaneously with the image data, the sensor generates signals for synchronization. The internal structure of a real CMOS image sensor (OV7620) is shown in Figure [1].

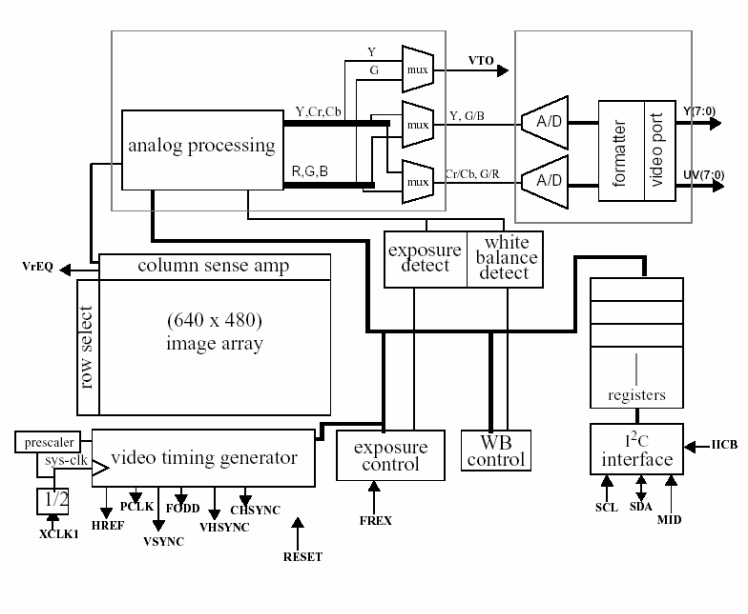

Figure 1 – Structure of OV7620

High integration and possibility of CMOS technology allows implementation of various algorithms for improving the image.

- AWB(Auto White Balance),
- AGC (Auto Gain Control),
- AEC (Auto Exposure Control),
- Windowing

There is a set of internal registers for tuning the image sensor.

Because of defects in the crystal, temperature noise and other influences, different pixels can have different value in equal intensity. Each CMOS image sensor has several defect pixels which always have maximal or minimal value.

External quartz oscillator is used for synchronization. The time diagrams of the synchronization signals are shown in Figure 2.

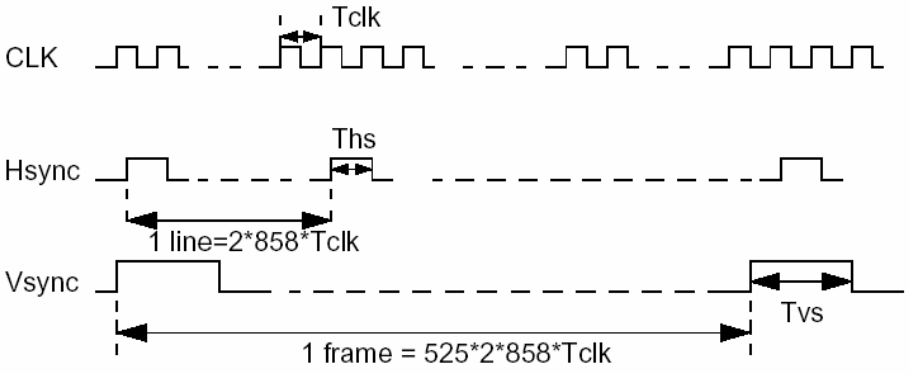

Figure 2 – Time diagrams of the synchronization signals

Psync = 2*CLK – pixel synchronization signal

Hsync = 858 Psync – line synchronization signal

Vsync = 525 Hsync – frame synchronization signal

Signal Psync is continuously generated, but on the data bus there are valid data only if Hsync is in HI state. The described sensor has 8-bits-data bus. The information about each pixel is consecutivly generated. Each pixel is presented with an 8-bit-binary number. Output data is synchronized by rising edge of signal Psync. During the valid data in a line, Hsync is in '1'. At the end of each frame, for frame synchronization Vsync is in '1'.

The aim is the virtual image sensor to be created. It must generate the same signals as a real image sensor. The virtual model of the image sensor was developed in VHDL, because the firmware of the optoelectronic system was developed in the same program language. It allows verification of the algorithms used in the system. The software model allows full control over output data from the sensor, generation of the arbitrary images with desired parameters, generation of the sequence of identical images. The virtual image sensor has to generate the same sequence of output signals as in the real CMOS image sensor. The software model can be implemented in FPGA and the signals from CMOS image sensor can be generated in practice.

VIRTUAL SENSOR DESCRIPTION

The virtual image sensor simulates a real CMOS image sensor. The program code generates output data and all synchronizing signals. The software model is developed with Quartus IV and is written in VHDL [2]. It is used during the development of the firmware of the optoelectronic systems. There is an opportunity for implementation in FPGA development kit. These signals can be generated as real signals and this is useful, because in this way the hardware of the optoelectronic system can be tested.

SOFTWARE MODEL

As a prototype in development of the virtual sensor a real CMOS image sensor OV7620 by Omnivision is used. The virtual sensor can generate images with arbitrary size. All realized algorithms are realized to work independently of the image size. The software model consists of two blocks: a management block and a memory block which are shown in Figure 3.

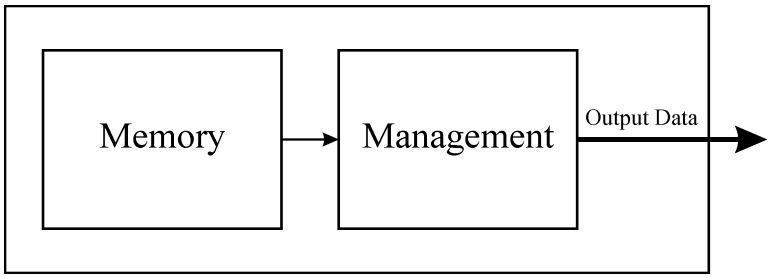

Figure 3 – Structure of the virtual image sensor

The memory block is a data array initialized in advance. It consists of information about each pixel of the image. The array can be with arbitrary size, according to the image size. The frame size is restricted only by the size of the PC memory capacity and by the used FPGA. The data for an image are eight bit binary numbers – MSB first. Each number presents an intensity of a corresponding pixel in the image. The information about the image can be entered in the virtual sensor in several ways. If the image is small the data can be entered by hand. The image can be generated with procedures in MathCAD and saved as 8 bit numbers in a text file. This is useful when the image has large size. With MathCAD real image also can be transformed in a proper format and saved like a text file. After that a contents of the text file can be copied in the virtual sensor's program code.

The management block reads the data from the image array, and outputs the data about each pixel. The structure of the image is the same as in OV7620.

Figure 4 shows a frame of the virtual sensor. The size of frame is 6x5 pixels. Figure 5 shows one line of this frame.

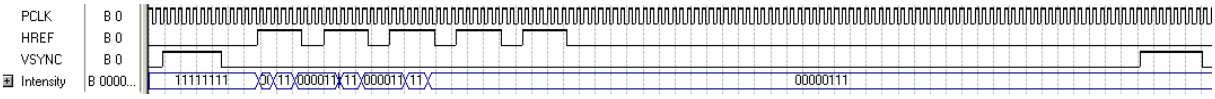

Figure 4 – Output data from a software model

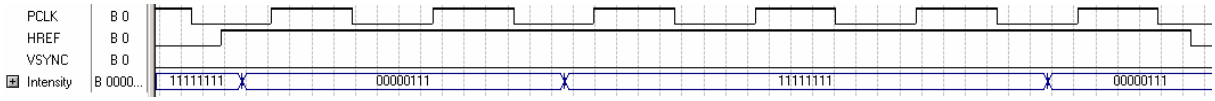

Figure 5 – Output data of one line of the frame in the software model

HARDWARE IMLPEMENTATION

The software model of the virtual sensor can be implemented in FPGA development kit. This is useful if a testing of hardware of the optoelectronic systems is needed. For programming of the optoelectronic system, by a computer, a JTAG interface is used. Figure 6 shows a possible hardware realization of the software model.

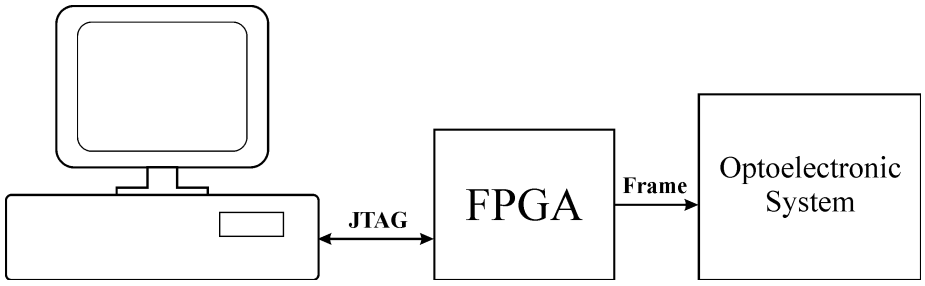

Figure 6 – Hardware realization of the software model

The optoelectronic system is realized by modules. There is a possibility of testing each module separate from the others. The sensor module can be unplugged, and a hardware implementation of a virtual sensor can be attached instead of it. The results on hardware level can be compared with the results achieved by the testing with the software model of the image sensor.

CONCLUSION

The process of developing the virtual sensor was provoced by the developed of an optoelectronic system for processing signals of CMOS image sensor. Using this virtual sensor, various algorithms were tested: dead pixel correction, median filtration, Threshold level calculation and others. The virtual sensor allows the exact testing and checking of all input and output data for each functional block in the optoelectronic system. The software model allows the repeated generation of equal frames and the generation of a sequence of frames with desired parameters. The use of the virtual image sensor confirms its efficiency and its ability to be used instead of a real CMOS image sensor in cases when it is necessary.

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