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FUNDAMENTAL BUILDING BLOCKS FOR MODELING OF RSFQ GATES

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ABSTRACT

This paper deals with two of the fundamental blocks of rapid single flux quantum electronics, namely the single Josephson junction and the Josephson junction comparator. The switching behavior of these blocks are exploited by numerical simulations. The obtained results may be used to derive the behavior of more complex circuits like the Josephson transmission line or the delay flip flop without recourse to further simulations. This can speed up the design process significantly.

Index Terms— RSFQ, fundamental building blocks

1. INTRODUCTION

Rapid Single Flux Quantum (RSFQ) electronics is a digital logic family where the information is coded by the presence or absence of a magnetic flux quantum $\Phi_0 = 2.07 \cdot 10^{-15}$Vs. The active element of RSFQ electronics is the Josephson junction which is a two terminal device. Apart from Josephson junctions, there are also inductors necessary for the correct operation of RSFQ circuits.

A possible way to model complex RSFQ circuits is to use a circuit simulator. Based on this approach one can extract all demanded performance metrics. From a designer point of view it is desirable to have an estimation of the performance prior to the simulation. One possibility to predict the behavior is to decompose the circuit into fundamental building blocks. Since the behavior of the fundamental building blocks is well known, one is able to derive the behavior of the complete circuit.

The method of decomposition makes use of fundamental building blocks. In RSFQ electronics, there are three building blocks, the single Josephson junction, a stack of two Josephson junctions and a storing loop composed of two Josephson junctions connected by a large inductor [1]. Any RSFQ circuit can be decomposed into these three blocks. Since we are interested in the dynamic behavior of the circuit only the single Josephson junction and the Josephson junction stack are of importance.

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2. SWITCHING BEHAVIOR OF A SINGLE JOSEPHSON JUNCTION

The single Josephson junction is used for three different purposes: as a repeater, for data transmission and for decoupling. The switching of a Josephson junction perfectly restores the digital information. This characteristic is mainly exploited in the receiver of a passive transmission line. For short distance one may use a chain of Josephson junctions for data transmission and/or data delay. More advanced cells, e.g., logic gates, data splitters and mergers, are designed such that the static interface currents to adjacent cells are zero. This condition can be effectively fulfilled by appending single Josephson junctions at the inputs and outputs. By this way a decoupling of adjacent cells is ensured. A schematic of a Josephson junction embedded between two inductors and with current source to tune the desired operation point is depicted in Fig. 1.

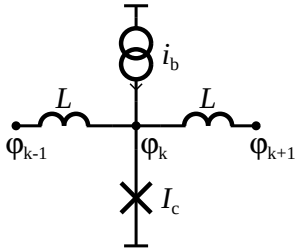

Fig. 1. A Josephson junction symbolised by a cross embedded between two inductors and a bias current source

A Josephson junction may be modeled by the RCSJ (resistively capacitively shunted junction) model depicted in Fig. 2 (the cross symbol of Fig. 1 unifies the complete RCSJ model). It is mathematically described by

the following system of differential equations

$$C\frac{\mathrm{d}u}{\mathrm{d}t} + I_\mathrm{c}\sin(\varphi) + \frac{1}{R_\mathrm{n}}u - i_\mathrm{n} - i_\mathrm{tot} = 0 \quad (1)$$

$$\frac{\mathrm{d}\varphi}{\mathrm{d}t} - \frac{2\pi}{\Phi_0}u = 0 \quad (2)$$

which can readily be implemented in a circuit simulator. The parameters of the junction are its capacitance C, its critical current I_c, and its shunt resistor R_n. The unknowns which have to evaluated during a circuit simulation are the superconductive phase difference φ and the voltage drop u across the Josephson junction. The current i_tot is in general a time dependant excitation of the network, whereas i_n is a Gaussian white noise source caused by the random motion of the electrons within the resistor. It is modeled as the formal derivative of a Wiener process with the following expectation values

$$\mathcal{E}\{i_\mathrm{n}(t)\} = 0 \quad (3)$$

$$\mathcal{E}\{i_\mathrm{n}(t)i_\mathrm{n}(s)\} = \frac{2\mathrm{k_B}T}{R_\mathrm{n}}\delta(t-s) \quad (4)$$

where $\mathrm{k_B}$ is the Boltzmann constant and T is the absolute temperature.

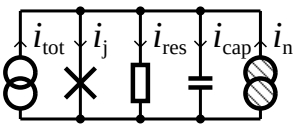

Fig. 2. RCSJ model of a Josephson junction with a noise current source

The switching behavior of a Josephson junction can be studied by investigating the behavior of a long Josephson transmission line (JTL). In Fig. 1 a segment of such a JTL is shown which is replicated to the left and right side several times. The network dynamics are described by the following differential-difference equation

$$\begin{aligned} i_\mathrm{b} &= I_\mathrm{c}\sin(\varphi_k) + \frac{\Phi_0}{2\pi R_\mathrm{n}}\frac{\mathrm{d}\varphi_k}{\mathrm{d}t} + \frac{C\Phi_0}{2\pi}\frac{\mathrm{d}^2\varphi_k}{\mathrm{d}t^2} \\ &\quad -\frac{\Phi_0}{2\pi L}(\varphi_{k-1} - 2\varphi_k + \varphi_{k+1}). \end{aligned} \quad (5)$$

where the linear relationship between inductor current and superconductive phase difference across the inductor is already incooperated. Due to the sine term, this equation is nonlinear and has no known closed form solution. Hence numerical simulations are necessary in order to gain additional insight.

The most important parameter of a single Josephson junction is the time delay t_JJ for the propagation of a single flux quantum. This time delay is caused by the finite switching speed of the junction. There are several possibilities to define the switching time in simulations using either current, voltage or phase information. All possibilities lead to same results, but sometimes one of them is more convenient. If a single flux quantum pulse propagates along the Josephson transmission line from the left to right, a current pulse through the two inductors close to the junction appears. The difference between the location of their maxima is used as the time delay in this paper. The time delay for nominal design values $\mathbf{p}_0$, listed in Table 1, amounts to approximately 5.1 ps. The robustness against process variations can be studied by a numerical sensitivity analysis which assumes a linear dependence between the deviation of a design parameter and the time delay according to

$$t_\mathrm{JJ}(\mathbf{p}) \approx t_\mathrm{JJ}(\mathbf{p}_0) + \left.\frac{\partial t_\mathrm{JJ}(\mathbf{p})}{\partial p_i}\right|_{\mathbf{p}=\mathbf{p}_0} \circ (\mathbf{p}-\mathbf{p}_0). \quad (6)$$

Due to the presence of noise the time delay t_JJ is no longer deterministic, but a stochastic variable τ_JJ. Hence, the mean value μ_τ and the variance σ_τ^2 are adequate measures to characterize the stochastic variable

$$\mathcal{E}\{\tau_\mathrm{JJ}(\mathbf{p})\} = \mu_\tau(\mathbf{p}) = t_\mathrm{JJ}(\mathbf{p}) \quad (7)$$

$$\mathcal{E}\{(\tau_\mathrm{JJ}(\mathbf{p}) - \mu_\tau(\mathbf{p}))^2\} = \sigma_\tau^2(\mathbf{p}) \quad (8)$$

where $\mathcal{E}$ denotes the expectation operator. In Table 1 the results of the sensitivity analysis are summarized. The maximum deviation from the straight line approximation are 0.3% and 1.6% for the sensitivity of the mean value and the variance, respectively. The capacitance has the least influence of all parameters on both expectation values. The sensitivity to the shunt resistor and the inductor are equal but with different sign. The effect of the critical current is even higher on the switching speed than for the former parameters. The bias current determined by the measurement setup has the highest influence at all.

Another important parameter is the correlation between the time delays of two adjacent Josephsons junction of the JTL. It is a measure for the influence of the noise current of one junction on the switching behavior of the other one. In our simulations the correlation coefficient was -0.08. The minus sign means that a fast switching of the first junction entails a slower switching of the second junction and vice versa. A correlation coefficient of one corresponds to fully correlated switching times.

The knowledge of the behavior of a single junction can be used to derive the timing behavior of a JTL comprising 20 Josephson junctions. The mean value for the time delay of pulse propagating on a JTL obtained by a simulation agrees very well with the estimated value. However, applying this method to the variance of the time delay a discrepancy appears. Due to the anticorrelated switching speed of two adjacent junctions the overall variance is overestimated. All values are summarized in Table 2.

Table 1. Numerical sensitivity analysis of the the mean value and the variance of the switching time of a Josephson junction embedded within a JTL. 16000 events were used to estimate the statistical quantities.

p_i	p_{0i}	$\left.\frac{\partial \mu_{\mathrm{JJ}}}{\partial p_i}\right\|_{\mathbf{p}=\mathbf{p}_0}$	$\left.\frac{\partial \sigma^2_{\mathrm{JJ}}(\mathbf{p})}{\partial p_i}\right\|_{\mathbf{p}=\mathbf{p}_0}$
I_{c}	250 μA	$\frac{319\mathrm{fs}}{12.5\mu\mathrm{A}}$	$\frac{1.59\cdot 10^{-3}(\mathrm{ps})^2}{12.5\mu\mathrm{A}}$
C	1.30 pF	$\frac{64\mathrm{fs}}{65\mathrm{fF}}$	$\frac{0.11\cdot 10^{-3}(\mathrm{ps})^2}{66\mathrm{fF}}$
R_{n}	1.00 Ω	$-\frac{147\mathrm{fs}}{0.05\Omega}$	$-\frac{1.57\cdot 10^{-3}(\mathrm{ps})^2}{0.05\Omega}$
L	2.00 pH	$\frac{175\mathrm{fs}}{0.2\mathrm{pH}}$	$\frac{1.21\cdot 10^{-3}(\mathrm{ps})^2}{0.2\mathrm{pH}}$
i_{b}	175 μA	$-\frac{360\mathrm{fs}}{8.75\mu\mathrm{A}}$	$-\frac{2.51\cdot 10^{-3}(\mathrm{ps})^2}{8.75\mu\mathrm{A}}$

Table 2. Comparison of estimated and simulated delay time values of a JTL comprising 20 Josephson junctions

Parameter	single junction	estimation for JTL	simulation of JTL
μ [ps]	5.12	102.4	102.5
$\sigma^2[(\mathrm{ps})^2]$	0.016	0.032	0.027

3. SWITCHING BEHAVIOR OF A JOSEPHSON JUNCTION COMPARATOR

The Josephson junction comparator is not only one of the fundamental building blocks of RSFQ circuits, but it is also used in superconductive analog-to-digital converters or in Josephson sampler circuits. In these applications the performance is often limited by the switching behavior of the Josephson comparator. The Josephson comparator is a 1-bit quantizer with three limiting parameters: first the threshold uncertainty (grayzone width), second the decision time to output a "0" or a "1" and third the variance of the decision time.

A Josephson junction comparator is normally driven by a continuous stream of SFQ pulses generated by the driver junction J_1. In an idealized RSFQ circuit with no thermal noise sources the SFQ pulses are equally separated by the sampling clock period t_{s}. For a sufficiently large sampling clock period either the upper J_2 or the lower J_3 comparator junction switches depending on the signal current i_{sig} (Fig. 3(a)). The switching behavior $pr_3(i_{\mathrm{sig}})$ of the junction J_3 of a Josephson comparator is depicted in Fig. 3(b). It can simply be expressed by a Heaviside step function

$$pr_3(i_{\mathrm{sig}}) = h(i_{\mathrm{sig}} - \mu_{\mathrm{sig}}). \qquad (9)$$

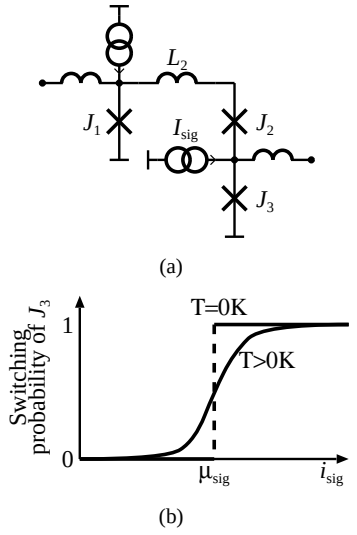

Fig. 3. A single Josephson junction (a) and a Josephson comparator (b) are two fundamental building blocks for RSFQ circuits

Due to the presence of noise in a real world circuit ($T > 0$K), the step function will be smoothed as indicated in Fig. 3(b) and the following equation holds

$$pr_3(i_{\mathrm{sig}}) = \frac{1}{2} + \frac{1}{2}\mathrm{erf}\left(\sqrt{\pi}\frac{i_{\mathrm{sig}} - \mu_{\mathrm{sig}}}{\Delta i_{\mathrm{sig}}}\right) \qquad (10)$$

where Δi_{sig} is defined as the grayzone width and erf is the error function.

If the lower junction switches, an SFQ pulse propagates from the left to the right with certain stochastic time delay characterized by its mean value μ_{JC} and variance σ^2_{JC}. For the comparator we used the phase information to define the time delay by evaluating the time difference between the location of the phase value of 5 of one of the comparator junctions and the driver junction J_1. The time delay is very susceptible to any change of the signal current i_{sig}, but also, as in the case of a single junction, to inductor and junction parameter values. In comparison to the time delay of the single junction much higher values are obtained. In Fig. 4 one can see the dependence of the mean value and standard deviation of the time delay for different signal current levels. The mean switching time and its variance of one of the comparator junction augments inversely to its switching probability. The maximum switching time for the upper μ_{JC2} and lower μ_{JC3} is about 25 ps, i.e., 5 times higher than for single Josephson junction. The standard deviation reaches levels of 8 ps which corresponds to a JTL of 65 junctions.

In Table 3 the grayzone width is compared with the two timing parameters. Evidently, there is a trade-off between fast switching and a reliable decision. Especially, the reduction of 50% of the grayzone width yields a four fold increase of the switching time and 20

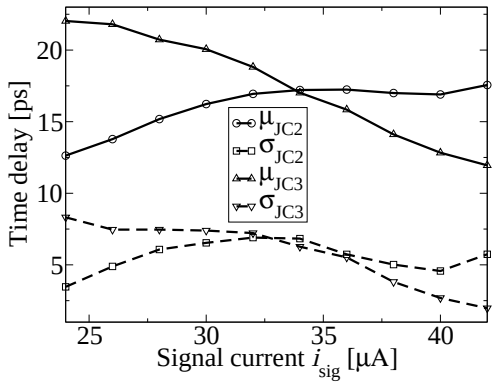

Fig. 4. Timing behavior of a the two comparator junctions for a bias level of 350 μA

Table 3. Comparison between the grayzone width and timing parameters for different bias levels

i_{b} [μA]	Δi_{sig}	μ_{JC} ($pr_3 = 0.5$)	σ_{JC} ($pr_3 = 0.5$)
320	5.5 ps	50 ps	38 ps
350	10.4 ps	18 ps	7 ps
380	11.2 ps	13 ps	2 ps

fold increase of its standard deviation.

4. MODELING OF A DELAY FLIP FLOP

The delay flip flop (DFF) is used as a flux storing element. In Fig. 5 the schematic of a DFF is shown. Apart from a connected JTL on the right hand side of the lower comparator junction, a second load, a storing loop, appears on the left hand side. The basic idea of our modeling approach is not simulate the circuit as a whole, but to unify the two loads in a single one, so that results of the previous section can readily be used.

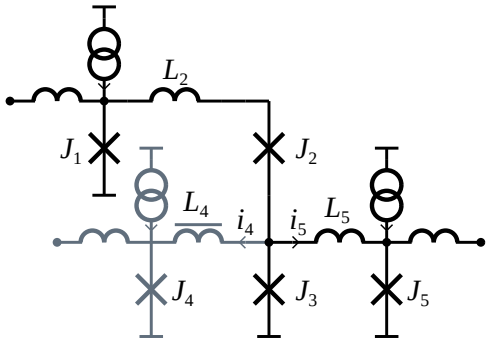

Fig. 5. Delay flip flop having a storing loop as a load on the left hand side of the lower junction

At the joining point of the two comparator junctions the differential currents are distributed according to an inductive current divider according to

$$\frac{i_4}{i_5} \approx \frac{L_5 L_{J_5}}{L_4 L_{J_4}} \tag{11}$$

where the differential Josephson inductance of a junction depending on its phase drop φ is defined by

$$L_J = \frac{\Phi_0}{2\pi I_{\mathrm{c}} cos(\varphi)}. \tag{12}$$

5. SUMMARY

Adapted from the behavior of two fundamental building blocks, the single Josephson junction and the Josephson junction comparator, the timing behavior of more complex circuits may be derived without further numerical simulations. In the case of the Josephson transmission line the calculated mean value of delay time and the simulated agree perfectly whereas the calculated jitter is approximately 20% above the simulated value due to anticorrelated switching of the junctions. A second example the delay flip flop seems to be attractive for estimations based on the Josephson junction comparator, but further investigation are still necessary. In summary, the method of decomposition enables the designer to choose adequate parameters for complex circuits prior to a detailed Spice simulation and, therefore, accelerates the design cycle significantly.

6. REFERENCES

[1] D.K. Brock, E.K. Track and J.M. Rowell, "Superconductor ICs: the 100-GHz second generation," *IEEE Spectrum*, vol. 37, pp. 40–46, December 2000.