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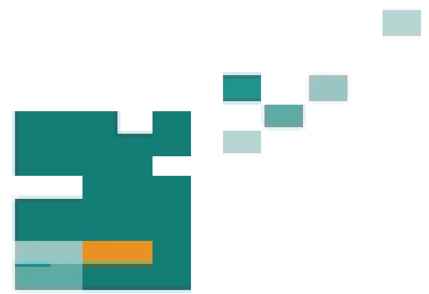

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11-15 September 2006

FACULTY OF ELECTRICAL ENGINEERING AND INFORMATION SCIENCE

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51st Internationales Wissenschaftliches Kolloquium
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Diana Pannicke, Sören Hirsch, Reinhard Mikuta, Edmund P. Burte, Bertram Schmidt

Research on an Under-Bump-Metallization for lead free Flip-Chip-Process

Micro- and Nanoelectronics

Abstract

The under bump metallization (UBM) is an important part of the flip chip technology. Lead containing solder materials were used in the past, but environmental laws ban the use of lead in electronic products from July 2006. This paper shows a low-cost and stable production process for lead-free flip chip connections. The UBM was analyzed and characterized e.g. by a suitable sample preparation, scanning electron microscopy (SEM) and focus ion beam (FIB).

Introduction

Packaging technology is still of great relevance and has to fulfill the growing demands of the industry and the costumers. Improvements in existing technologies and new innovations are required. The driving forces for that are manifold. Higher component integration and system integration into the package, higher clock frequencies, lower loss factor densities and, most importantly, the environmental and cost factor ask for new packaging solutions.
Since environmental protection is fundamental, the industry focuses on lead-free manufacturing processes. Lead leaks out of the package and electronic waste can therefore poison soil and ground water. Thus lead can harm plants, animals and humans. The ground water contamination was the principal reason for the European Union to adopt laws, which ban lead from electronic production. The concerning regulations WEEE (Waste Electrical and Electronics Equipment) and ROHS (Restrictions on the use of Hazardous Substances) become effective from July 1st 2006 [1].

Due to these rules and the demand for shortest connecting lengths and high function densities direct packaging of integrated circuits (chips) on printed circuit boards, like flip chip technology, becomes more and more attractive. Apart from the miniaturization flip chip technology has advantages in process costs. Solder bumps are deposited on the connection pads and the chip is soldered face-down on the circuit board. The chip is fixed and contacted at the same time with its active side on the substrate [2].
To introduce flip chip as a “green”, i.e. lead-free, technology extensive research has to be done. One important issue is the reliable application of flip chip electronics in high-temperature environments particularly in the automotive industry.
Flip chip connections are formed by solder bumps on the contact pads. Unlike in wire bond technology the aluminium oxide layer on the contact pads is not broken by screen printing the bumps on the chip. This means poor mechanical and electrical properties and stability. To overcome this disadvantage an under bump metallization (UBM) is necessary. The UBM acts as diffusion barrier and forms a stable soldered connection to the lead-free bump. Further the UBM protects the contact pad from oxidation, forms a low contact resistance, adheres to the aluminuim and is reliable under to mechanical and thermal stress [3].
The reflow process requires good wetting and soldering characteristics of the UBM. This can be accomplished by a combination of different layers, only. Though the metallisation is done in several steps the process has to be simple, cost-effective, reproducible and suitable for batch production.
The different objectives, like miniaturization, environmental protection, temperature sensitiveness and so on, leave space for further investigation and many material combinations.
This paper presents a complete, reproducible and low-cost flip chip process and analyses the UBM.

Fabrication

For the UBM fabrication the thin oxide layer and contaminations on the contact pads are removed by sputter etching. The undercoating (Cr), the diffusion layer (Ni), the solder layer (Cu) and the passivation layer (Pd) are deposited by evaporation. This layer sequence was chosen because of the metals’ favorable properties and their compatibility to each other. There is very little stress in the metal layers.

Figure 1 shows the layer sequence of the UBM with the respective thickness. The under bump metallization was deposited in an octagon on the aluminium pad to promote the development of a rounder meniscus of solder after reflow. The structure is demonstrated in figure 2. The UBM is 10 µm smaller than the aluminium contact pad.

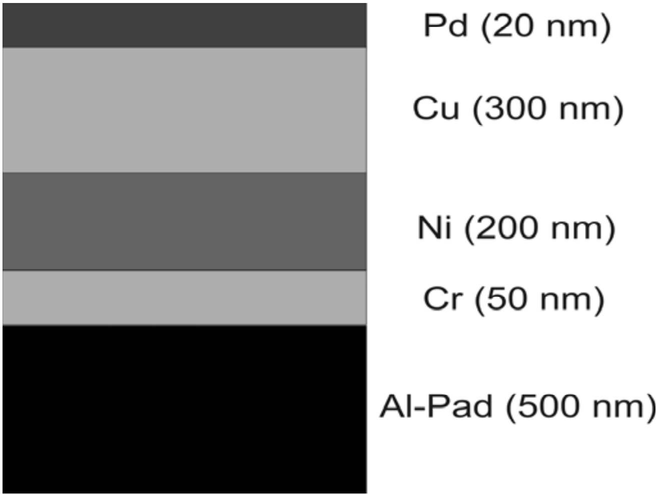


Figure 1: UBM layer sequence with respective thicknesses for a lead free flip chip-process

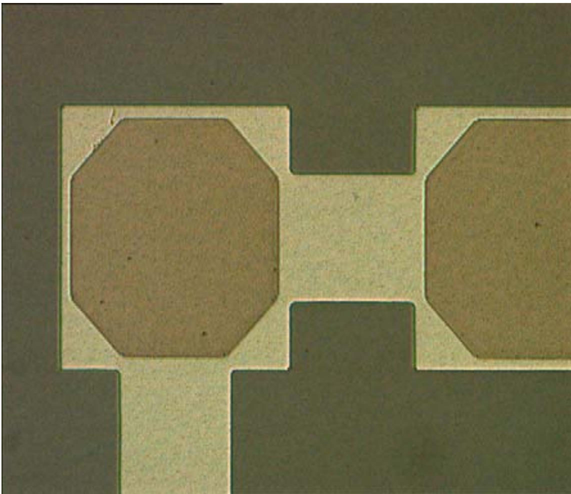


Figure 2: Test structure UBM

After manufacturing the UBM on the aluminium pad, the wafer was coated with solder paste by screen printing technology. Afterwards the solder bumps are formed in a reflow process. The temperature profile is shown in figure 3 and figure 4 shows the bumps after reflow.

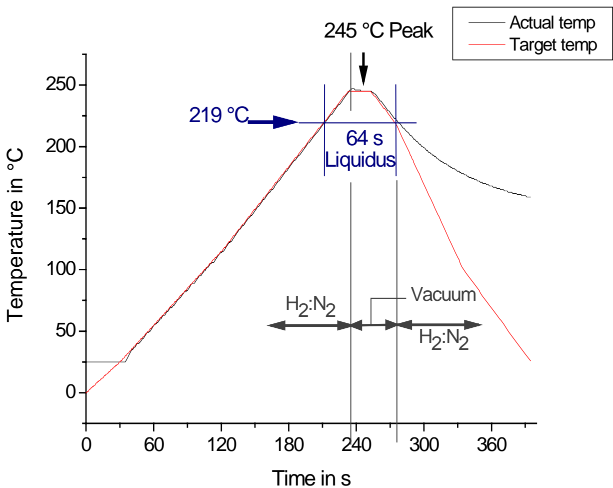


Figure 3: Reflow process for lead free solder paste Sn95.5Ag4Cu0.5

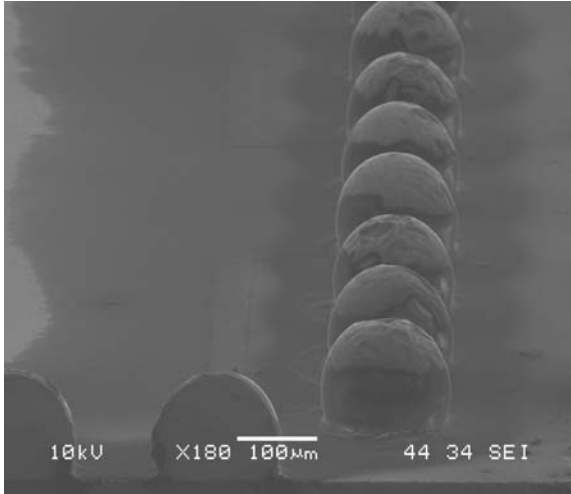


Figure 4: Solder bumps after reflow (SEM)

To analyze the interface between the UBM and the solder bump after reflow assess the quality a sample preparation was done.
Several preparation approaches were done to find the best result as the preparation of a combination of soft and hard materials is a challenge.
The resulting process is shown in figure 5. The procedure starts with dicing the wafer, continues with grinding and polishing and finally the specimen is embedded in an compound. Also the abrasive, lubricant and compound have to match the physical properties of the specimen.

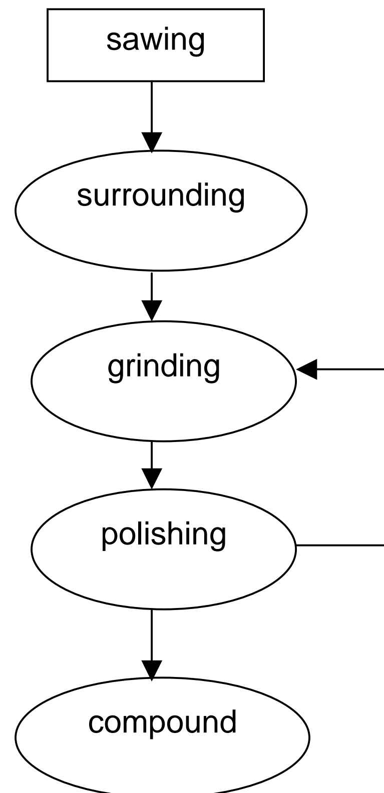


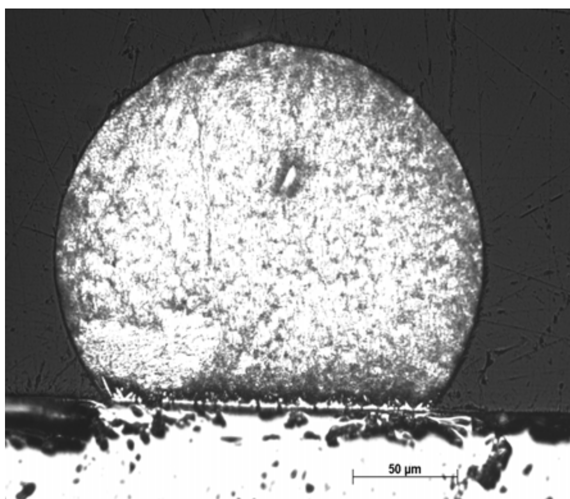
Figure 5: Preparation steps

Generally SiC paper is used to grind soft and middle hard materials. The specimen consists of the hard silicon and the soft Sn95.5Ag4Cu0.5 solder bumps. To prevent edge rounding and scratches in the silicon the correct abrasive and grinding time has to be chosen.
Epoxy resin was used to embed the specimen because of its transparence, the low curing temperature and viscosity. These properties are advantageous for electronic devices.
After sample preparation the material combination was analyzed macroscopically to find defects like bad solder assembly and voids in solder bumps. For fine grinding a sequence of SiC papers was used (300 grains per inch, 600 grains per inch, 4000 grains per inch). The polish was done with a 1 µm steel polishing wheel and 1 µm diamond suspension adding an alcohol based lubricant. This results in a high accuracy polish without defects.

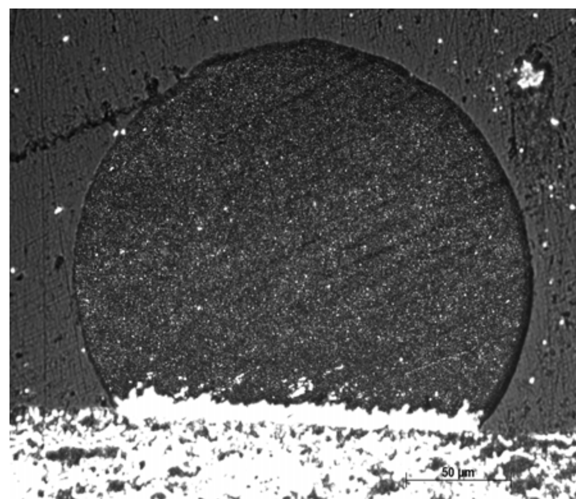
Analysis and Results

The finished preparation is shown in figure 6. To analyze the UBM and to check for voids or other abrasive mistakes in the bumps the sample was etched with ammonium persulfate. Figure 7 reflects the result of the etching. The intermetallic phase Cu_6Sn_5 between the UBM and solder bump is clearly visible. The Cu_3Sn phase was not generated, because the maximum temperature of the reflow profile was 245°C. After reflow a meniscus and a good solder contact is generated.

Figure 6: Sample after preparation in comparison to a biro



a)



b)

Figure 7: Ammonium persulfate etching to see the intermetallic phases, (light microscopy, magnification 500) a) after 1 minute, b) after 5 minutes

In figure 8 and 9 show SEM analyses to examine the intermetallic phases. The concretions of the material after polishing are removed with FIB. So a better analysis is possible. The UBM is visible in both figures. The Cu_6Sn_5 intermetallic phase extends approximately 4 µm into the bump. Furthermore a nickel tin intermetallic phase has developed. The Ni_3Sn_4 phase is much thinner (approx. 250 nm). The copper layer

disolved in the SnAgCu-bump.

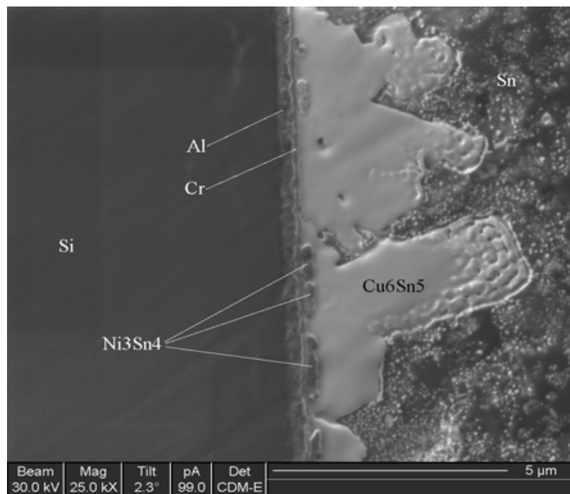


Figure 8: SEM analysis after ammoium persulfate etching

Layer sequence: Si, Al, Cr, intermetallic phases: Cu_6Sn_5, Ni_3Sn_4

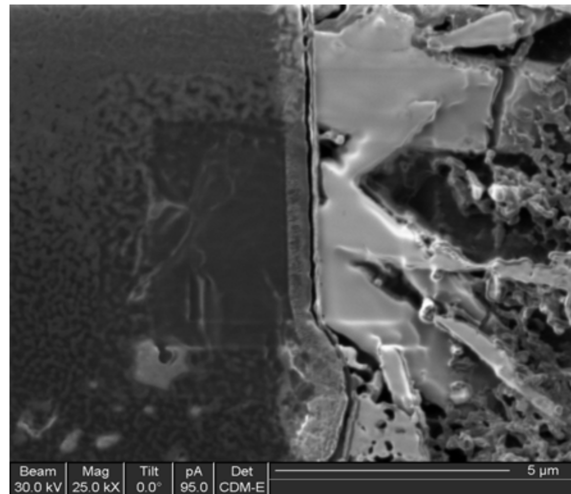


Figure 9: SEM analysis after FIB

Layer sequence: Si, Al, Cr, intermetallic phase: Cu_6Sn_5

Conclusion

The experiment and the following analyses with microscopy, etching and SEM show that the copper layer of 300nm is not thick enough to save one process step to leave the nickel. The solder process takes place on nickel. For the future the copper layer should be much thicker like 500 - 600 nm.

It could be shown that the soldering was successful with the suitable reflow profile and that no voids or other defects were found. Furthermore the two intermetallic phases Cu_6Sn_5 and Ni_3Sn_4 were found and analyzed.

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