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51. Internationales Wissenschaftliches Kolloquium
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B. Ebert, S. Humbla, A. Fell, T. Ortlepp, F. H. Uhlmann

Design of an ultra fast superconductor-to-semiconductor interface

INTRODUCTION

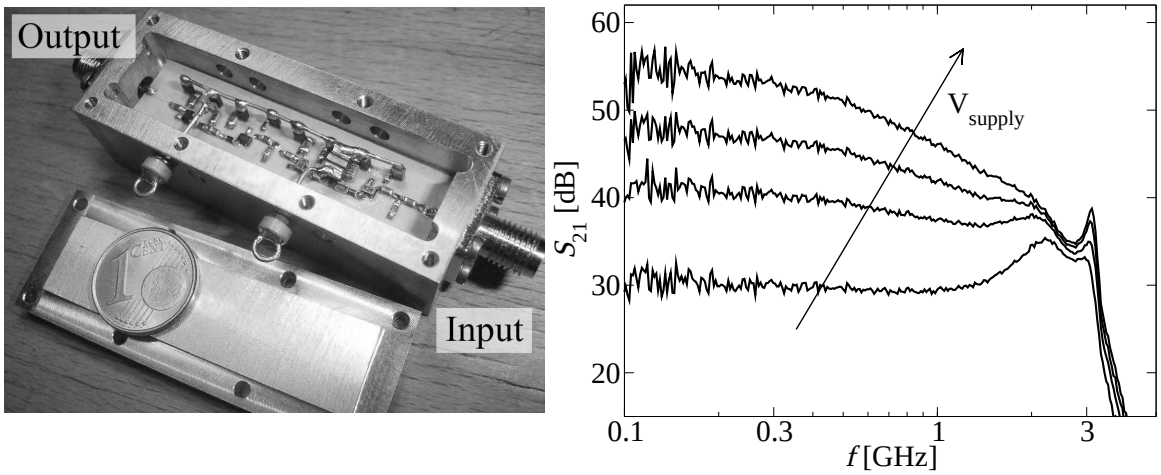
The superconductive Rapid Single Flux Quantum (RSFQ) electronic is capable to outperform conventional semiconductor electronics by speed and power consumption. Although fabrication technology has matured and efficient cryocoolers are available, there are still some obstacles which hinder a wide range application of this promising technology. One of these unsolved problems is the interface between the superconductive circuit and the semiconductive room temperature electronics.

Coupling in a direct manner superconductive and semiconductive chips or also measurement systems is not practicable for several reasons: First there is an impedance mismatch because the line impedance of superconductor chips amounts to approximately 4 Ω while cables for the interconnection have normally 50 Ω. Second the output voltage of RSFQ logic amounts to several hundreds of microvolts. Hence a voltage gain of 80 dB is required to achieve standard voltage levels of semiconductor logic families. According to the high clock frequency a third subproblem arises. If the high performance potential of RSFQ circuits is fully exploited, the data stream coming from the superconductive chip will reach several GBits per second. The last two subproblems lead to the design of a low noise broadband amplifier. Superconductive circuits are always accommodated in a cooling system, therefore it is reasonable to cool down the amplifier as well to cryogenic temperatures (e.g. 77 K) for the sake of noise reduction and gain improvement.

Combining transmission lines with different impedances and waveguide types over a broad frequency- and temperature range results in a complex design process due to the occurring mismatch [1]. In general mismatch causes reflections which affect the signal source and reduce the already small amplitude of the signal coming from the RSFQ circuit. The superconductive chip is mounted on a printed circuit board serving as a chip carrier. On the chip carrier the waveguide type is coplanar whereas microstrip line structures are implemented on the chip. Interconnections between the chip and the carrier are realised with bond wires. Hence the waveguide type transformation has already to be accomplished on the superconductive chip. The impedance matching between 4 and 50 Ω can be effected partly on the chip or on the printed circuit board depending on the impedance range of the bond wires.

Designing a cryogenic amplifier necessitates semiconductor technology which does not suffer under the low temperature working environment [2]. Hence transistors made of GaAs compounds are a good choice, but cost restraints lead to the use of SiGe bipolar heterojunction transistor [3] like the Infineon BFP620. An additional limitation is the overall power dissipation of the amplifier which should not exceed several mW owing to the limited heat removal capacity of the cryocooler.

A two stage common-emitter amplifier was designed for room temperature [4, 5] and showed good agreement to the measurement results. So the two stage discrete amplifier was enhanced to four stage amplifier. The correct working of this circuit has been successfully demonstrated with a cut-off frequency of 3 GHz and a linear gain of 40 dB (fig. 1 (b)). Using a cascode amplifier should reach in comparison with a common-emitter stage even higher cut-off frequencies by maintaining the gain. Due to the common-base stage the cascode amplifier tends to oscillate at high frequencies which was confirmed by the measurements. By reducing the temperature it could be shown that gain and noise behavior of the tested four stage amplifier have improved considerably.



(a) (b)

Fig. 1. (a) Four stage amplifier (b) S_{21}-Parameter measurement of the amplifier for different supply voltages

GENERAL CONSIDERATIONS ON THE DESIGN FLOW PROCESS

Nowadays the circuit design process makes extensively use of numerical simulation tools. The main purpose of this is to predict circuit behaviour in a fast and accurate way. Nevertheless the accuracy of the simulation depends predominantly on the models for active and passive devices as well as for the interconnections between the lumped elements. Manufactures provide quite often models for their devices but these specifications are only valid for a certain temperature which is normally room temperature. Physical properties change over temperature and so it is obviously that room temperature specifications are no longer suitable for simulations of circuits which are intended to be embedded in a cryogenic environment. Thus the first work step in a design flow has to be the specification of devices at cryogenic temperature. Feeding simulation tools with these cryogenic models is the way for obtaining results which are close as possible to the measurement.

CHARACTERIZATION OF PRINTED CIRCUIT BOARDS

The printed circuit board (PCB) is the carrier of all other active and passive components. As long as the length of the PCB considered as a discontinuity is below $\lambda/20$ of the highest frequency, the influence of the board on the electrical behaviour can be neglected. For the transmission of a 1 GHz signal on a standard board with an effective permittivity $\epsilon_{r,eff}$ of 2.5, the signal path should not exceed

$$\lambda/20 = \frac{c_0}{20\sqrt{\epsilon_{r,eff}}f} \approx 1\text{cm} \tag{1}$$

whereas c_0 equals to the velocity of light and f is the frequency. Especially in multi-stage amplifiers this length will be significantly above the assumed value and so the effects of substrate have to be encountered.

The two main substrate parameters are the permittivity ϵ_r and the dielectric loss factor $\tan(\delta)$. A half-wave microstrip resonator in combination with a network analyzer is the simplest mean to determine both of them. The transmission coefficients $s_{21} = s_{12}$ exhibit several peaks above the first resonant frequency f_{res}. This frequency allows to calculate the effective permittivity by

$$\epsilon_{r,eff} = \left(\frac{2lf_{res}}{c_0}\right)^2 \tag{2}$$

whereas l is the length of half-wave resonator. There are software tools which are capable to extract the permittivity of the substrate based on the effective permittivity and the substrate height. Beside the resonant frequency there are a lower and an upper 3-dB cut-off frequency f_l and f_u respectively. Neglecting losses caused by radiation and conductance the loss factor is determined by

$$\tan(\delta) = \frac{(f_u - f_l)(1 - |s_{21}|)}{f_{res}}. \tag{3}$$

CHARACTERIZATION OF SURFACE MOUNTED CAPACITORS

Using surface mounted capacitors in high frequency applications, the equivalent circuit is no longer a sole capacitor but a series circuit of capacitor C, resistance R and inductance L. The self-resonant frequency can be found at

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}.$$

The parasitic inductance is owing to the leads of the capacitor. To minimize the inductance it is advisable to use small packages, which have the drawback of providing only small capacitance values.

The equivalent series circuit is linear and so a network analyzer can be used to determine the values of the elements. The capacitor is mounted on printed circuit board and is connected by a 50 Ω microstrip transmission line to the coaxial cables of the network analyzer. Consequently, it represents a series impedance and the scattering parameter $\underline{s}_{11}(\omega)$ provides all information to calculate the equivalent elements:

$$R = 2Z_0 \Re\left\{\frac{\underline{s}_{11}(\omega)}{1 - \underline{s}_{11}(\omega)}\right\} \tag{4}$$

$$C = \frac{\omega}{2Z_0}\left(\frac{1}{\omega_{res}^2} - \frac{1}{\omega^2}\right) \Big/ \Im\left\{\frac{\underline{s}_{11}(\omega)}{1 - \underline{s}_{11}(\omega)}\right\} \tag{5}$$

$$L = \frac{2Z_0\omega}{\omega^2 - \omega_{res}^2} \Im\left\{\frac{\underline{s}_{11}(\omega)}{1 - \underline{s}_{11}(\omega)}\right\} \tag{6}$$

LINEAR TRANSISTOR MODELING AT CRYOGENIC TEMPERATURES

The Gummel-Poon parameters of a bipolar transistor [6, 7] provided by the manufacture are not suitable for the design of cryoelectronic circuits. A correct description of the behaviour of the transistor is a crucial step in the design process. The simplest way to do this is a S-parameter measurement of the transistor. A DC power supply is needed for setting up the desired operating point of the transistor. If the ac signal amplitudes of the input and output are small enough to prevent nonlinear effects, the transistor behaves like a linear two port. Hence can be described by its S-parameters.

The measured S-parameters are only valid for a single operating point and consequently in the simulation an appropriated resistive bias network has to be chosen in order to obtain correct prediction of the circuit behaviour. Nonetheless, due to the linear nature of the model, nonlinearities will not be observed in the simulation. Although there is no problem to capture the S-parameters at various temperature, this linear approach is not practical to make general derivations on temperature behaviour or even to extract the physical reasons of changes in the device characteristic. Overcoming this drawback demands the introduction of a nonlinear model which encounters physically based parameters.

NONLINEAR TRANSISTOR MODELING AT CRYOGENIC TEMPERATURES

There are several approaches for modeling nonlinear behaviour. Some approaches demand intrinsic structure, dotation levels and other physical parameters which are not available for off-the-shelf components. Other approaches such as the Gummel-Poon model using approximation functions to characterize the transistor. Although it takes some time to determine all parameters [8], simulation results will be more accurate

then those of the linear model. Moreover, the temperature dependence of the parameters can be easily derived, so that an optimization with respect to the final operating temperature can be done.

Extracting the parameters necessitates static I-V and C-V curve tracing as well as some S-parameter measurements. A de-embedding process has carefully to be applied in order to exclude packaging and test fixture parasitics [9]. With these results specialized software tools can determine the parameters by fitting the approximation functions to the measurement curves.

SYSTEM INTEGRATION AT CRYOGENIC TEMPERATURE

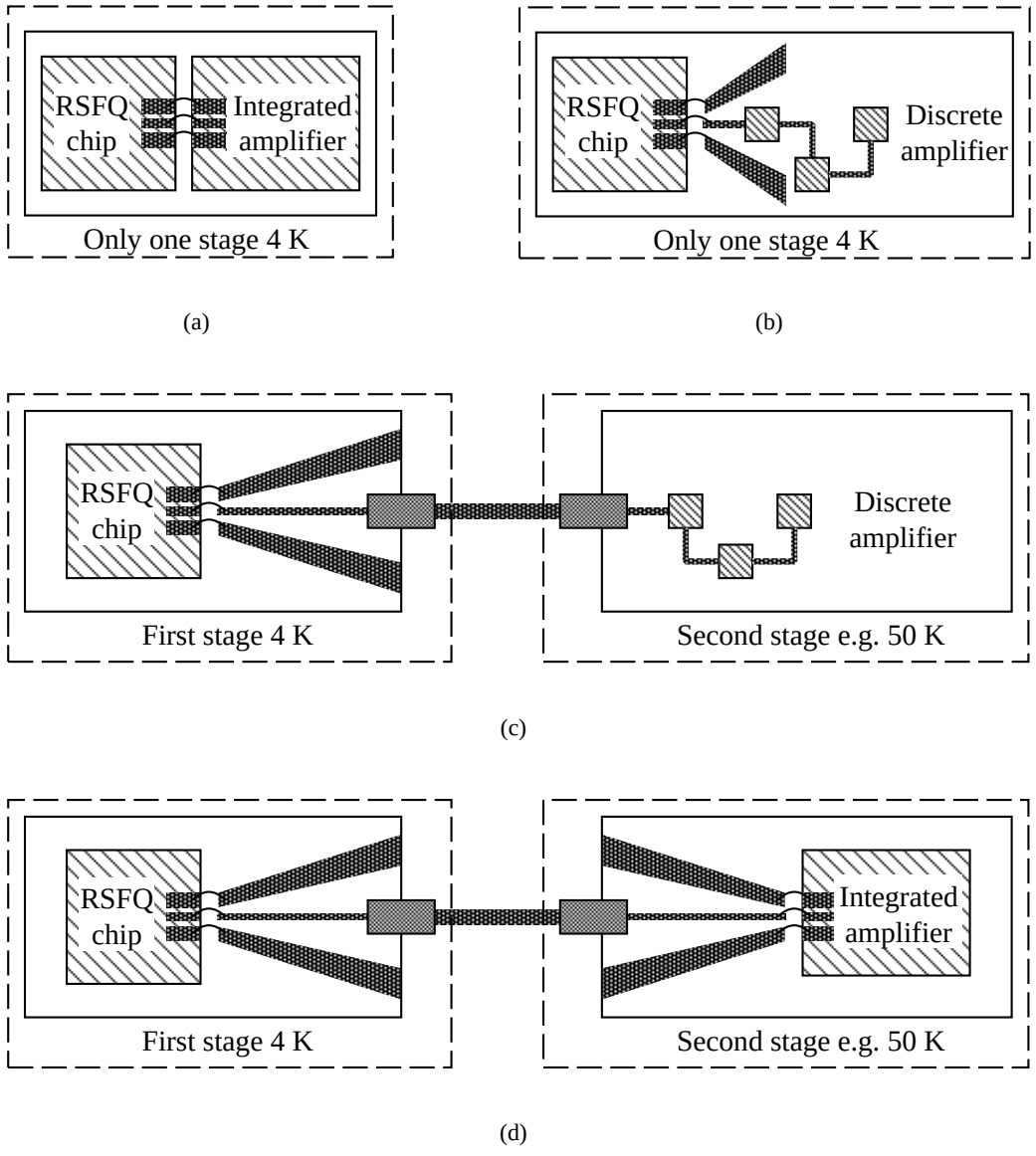


Fig. 2. Possible configurations to realize a superconductor-to-semiconductor interface

Once all parameters of active and passive devices are available, the design optimization process of the amplifier can be started. The next step is to connect the amplifier with the superconductive chip. Whether the amplifier is integrated (Fig. 2 (a)) or is built up with discrete devices (Fig. 2 (b)), it has to be placed as close as possible to the RSFQ-chip. Amplifiers capable to operate at 4 K like niobium based RSFQ chips are suitable to fulfill this requirement. Using an integrated amplifier alleviates the impedance matching, because the distance between the two chips can be considered as electrical small up to several GHz. Additionally,

more than one amplifier could be integrated. A discrete amplifier is the second choice because a coplanar to microstrip transmission line conversion has to be accomplished and a broadband impedance transformation from 4 Ω on the RSFQ chip to the input impedance of the amplifier is obligatory. If the power dissipation of the amplifier exceeds the heat removal capacity of the entire system, it has to be placed in a second stage of the cryostat which has a higher operating temperature and supports a greater power dissipation. In this case, the connectivity is the main challenge because it has to be dimensioned with regard to the characteristic impedance of coaxial cable linking the two stages of the cryostat. Even thoroughly matched, the coplanar to microstrip and microstrip to coaxial conversions will produce multiple reflexions disturbing the digital signal stream and perturbing the sensitive output of the RSFQ chip. The setup with a discrete amplifier shown in figure 2 (c) is preferable because it renders dispensable the microstrip to coplanar conversion required by the integrated amplifier (Fig. 2 (d)).

LOW TEMPERATURE MEASUREMENTS

Performing measurements at cryogenic temperature is a very challenging task. The device under test (DUT) is enclosed by a cryocooler and so it is more distant from the measurement instrument than it would normally be. Measurement accuracy is deteriorated by cable losses and electromagnetic interference could occur due to not properly shielded cables. Another aspect is calibration which is made at room temperature, cooling down the DUT will change the characteristic of the measurement system. Consequently, appropriate cables have to be chosen which do only slightly change their electrical properties e.g. characteristic impedance, phase velocity and attenuation in comparison to a room temperature environment. If this is the case, the performed calibration is also valid for measurements at cryogenic temperatures. Low loss cables have a good electrical conductance and thus also a good thermal conductance. Care has to be taken that the heat introduced in the cryocooler by the cables does not exceed his heat removal capacity.

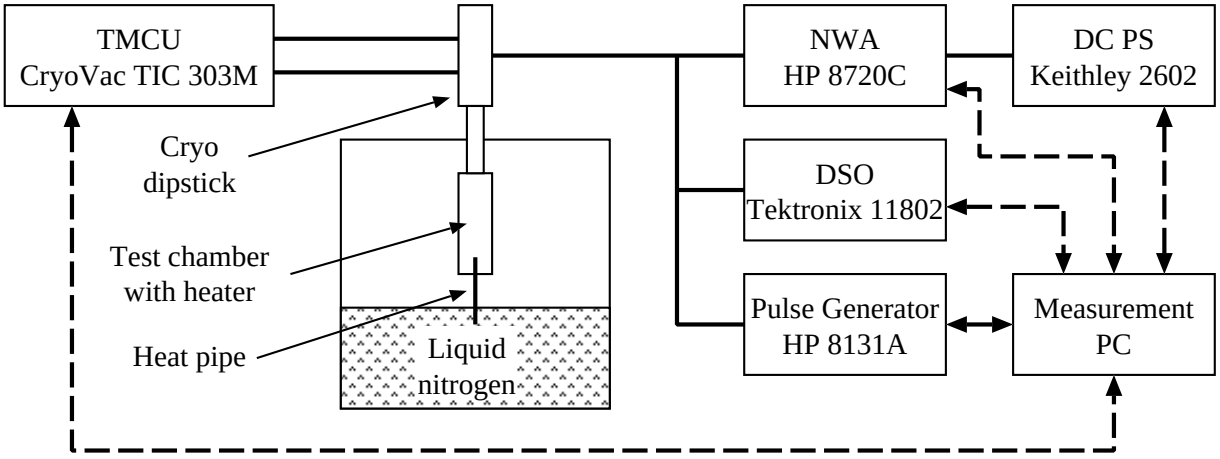


Fig. 3. Measurement setup for DC and RF measurements at various temperatures down to 77 K

The measurement setup is shown in figure 3. It consists of a bottle of liquid nitrogen, a cryo dipstick, a temperature measurement control unit (TMCU) and various instruments for DC and RF measurements. At the bottom of the cryo dipstick there is a test chamber in which the device under test is mounted. This chamber is connected by a heat pipe to the liquid nitrogen so that the probe can be cooled down to 77 K. A simple resistance within the chamber serves as a heater capable to adjust the desired temperature. The actual temperature, measured with a diode, is compared with the target value. Any deviation would lead to a modification of the heat power delivered by TMCU.

DC measurements can be accomplished by connecting the power supply (PS) directly to the cryo dipstick or by connecting them to the internal bias tees of the network analyzer (NWA). Time domain measurements are performed by a pulse generator in combination with a digital sampling oscilloscope (DSO). The whole system is controlled by software programs via GPIB interface.

CONCLUSION

This paper summerizes all steps necessary to design a superconductor-to-semiconductor interface. At the beginning of the design process stands the characterization of all components at cryogenic temperature. The components comprise the printed circuit board, surface mounted capacitors and transistors. In order to obtain the parameters, a low temperature test system was proposed. Due to the temperature measurement control unit, the test system has the capability to adjust any temperature between 77 K and room temperature. At last, an overview of different superconductor-to-semiconductor interface configurations is given.

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