51. IWK

Internationales Wissenschaftliches Kolloquium
International Scientific Colloquium

PROCEEDINGS 11-15 September 2006

FACULTY OF ELECTRICAL ENGINEERING AND INFORMATION SCIENCE

INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING - DEVICES AND SYSTEMS, MATERIALS AND TECHNOLOGIES FOR THE FUTURE

Startseite / Index:
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TECHNISCHE UNIVERSITÄT
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Impressum

Herausgeber: Der Rektor der Technischen Universität Ilmenau
Univ.-Prof. Dr. rer. nat. habil. Peter Scharff

Redaktion: Referat Marketing und Studentische Angelegenheiten
Andrea Schneider

Fakultät für Elektrotechnik und Informationstechnik
Susanne Jakob
Dipl.-Ing. Helge Drumm

Redaktionsschluss: 07. Juli 2006

Technische Realisierung (CD-Rom-Ausgabe):
Institut für Medientechnik an der TU Ilmenau
Dipl.-Ing. Christian Weigel
Dipl.-Ing. Marco Albrecht
Dipl.-Ing. Helge Drumm

Technische Realisierung (Online-Ausgabe):
Universitätsbibliothek Ilmenau
ilmedia
Postfach 10 05 65
98684 Ilmenau

Verlag:
Verlag ISLE, Betriebsstätte des ISLE e.V.
Werner-von-Siemens-Str. 16
98693 Ilrnenau

ISBN (Druckausgabe): 3-938843-15-2
ISBN (CD-Rom-Ausgabe): 3-938843-16-0

Startseite / Index:
http://www.db-thueringen.de/servlets/DocumentServlet?id=12391

51. Internationales Wissenschaftliches Kolloquium
Technische Universität Ilmenau
September 11 - 15, 2006

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Improved stability of bistable RSFQ circuitry by using Josephson junctions with intrinsic π-phase shift

INTRODUCTION

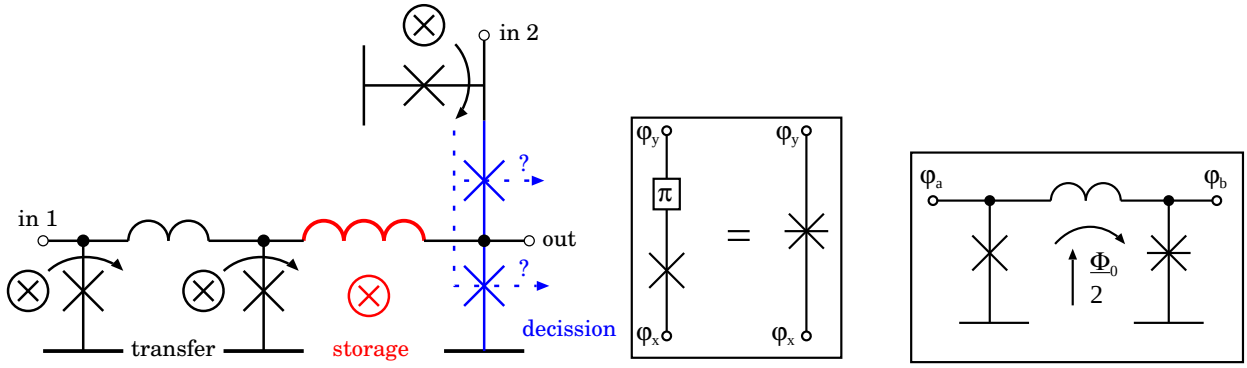
The Rapid Single Flux Quantum (RSFQ) logic is a superconducting intrinsic digital circuit technique based on the representation of information by a single quantum of magnetic flux. To define the binary data the presence or absence of such a flux quantum $\Phi_0 = h/2e$ (Planck constant h and elementary charge e) in a superconducting loop is used [1]. The switching between logical states is distinguished by a very low time constant combined with a low power consumption. Due to a simple fabrication technology and successful demonstrated circuits it is today the most promising quantum electronics [2].

There are two basic variables describing the state of a superconducting loop: the current I and the phase φ of the superconducting wave function. Usually all charge carriers in a superconducting ring can be characterized by the same wave function, but an energy barrier can be used to separate the superconductors and decouple the wave functions. Such an element creates a weak link between two superconductors and is called Josephson junction (JJ). If one connects an additional shunt resistor in parallel, the result is a nonlinear overdamped switching device, the key element of RSFQ logic [3]. This JJ acting as a kind of gate allowing the exchange of flux quanta between contiguous loops. Such a transfer is combined with a small voltage peak, called single flux quantum (SFQ) pulse with a defined area of $2,07\text{mV}\cdot\text{ps}$.

In traditional RSFQ electronics there are three degrees of freedom to adjust the behavior of a circuit: the inductance L, the critical current of a Josephson junction I_c and the bias current I_b. The combination of these elements creates three elemental structures as shown in Fig. 1a [4]. The difference between transfer and storing is determining by the normalized parameter $\beta_L = \frac{2\pi I_c L}{\Phi_0}$. The first element is used for an active transfer of SFQ pulses. It is characterized by a small loop inductance ($\beta_L < 2\pi$) usually $\beta_L = \pi$. Thereby the loop current caused by an entering SFQ pulse is clearly higher then the critical current of the JJ thus this one is switching as well and the SFQ pulse leaves the loop. When using a bigger inductance between both junctions ($\beta_L > 2\pi$), the circulating current, a result of a flux quantum inside the loop, is not strong enough to switch the second junction and a single flux quantum is stored as a representation of a binary information. That is the way to build structures with more then one stable state. The number of storable single flux quanta, thus the number of stable states, depends on β_L. To read an arbitrary information in such a loop, a decision element is needed, namely the comparator composed of two junctions. In this matter data latching is a task of most importance, because of the pulse-driven character of this electronic family. Almost every basic cell for logic operations (OR, AND,..)requires the capability of temporary data storage.

At present a new element which behaves like a JJ with an intrinsic π phase offset is available. This so called π junction was predicted long time ago. The first experimental determination was done by Wollman in 1993 [5]. The evidence was confirmed by Brawner some years later [6]. This element is distinguished by an π offset in his current-phase characteristic compared with a JJ. While a JJ can be described by:

$$I = I_c \cdot \sin(\varphi)$$



(a) (b)

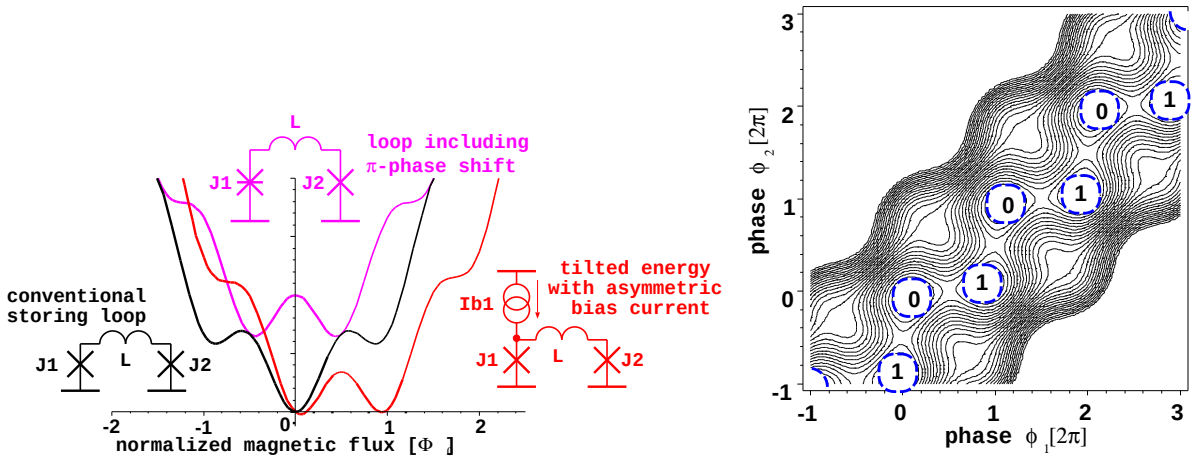
Fig. 1. a) The traditional RSFQ electronics is composed by this three elemental structures. b) The π junction as a JJ with intrinsic π phase shift and the natural behavior of an loop containing this new element.

a π junction is defined by:

$$I = I_c \cdot \sin(\varphi + \pi) = -I_c \sin(\varphi).$$

Thus the π junction can be taken as a JJ with a negative critical current corresponding to a complementary element [7]. Like the correlation of PNP and NPN transistor, the π junction does not provide a in principle new performance, rather it enables a simple and symmetrical design. This π junction is the first topological extension since the development of RSFQ electronics itself.

Supplementing a superconducting loop by an constant phase shift leads to remarkable effects. A spontaneous current is flowing in such a ring to compensate this build-in phase shift, at which both possible directions of the current appear in equal likelihood. A loop containing an inductance, a JJ and a π-junction has a build-in π-phase shift (Fig. 1b). The resulting magnetic flux coupled with the spontaneous current accumulates up to half a flux quantum in the large inductance limit [8]. The polarity of this flux can be utilized to store binary data. Such a circuit establishes a natural bistable character in contrast to a traditional RSFQ loop composed of an inductance and two junctions. This configuration is distinguished by an odd number of stable states, thus bistable behavior needs to be artifically synthesized. Therefore usually a bias current is used, which is the reason for an asymmetric design and worse parameter margins of classical RSFQ cells (Fig. 2) [9].



(a) (b)

Fig. 2. a) Potential energy U as a function of enclosed magnetic flux b) 3-D energy plot
$U = \frac{\Phi_0}{2\pi}\left\{I_{c1}(1-\cos(\varphi_1)) + I_{2c}(1-\cos(\varphi_2)) + \frac{\Phi_0}{2\pi L}(\varphi_1-\varphi_2)^2 - I_b\varphi_1\right\}$ of a bistable RSFQ device shown in Fig. 1b. In which the critical current of the π junction has a negative algebraic sign as mentioned.

DESIGN OF BASIC CELLS

A new approach for designing RSFQ circuits by utilizing build-in π phase shifts was mentioned by Ustinov, where the π junction is used as a passive phase bias and could be replaced by any other phase source [10]. In contrast our concept is to functionalize π junctions as an active JJ as well as a phase source. We intend to use the natural bistability of π loops to create more robust RSFQ devices.

To demonstrate the functionality of this idea a new cell library has to be designed. The Josephson Transmission Line (JTL) is the most simple cell of the RSFQ electronics, whose creating is the first step in a cell based design. This cell is used for an active and quantum precise transmission of SFQ-pulses, as mentioned in Fig. 1. It is a cell with only one stable state, therefore it is not appropriate for applying π junctions.

The interface between the established semiconductor technology and the new RSFQ technology is a fundamental component for experimental analysis. Converting a high energy semiconductor signal to a low energy single flux quantum is the task of the DC/SFQ converter. This cell is controlled by the input current I_{in}. While this current is zero, only the bias current provided by Ib1 is flowing through the junctions. A raising input current is split up, one part is flowing through L1 and the other part through J1 and J2 to ground. The functionality of the cell is only supported by the current flowing through the JJs, thus the value of L2 and L3 should be much smaller then L1. The superposition of input and bias current in the junctions favors the switching of J2 and handicaps the switching of J1. If the input current is high enough, J2 switches and emits a SFQ pulse. Thereby a flux quantum is extracted from the loop and the current is redistributed inside the loop changes, which induced a counter clockwise loop current. The main part of the input current in this state is flowing through L1 to ground. This state is stable as long as the input current is constant. If this one is decreased the induce loop current will become dominant and cause a switching of J1. Thereby a single flux quantum enters the loop, the induced current eliminates the loop current and the initial state is reached. To accomplish ideal margins of all parameters the equation $\Delta I_{in} \cdot L1 = \Phi_0$ should be satisfied. In that case the flux quantum, which is leaving the loop through J2, will be compensated by the magnetic flux caused by the current through the inductance L1. Thus the effective current flowing through J1 and J2 is the same in both states, as illustrated in Fig. 3a. The mentioned natural bistability of loops with one π junction is based on toggling effective current directions, therefore the DC/SFQ converter do not benefit from π junctions. Even if this device has two operation points it has only one stable state. The second operation point is only reached by adjusting the bias current. That is why this cell is designed in a traditional way, as shown in Fig. 3b [11].

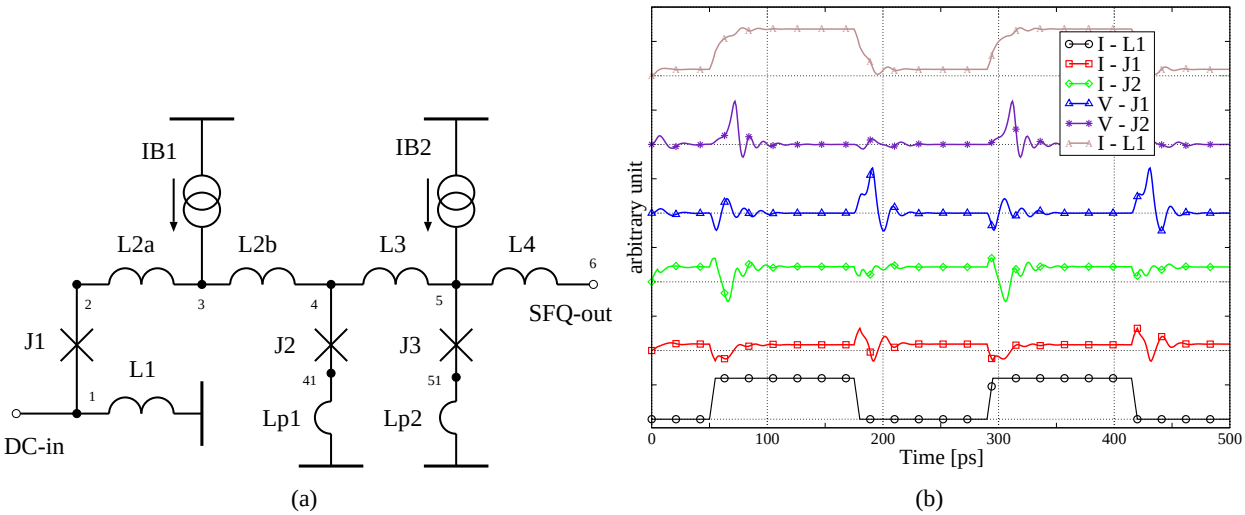


Fig. 3. a) Equivalent network of the DC/SFQ converter. b) The Simulated transient behavior of the parameter voltage (V) and current (I) of this device.

The counter part to the DC/SFQ converter is the SFQ/DC converter, it is an essential interface for detecting a single flux quantum with CMOS technology. This device is composed of a Toggle Flip Flop (TFF) and

a read-out SQUID. The TFF has two stable states characterized by two different directions of the current inside the storage inductance. In traditional RSFQ electronics this loop current is the result of an external bias source Ibgx, illustrated in Fig. 4a. An alternative approach is working without bias source, but it caused

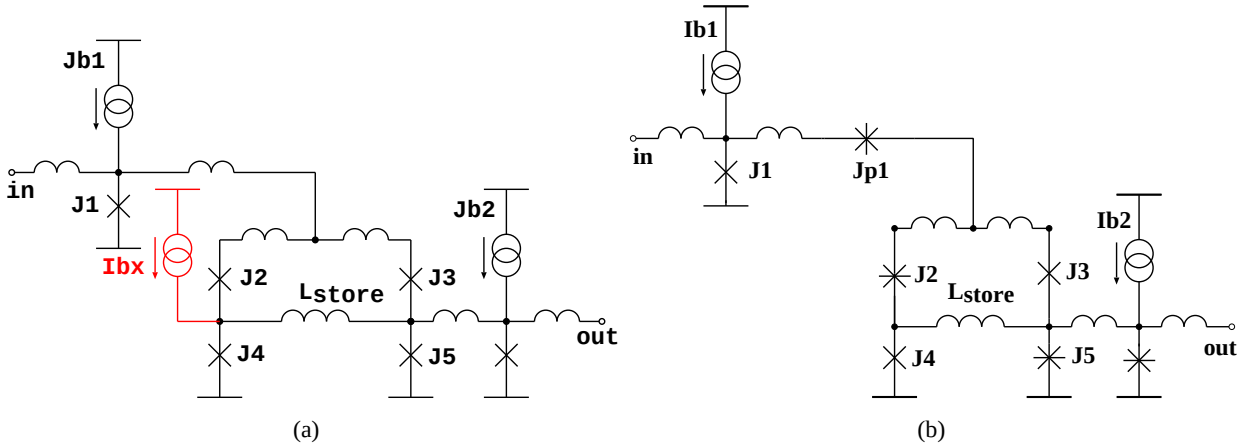


Fig. 4. Equivalent circuit of a Toggle Flip Flop with a single output: a) the current inside the storage inductance L_{store} as a result of a current source marked by the red color. b) Alternative approach: current inside the storage inductance is generated by a phase shift inside border loops caused by a combination of π junction and JJ.

an extreme assymetric topology. In experimental analysis the correct function of this circuit was observed, but the margins are low [12]. Utilizing π junctions as a phase shifter in the storing loop of a Toggle Flip Flop was proposed by Ustinov [10]. In difference to this idea the TFF shown in Fig. 4b is composed of active π junction in combination with JJ. This circuit contains two storage loops sharing the storage inductance L_{store}. The phase shift inside L_{store} causes a spontaneous current flowing stable in either clockwise and counter-clockwise direction. Let us assume the TFF is in the state with a clockwise current in the storage loop. A incoming SFQ pulse enters the cell through J1 (Fig. 5a). The associated current splits up and flows through J2 and J3 to ground. This additional current favors switching of J3 and J4 and handicaps J2 and J5 at the same time. By switching of J3 a flux quantum is extracted from the storage loop I reversing the flux state and changing the bearing of the current. When J4 is switching a positive flux quantum is pumped into loop II superposing with the initial flux $-\Phi_0/2$ to establish a new flux state $+\Phi_0/2$ Fig. (6b). Thereby a SFQ pulse is leaving the cell by outputgate 2. If a second pulse arrives at the input, J2 and J5 are favored for switching (Fig. 5b). J2 counts one flux quantum into storage loop I as shown in Fig. 5c, in doing so the initial state of this loop is established. By the switching of J5 a flux quantum is extracted from the storage loop II, thus the flux state is again $-\Phi_0/2$. As a result a SFQ pulse leaves the cell through outputgate 1 (Fig. 6c).

To create a SFQ/DC converter a dc-SQUID tapping the storage inductance of the TFF is used. The operating point of this phase sensitive sensor can be adjusted in a way that a voltage signal is created for an upward flux and no voltage for a downward flux inside the storing loops. In doing so it is possible to analyze a RSFQ circuit with standard semiconductor electronic measuring equipment.

CIRCUIT LAYOUT

There are several possibilities to establish a phase shift in a superconducting loop. For example by implementing a field bias provided by an extra control current line. This approach can be realized in traditional RSFQ technology as already implemented by Terzioglu [13]. The disadvantage of this idea is the additional bias line, which is the reason for a more complex layout and a higher power consumption. Another alternative is utilizing a frozen magnetic flux in a superconducting loop. In doing so it is possible to create an arbitrary phase shift between $\varphi = 0$ and $\varphi = \pi$ [14]. Also thinkable is a realization of grain boundary junctions with high temperature superconductors. Therefore one needs a substrate with at least three domains with different orientations. A spontaneous magnetization of $\Phi_0/2$ was observed in such a configuration,

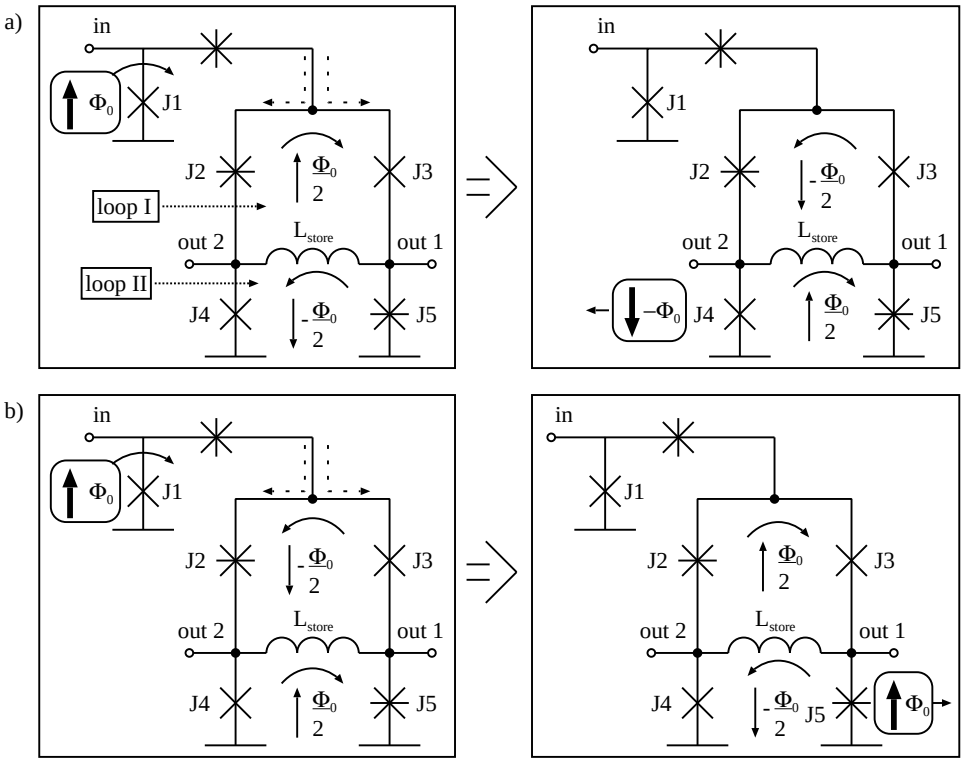


Fig. 5. Functional principle of a TFF with active π junctions. An entering single flux quantum is leaving the device through output port 1 (b) or 2 (a), depending on the internal state of the device.

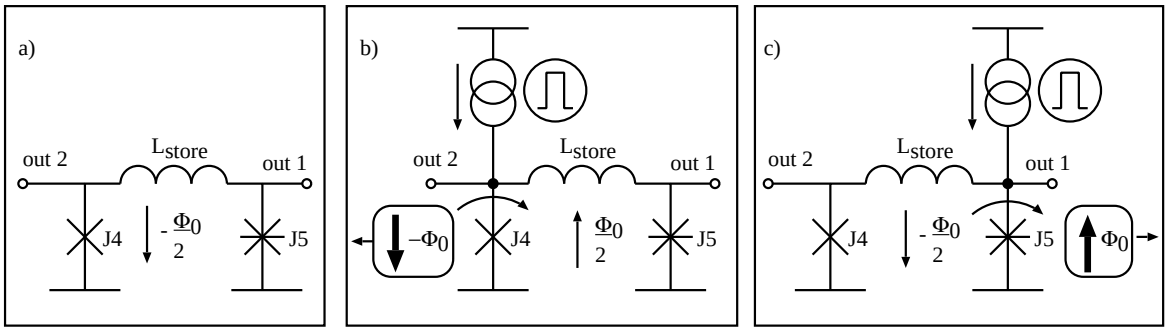


Fig. 6. a) Initial state of storage loop II of a Toggle Flip Flop. b) By switching of J4 a flux quantum is pumped into the storage loop and a SFQ pulse leaves the cell via outputgate. 2. c) By switching of J5 a flux quantum is extracted from the storage loop and a SFQ pulse leaves the cell via outputgate 1. Thus the initial state is established again.

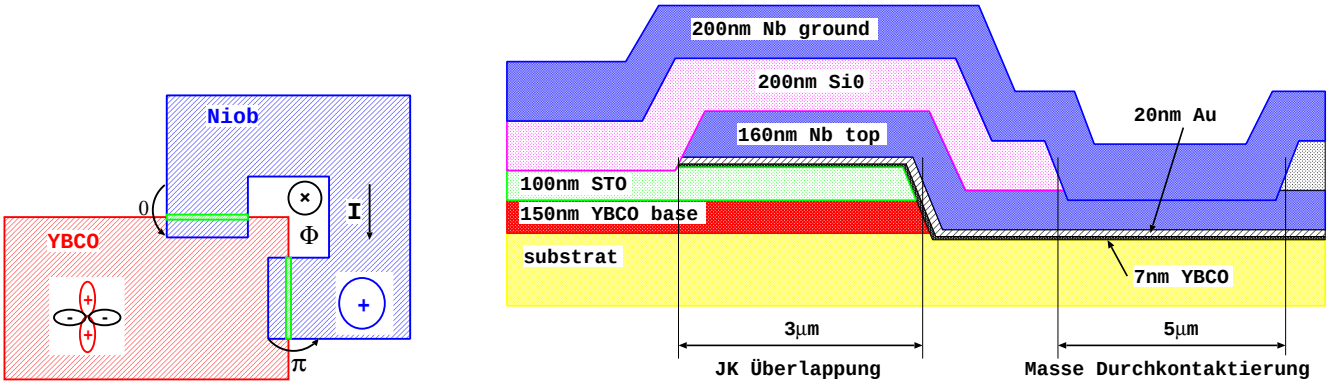


Fig. 7. a) Connecting the same YBCO area from two perpendicular directions with Nb creates a loop containing a JJ and a π junction. b) A cross section of the technology developed at the University of Twente (Netherlands).

which confirms a π phase shift [15]. The implementation of SFS junctions, which contains a ferromagnetic barrier, is today the only solution for a lumped element π junction [16].

The fabrication process we are going to use, comprises a low and a high temperature superconductor. It permits ramp-type junctions between YBCO and Nb [17]. The d-wave symmetry of YBCO enables in combination with s-wave symmetry of Nb a π phase shift generation in a two junction loop. Furthermore the technology characteristics enable RSFQ electronics. A critical current density about 20 kA/cm^2 as well as a characteristic voltage of $I_c R_N = 0,7$mV was achieved [18]. More important for a technical application is the reproducibility which was proven by the analyzing of an array with 25000 π loops [19]. At present the fabrication process of the University of Twente (Netherlands) is the only one to allow the production of RSFQ circuits with π junctions.

A π junction can be produced by connecting the same YBCO area from two perpendicular directions with niobium Fig. 7a. The created loop contains a π junction and a JJ. This feature restricts the degrees of freedom in the circuit layout. The cross section of this fabrication process is shown in Fig. 7b. Every connection between YBCO and Nb creates a junction, thus there is no way for a direct link between the YBCO layer and ground. Consequently only a even number of junctions per loop is producible.

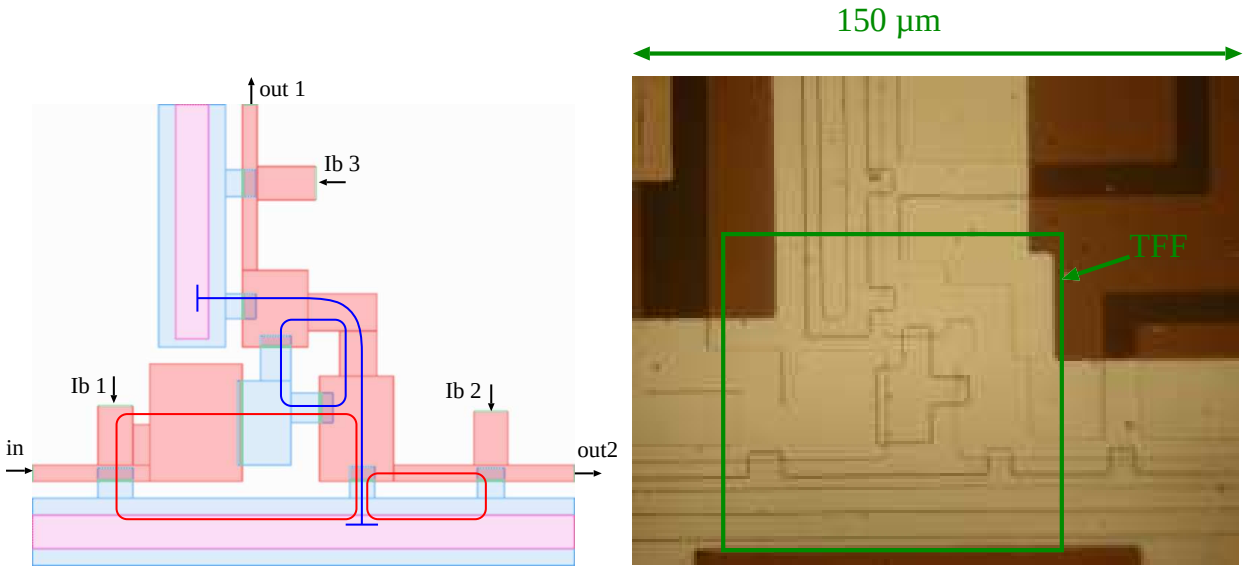


Fig. 8. Layout (a) and optical micrograph (b) of a Toggle Flip Flop with YBCO-Nb rampe-type junctions.

The layout of a TFF is displayed in Fig. 8a, where an example of loops without phase shift are marked by the red color and loops with intrinsic phase shift are marked by the blue color. There is a difference between both red loops: while loop I contains two π junctions, loop II contains no π junction. The effect in both cases is the same, no spontaneous current is flowing within these loops. Furthermore in the layout, as well as in the equivalent circuit (Fig. 4b), a parasitic junction Jp1 can be recognized, which is needless from electrical point of view . Because of the mentioned limitation to an even number of junctions per loop this parasitic junction is inevitable (Fig. 4b). It is important to ensure this junction is not switching. At Fig. 8b the photograph of a TFF covered by the ground plane is displayed. The required space of this cell is only a quarter of the standard size. This size reduction was achieved although a common feature size of $2,5\mu$m was used and the minimization was not the primary aim of the layout. It is enabled by the ramp-type technology and thus an additional advantage of this new fabrication process.

SIMULATIONS AND MEASUREMENTS

To study the influence of parameter variations on the circuit performance and to analyses the expected fabrication yield a Monte Carlo analysis was performed. Therefore several thousand Gaussian distributed parameter sets were calculated. The functionality of the π circuits by utilizing those parameters were checked by automatic circuit simulation runs. All devices containing π junction (TFF and SFQ/DC) show a strongly improved stability against possible parameter variations (Fig. 10a). Furthermore there are no disadvantages for circuits build in this technology without π junctions (DC/SFQ). The properties of those devices are the same as of standard RSFQ.

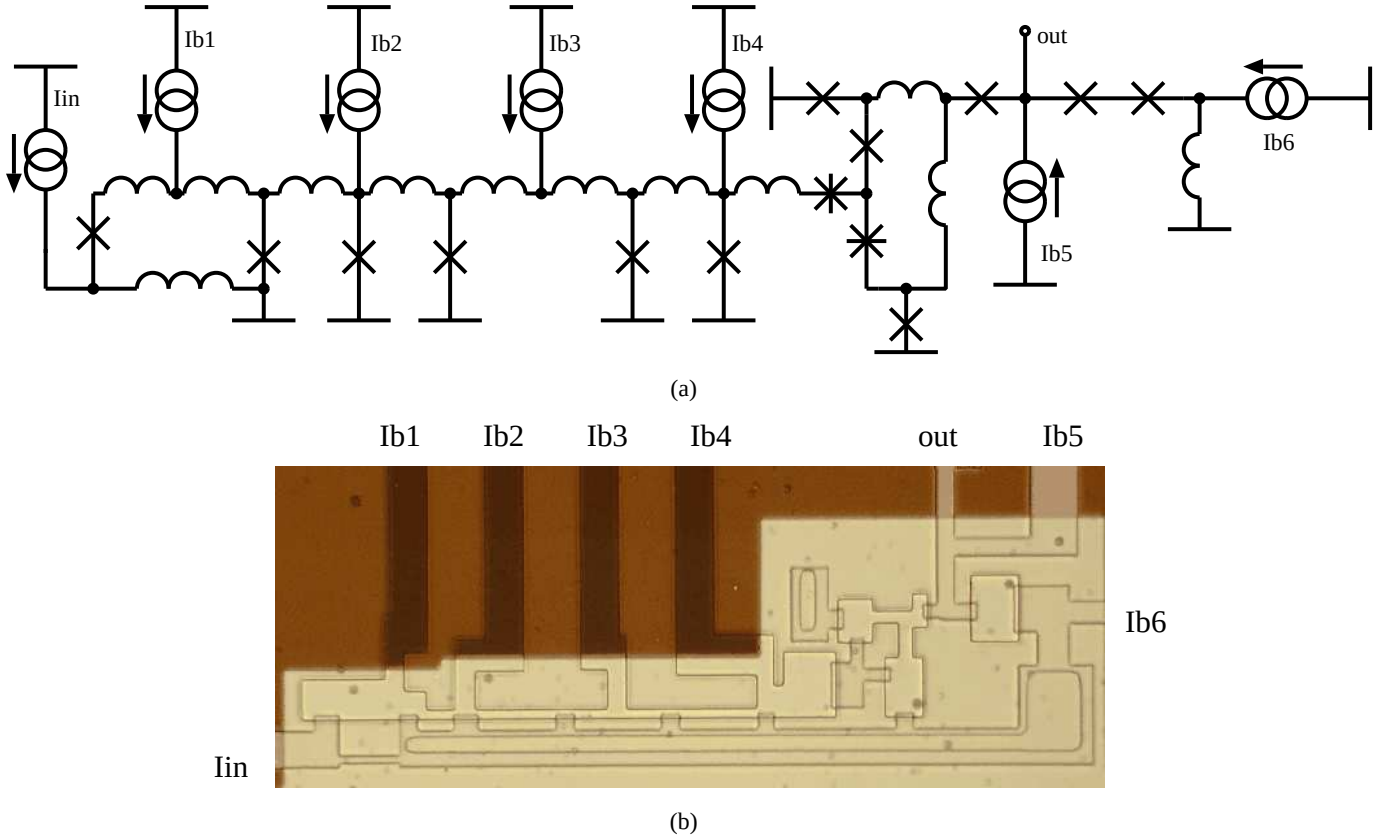


Fig. 9. The equivalent circuit (a) and the photograph (b) of the DC/DC circuit.

To prove this mentioned stability enhancement, some basic cells as well as some simple test circuits were fabricated at the University of Twente (Netherlands). For realizing RSFQ circuits the existing technology was expanded by an additional ground plane. That is necessary to create microstriplines which generate exactly defined inductances. In a further step the technology parameters were extracted. Afterwards a quantumprecise functionality test of the smallest digital circuit was performed whose optical micrograph and schematic are displayed in Fig. 9. This so called DC/DC circuit is composed of a DC/SFQ a JTL and a SFQ/DC converter. During this analyses the DC/SFQ converter is controlled by a triangular input current signal. The device is generating a SFQ pulse at every raising ramp of the input signal (Fig. 10). It is transmitted via the JTL to the SFQ/DC converter, switching the state of the comprised TFF. Thus output voltage over the read-out SQUID has to be changed as well. Figure 11a shows the triangular input signal and the output voltage clearly demonstrating the toggling of the TFF at every raising ramp. Several experiments were accomplished confirming the correct operation of the electronics. One of which is shown in Fig. 11b. The amplitude of the input signal is gained, so that three flux quanta are generated per raising ramp. Thereby the output state is changed three times as well.

The maximum output voltage of the mentioned SFQ/DC converter is half of the characteristic voltage

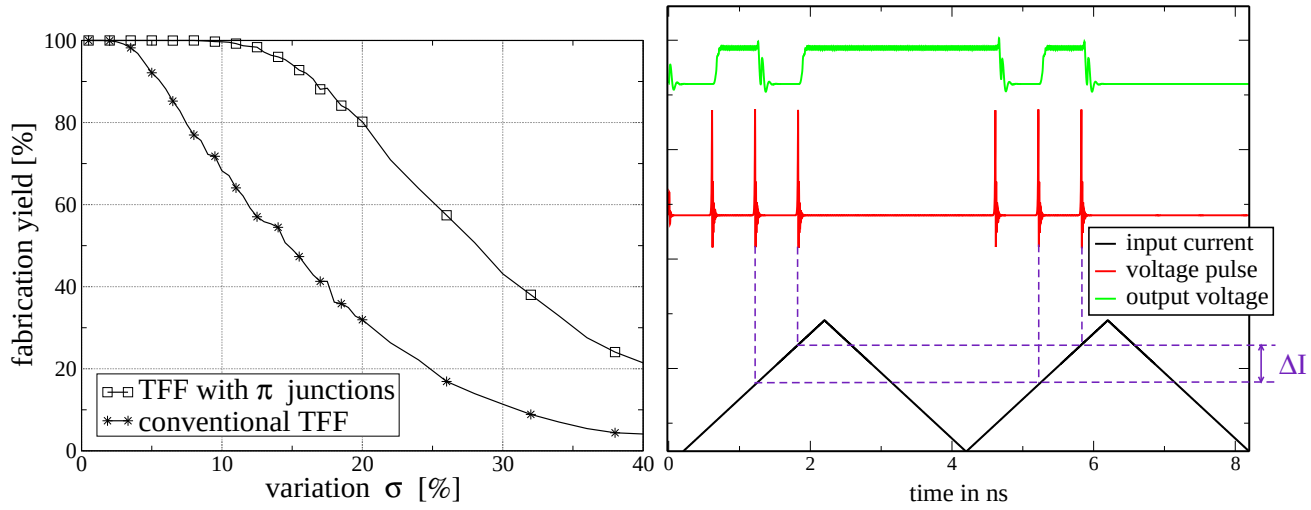


Fig. 10. a) Diagram of the expected fabrication yield of a standard Toggle Flip Flop. b) The simulated transient behaviour of a DC/DC circuit which is generating a single flux quantum every $\Delta I_{in} = \Phi_0/L1$ at the raising input current edge. The voltage pluse which is coupled with the singel flux quantum is shown. The toogle of the voltage ouptut state can be recognized as well.

I_cR_N, which depends on the technology parameters. In this first sample the characteristic voltage is $I_cR_N = 150\mu$V, that is why the output voltage is $U = 55\mu$V. Nevertheless values up to $I_cR_N = 0,7$mV have been shown by analysing a similar fabrication process [18]. The voltage corresponds with a maximum frequency of $f = 340$ GHz, which matches with other standard RSFQ technologies.

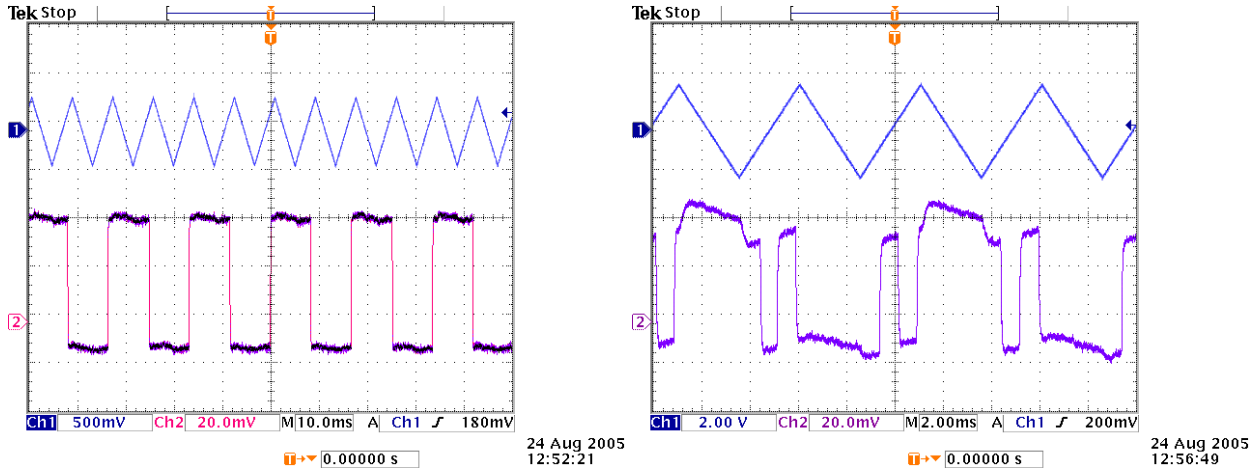


Fig. 11. Measurement results of a DC/DC circuit using triangular input signal with different amplitudes and detecting the rectangular output signal.

The theoretically predicted stability against parameter variations was also observed in experimental analyses. Even for this first sample with partial heavy parameter variations the correct operation was shown for a wide temperature range between 5,3K and 5,8 K. The bias current Ib4 (Fig. 9) of the TFF can be varied between $\pm 18\%$ without losing the functionality. With an improved fabrication process it can be expected to realize margins of $\pm 55\%$ for the bias current, as the parameter analyses by simulations calculated.

CONCLUSION

We present the first RSFQ electronics utilizing active switching π junctions in combination with Josephson junctions. This enables a more simple and symmetrical circuit design then standard RSFQ electronics. Thereby a strongly improved stability against parameter variations, which was confirmed by various parameter analyses, is achieved. This first implementation of an RSFQ circuits with HTS - TTS ramp-type junctions is characterized by low required space. Our TFF needs only a quarter of the area of a standard TFF realization with the same feature size. A correct quantumprecise digital operation in a wide temperature-range between 5,3K and 5,8K was observed by experimental analysis.

References

[1] K.K. Likharev and V.K. Semenov, "RSFQ logic/memory family: A new Josephson junction technology for sub-terahertz-clock-frequenzy digital systems," *IEEE Trans. Appl. Superconductivity*, vol. 1, no. 1, pp. 3–27, 1991.

[2] Semiconductor Industry Association, "International Technology Roadmap for Semiconductors," http://www.itrs.net/Common/2004Update/2004_05_ERD.pdf, 2004.

[3] V.K. Kaplunenko, M.I. Khabipov, K.K. Likharev, et al., "Experimental study of the RSFQ logic elements," *IEEE Trans. on Magnetics*, vol. 25, no. 2, pp. 861–864, 1989.

[4] D.K. Brock, E.K. Track, and J.M. Rowell, "Superconductor ICs: the 100-GHz second generation," *IEEE Spectrum*, vol. 37, no. 12, pp. 40–46, 2000.

[5] D.A. Wollmann, D.J. Van Harlingen, W.C. Lee, D.M. Ginsberg, and A.J. Leggett, "Experimental determination of the superconducting pairing state in YBCO from the phase coherence of YBCO-Pb dc SQUIDs," *Physical Review Letters*, vol. 71, no. 13, pp. 2134–2137, 1993.

[6] D.A. Brawner and H.R. Ott, "Evidence for a non-s-wave superconducting order parameter in $YBa_2Cu_3O_{6.6}$ with T_c=60K," *Physical Review B*, vol. 53, no. 13, pp. 8249–8252, 1996.

[7] E. Terzioglu and M.R. Beasley, "Complementary Josephson junction devices and circuits: A possible new approach to superconducting electronics," *IEEE Trans. Appl. Superconductivity*, vol. 8, no. 2, pp. 48–53, 1998.

[8] J.R. Kirtley, K.A. Moler, and D.J. Scalapino, "Spontaneous flux and magnetic-interference patterns in 0-π Josephson junctions," *Physical Review B*, vol. 56, no. 2, pp. 886–891, 1997.

[9] T. Ortlepp, Ariando, O. Mielke, C.J.M. Verwijs, K.F.K. Foo, H. Rogalla, F.H. Uhlmann, and H. Hilgenkamp, "Flip-Flopping fractional flux quanta," *Science*, vol. 312, pp. 1495–1497, 2006.

[10] A.V. Ustinov and V.K. Kaplunenko, "Rapid single-flux quantum logic using π-shifters," *Journal of Applied Physics*, vol. 94, no. 8, pp. 5405–5407, 2003.

[11] TU-Ilmenau RSFQ design group, "RSFQ cell library," Fluxonics, http://www4.tu-ilmenau.de/EI/ATE/kryo/cell_library/index.htm, 2006.

[12] S.V. Polonsky, V.K. Semenov, P.I. Bunyk, A.F. Kirichenko, A.Yu. Kidiyarova-Shevchenko, O.A. Mukhanov, P.N. Shevchenko, D.F. Schneider, D.Yu. Zinoviev, and K.K. Likharev, "New RSFQ circuits," *IEEE Trans. Appl. Superconductivity*, vol. 3, no. 1, pp. 2566–2577, 1993.

[13] E. Terzioglu, D. Gupta, and M.R. Beasley, "Complementary Josephson junction circuits," *IEEE Trans. Appl. Superconductivity*, vol. 7, no. 2, pp. 3642–3645, 1997.

[14] J.B. Majer, J.R. Butcher, and J.E. Mooij, "Simple phase bias for superconducting circuits," *Applied Physics Letters*, vol. 80, no. 19, pp. 3638–3640, 2002.

[15] C.C. Tsuei, J.R. Kirtley, C.C. Chi, A. Gupta, T. Shaw, J.Z. Sun, and M.B. Ketchen, "Pairing symmetry and flux quantization in a tricrystal superconducting ring of $YBa_2Cu_3O_{7-\delta}$," *Physical Review Letters*, vol. 73, no. 4, pp. 593–596, 1994.

[16] V.V. Ryazanov, V.A. Oboznov, A.Yu. Rusanov, A.V. Veretennikov, A.A. Golubov, and J. Aarts, "Coupling of two superconductors through a ferromagnet: Evidence for a π junction," *Physical Review Letters*, vol. 86, no. 11, pp. 2427–2430, 2001.

[17] H.J.H Smilde, H. Hilgenkamp, G.J. Gerritsma, D.H.A. Blank, and H. Rogalla, "Realization and properties of ramp-type $YBa_2Cu_3O_{7-\delta}$/Au/Nb junctions," *Physica C*, vol. 350, pp. 269–275, 2001.

[18] H.J.H Smilde, H. Hilgenkamp, G. Rijnders, D.H.A. Blank, and H. Rogalla, "Enhanced transparency ramp-type Josephson contacts through interlayer deposition," *Applied Physics Letters*, vol. 80, no. 24, pp. 4579–4581, 2002.

[19] H. Hilgenkamp, Ariando, H.J.H Smilde, D.H.A. Blank, G. Rijnders, H. Rogalla, J.R. Kirtley, and C.C. Tsuei, "Ordering and manipulation of the magnetic moments in large-scale superconducting π-loop arrays," *Nature*, vol. 422, pp. 50–53, 2003.

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