



**FACULTY OF ELECTRICAL ENGINEERING
AND INFORMATION SCIENCE**



**INFORMATION TECHNOLOGY AND
ELECTRICAL ENGINEERING -
DEVICES AND SYSTEMS,
MATERIALS AND TECHNOLOGIES
FOR THE FUTURE**

Startseite / Index:

<http://www.db-thueringen.de/servlets/DocumentServlet?id=12391>

Impressum

Herausgeber: Der Rektor der Technischen Universität Ilmenau
Univ.-Prof. Dr. rer. nat. habil. Peter Scharff

Redaktion: Referat Marketing und Studentische
Angelegenheiten
Andrea Schneider

Fakultät für Elektrotechnik und Informationstechnik
Susanne Jakob
Dipl.-Ing. Helge Drumm

Redaktionsschluss: 07. Juli 2006

Technische Realisierung (CD-Rom-Ausgabe):
Institut für Medientechnik an der TU Ilmenau
Dipl.-Ing. Christian Weigel
Dipl.-Ing. Marco Albrecht
Dipl.-Ing. Helge Drumm

Technische Realisierung (Online-Ausgabe):
Universitätsbibliothek Ilmenau
[ilmedia](#)
Postfach 10 05 65
98684 Ilmenau

Verlag:  Verlag ISLE, Betriebsstätte des ISLE e.V.
Werner-von-Siemens-Str. 16
98693 Ilmenau

© Technische Universität Ilmenau (Thür.) 2006

Diese Publikationen und alle in ihr enthaltenen Beiträge und Abbildungen sind urheberrechtlich geschützt. Mit Ausnahme der gesetzlich zugelassenen Fälle ist eine Verwertung ohne Einwilligung der Redaktion strafbar.

ISBN (Druckausgabe): 3-938843-15-2
ISBN (CD-Rom-Ausgabe): 3-938843-16-0

Startseite / Index:
<http://www.db-thueringen.de/servlets/DocumentServlet?id=12391>

Th. Ortlepp, F. H. Uhlmann

Gate Delay Jitter in Superconductor Electronics

INTRODUCTION

Rapid Single Flux Quantum (RSFQ) logic is a superconductive digital circuit technique, in which the data are represented by the presence or absence of a flux quantum $\Phi_0 = h/2e$ (Plancks constant h and elementary charge e) in a cell, which is generated of Josephson junctions and inductances. The quantum mechanical phase difference over each junction defines the internal state in these circuits. The switching of RSFQ logic circuits between logical states is characterized by very high speed as well as low energy consumption [1].

All complex devices in rapid single flux quantum (RSFQ) technique work at much lower clock rates than possible for simple cells. New data driven self timed or asynchronous concepts can reduce this gap, but even in this case a discrepancy between simulation and experiment is still present. We address the complete simulation and optimization cycle for the development of logic cells. We start analyzing a Josephson transmission line (JTL) as the origin for RSFQ circuit design.

The step from the level logic semiconductor circuits to the pulse logic RSFQ is accompanied by a new kind of transient analysis in the system design. We can see a clear gap between the maximum operation frequencies of simple logic cells and than for complex devices which are about one order of magnitude. Already [2] reflects the timing jitter as the most limiting factor for large-scale RSFQ digital systems.

It has been pointed out in previous studies, that the influence of thermal fluctuations in RSFQ circuits is divided into static and dynamic switching bit errors as well as timing jitter induced failures. Our last results show for the first time, that the variance of the switching time is much slower decreased by reducing the temperature and is still important at 4.2 K. The delay between output signal and the input signals for typical RSFQ cells shows a variation over 1 ps which is more than 10% of the switching time itself. We combine in our investigations the switching time variations caused by thermal noise and by technology related parameter spread.

PULSE PROPAGATION IN A JOSEPHSON TRANSMISSION LINE

The parameter set for a Josephson Transmission Line (JTL) serves as a base for designing RSFQ logic cells. We set first the critical current of the Josephson junction to a certain value, e.g. $I_c = 250\mu A$. Its value should not be too small to obtain a high stability against thermal noise due to a high Josephson coupling energy [3]. On the other hand, smallest possible inductance value L for a superconducting loop gives an upper bound for the critical current. The model for the JTL used in this work is shown in Figure 1(a). If we assume a complete switching of the first junction J_1 , it generates a driving current through the inductance of $I_L \approx \frac{\Phi_0}{L_2+L_3}$. If this current is larger than the critical current of the second junction, it will switch and therefore increase its phase difference by 2π . With the bias level of $I_b = 0.75 \cdot I_c = 187.5\mu A$, this results in an optimal loop inductance of $L^* = 3.979\text{pH}$ [4]. Figure 1(b) shows a realization of the cell in the Niobium tri-layer technology of IPHT Jena [5]. The bias current source is build with a constant voltage source of 2.5mV and a resistor.

The transmission of SFQ-pulses is the most simple, but essential part of RSFQ circuits. It is the typical interconnect between logic cells and its operation as an active pulse repeater improves the pulse shape as

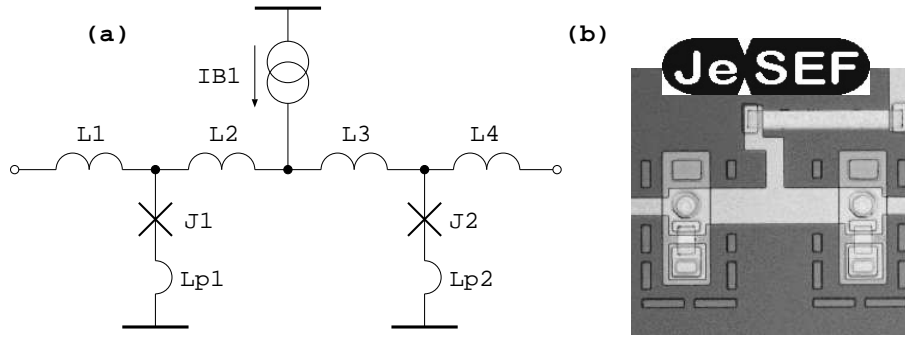


Fig. 1. The JTL circuit model (a) and the photograph of the fabricated structure (b) with parameters as used for the simulations (critical currents: $J_1=J_2=250 \mu\text{A}$; inductances: $L_1=L_2=L_3=L_4=1.85\text{pH}$, $L_{p1}=L_{p2}=0.15\text{pH}$; bias current: $I_{B1}=375 \mu\text{A}$).

well as reduces the undesired interaction between adjacent cells. For an theoretical analysis of a JTL, we assume all junctions and all loops with equal parameters and neglect the junction capacitance. According to Fig. 2, this results for a n-stage JTL in a system of n nonlinear differential state variable equations

$$\begin{aligned} \frac{\Phi_0}{2\pi R_n} \dot{x}_1 &= I_b - I_c \sin(x_1) - \frac{\Phi_0}{2\pi L}(x_1 - x_2), \\ \frac{\Phi_0}{2\pi R_n} \dot{x}_k &= I_b - I_c \sin(x_k) + \frac{\Phi_0}{2\pi L}(x_{k-1} - x_k) - \frac{\Phi_0}{2\pi L}(x_k - x_{k+1}), \quad k = 2..n - 1, \\ \frac{\Phi_0}{2\pi R_n} \dot{x}_n &= I_b - I_c \sin(x_n) + \frac{\Phi_0}{2\pi L}(x_{n-1} - x_n) \end{aligned} \quad (1)$$

with the quantum mechanical phase difference x_k across the Josephson-junction J_k .

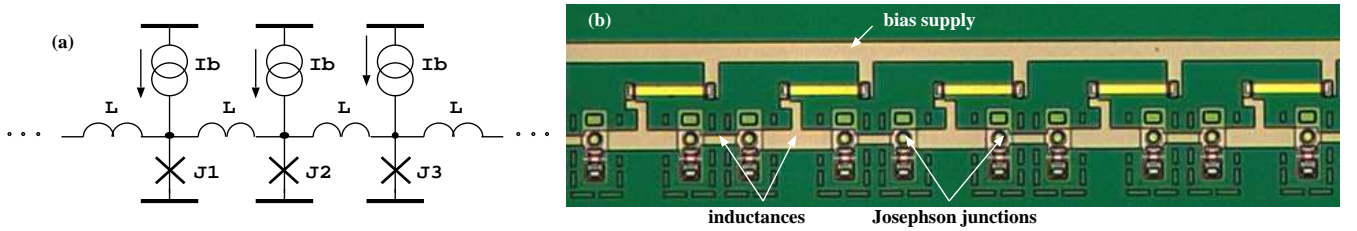


Fig. 2. Model for the theoretical analysis with separated current sources for each junction (a) and the realization of a long JTL in three layer niobium technology (b), fabricated at IPHT Jena, Germany.

The potential energy for all circuit elements allows the straight forward construction of the total potential energy of a logic cell. If the capacitance of the junction C_J or parasitic dynamic elements should be included in the analysis, this energy includes additional terms. In equivalence to the derivation of the equations of motion for the principle of minimal action, we can derive the system differential equation for the JTL from its potential energy. In comparison to the node voltage in classical circuits, we can define a phase value for each node in a superconducting circuit. The common ground phase reference is set to be zero. For Josephson junctions and inductances the phase difference $x_1 - x_2$ between the terminals is used. Due to the connection of all current sources to ground, we need only one phase value x for the potential energy of a source. The energy terms for all circuit elements are shown in Table I.


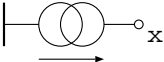

circuit component	scheme	energy term
Josephson-junction		$\frac{\Phi_0 I_c}{2\pi} (1 - \cos(x_1 - x_2))$
current source		$-\frac{\Phi_0 I_b}{2\pi} x$
inductance		$\frac{\Phi_0^2}{4\pi^2 L} (x_1 - x_2)^2$

TABLE I

INHERENT ENERGY OF CIRCUIT ELEMENTS DEPENDING ON THE PHASE DIFFERENCE BETWEEN NODES.

If we sum all energy terms for the transmission line model, we end up with

$$E(\underline{x}) = I_c \left(n - \sum_{k=1}^n \cos(x_k) \right) - I_b \sum_{k=1}^n x_k + \frac{\Phi_0}{4\pi L} \sum_{k=1}^{n-1} (x_k - x_{k+1})^2. \quad (2)$$

This equation can be interpreted as a first integral of the system of differential equations (1) and between this equations the potential energy $E(x_1, x_2)$ holds the simple equation

$$\frac{\Phi_0}{2\pi R_n} \frac{\partial}{\partial t} \begin{pmatrix} x_1 \\ x_2 \\ \dots \\ x_n \end{pmatrix} = -\text{grad}(E(x_1, x_2, \dots, x_n)). \quad (3)$$

The state of the system is defined by the state vector $\underline{x} = (x_1, x_2, \dots, x_n)$. A stable state of the system is characterized by vanishing time derivations $\dot{x}_k \stackrel{!}{=} 0$. On the other hand, this is a necessary condition for a minimum of the system energy

$$\frac{\Phi_0}{2\pi R_n} \dot{x}_k = -\frac{\partial E}{\partial x_k}. \quad (4)$$

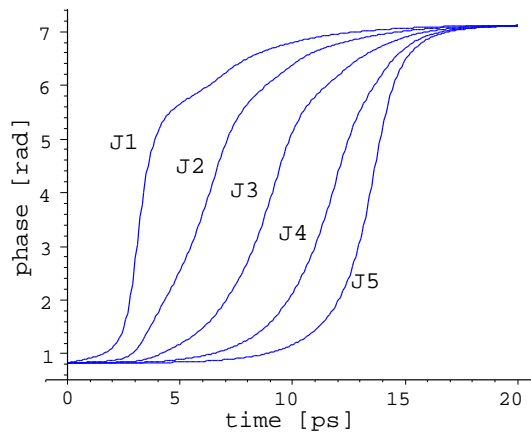


Fig. 3. Phase values x_k of a 5-stage JTL for a forced switching of $J1$.

Figure 3 shows the result of a numerical simulation of a 5-stage JTL. An artificial source forces the first junction to switch and starts the transmission of a SFQ pulse. The other junctions start to switch one by one

with a certain time delay. Due to the open end of the circuit, we generate a mismatch resulting in a modified switching of the last two junctions. If we would increase the number of junctions in the simulations, all inner junctions will behave like $J3$. The differential equation for stage k in Eq.(1) can be written as

$$\frac{\Phi_0}{2\pi R_n} \dot{x}_k = I_b - I_c \sin(x_k) + \frac{\Phi_0}{2\pi L} (x_{k-1} - 2x_k + x_{k+1}). \quad (5)$$

If we assume the position k of a certain junction in the JTL as a discretization in space, we can write this equation as

$$\frac{\Phi_0}{2\pi R'_n} \frac{\partial x}{\partial t} = I'_b - I'_c \sin(x) + \frac{\Phi_0}{2\pi L'} \frac{\partial^2 x}{\partial z^2} \quad (6)$$

for the space dependent phase $x(z, t)$. In the case, we can interpret z as the position in space of a junction in a straight long JTL. By using a step size h_z , we can write all corresponding circuit parameters as

$$L = L' h_z, \quad I_c = I'_c h_z, \quad I_b = I'_b h_z, \quad R_n = \frac{R'_n}{h_z}. \quad (7)$$

Finally, we get with function $f(x) = \frac{2\pi}{\Phi_0} (I'_b - I'_c \sin(x))$ the partial differential equation

$$\frac{1}{R'_n} \frac{\partial x}{\partial t} = f(x) + \frac{1}{L'} \frac{\partial^2 x}{\partial z^2}. \quad (8)$$

If we would like to use the junction capacitance $C_J = C'_J h_z$ in this approach, one can derive a similar equation with the first and second time derivation

$$C'_J \frac{\partial^2 x}{\partial t^2} + \frac{1}{R'_n} \frac{\partial x}{\partial t} = f(x) + \frac{1}{L'} \frac{\partial^2 x}{\partial z^2}. \quad (9)$$

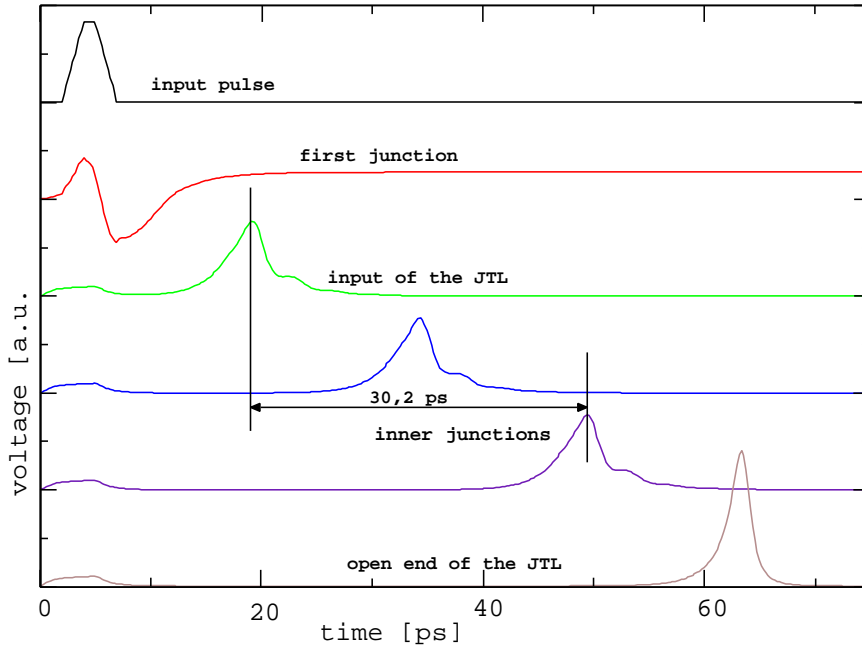


Fig. 4. Pulse propagation on a JTL with 30 junctions. The measured value of 30.2ps corresponds to the 10 junctions in the middle. parameters are $L = 3.5$ pH, $R_n = 1.5$ Ω , $I_c = 200$ μ A and $I_b = 140$ μ A with a switching time of $t_s = 3.02$ ps.

For all kind of digital circuits, so called short Josephson-junctions are used, where the variation of the phase versus space can be neglected. From the theory point of view, the third Josephson-equation describes

the influence of a magnetic field \vec{B} and the phase difference x across a junction as

$$\text{grad}(x) = \frac{2\pi}{\Phi_0}(\vec{B} \times \vec{e}_z)(2\lambda_L + d) \quad (10)$$

with the London penetration depth λ_L and the effective thickness of the insulating barrier d between the superconductors. The transition from Eq.(1) to Eq.(8) is equivalent to the transition from a discrete coupling of an infinite number of separated junctions to a continuous distributed long junction. Therefore, this kind of partial differential equation has been analyzed in the past [6, 7] and the results can be translated to the dynamic behavior of a JTL as a discrete form of a long Josephson-junction.

We replace the first junction by a driving phase source, acting as a hard source for the input signal $x_1(t)$. The shape of the 2π -phase transition is changed, if the second junction repeats the pulse to $x_2(t)$ and so on. If we use this as a new input signal for the next junction, we generate an iteration process without feedback to the source.

$$\frac{\Phi_0}{2\pi R_n} \dot{x}_k = I_b - I_c \sin(x_k) + \frac{\Phi_0}{2\pi L} (x_{k-1} - x_k). \quad (11)$$

If we can observe a switching process inside a long JTL, the only difference between both curves is a certain time delay. A normalization in time $\frac{\Phi_0}{2\pi I_c R_n} \tau = t$ and inductance $\beta_L = \frac{2\pi I_c L}{\Phi_0}$ reduces this equation to

$$x'_k = \frac{I_b}{I_c} - \sin(x_k) + \frac{1}{\beta_L} (x_{k-1} - x_k). \quad (12)$$

The inductance has to fulfill $L < \frac{\Phi_0}{I_c - I_b}$, to avoid a trapping of the magnetic flux quantum inside the loop. This corresponds to $\beta_L < \frac{1-i}{2\pi}$ for the normalized equation. The time and space dependent phase $x(z, t)$ can be expressed as

$$\frac{\partial x}{\partial \tau} = \frac{I_b}{I_c} - \sin(x) + \frac{1}{\beta_L} \frac{\partial x}{\partial z} \quad (13)$$

with a space step of $\Delta z = 1$. For a bias current $0 < i < 1$ exists an analytical solution

$$x(z, \tau) = 2 \arctan \left\{ \frac{1}{i} - \frac{\sqrt{1-i^2}}{i} \tanh \left(\frac{\sqrt{1-i^2}}{2} \beta_L [z + F_1(\tau - z\beta_L)] \right) \right\}. \quad (14)$$

with an arbitrary function F_1 . The shape of this function is defined by the initial driving pulse shape and the argument $\tau - z\beta_L$ is typical of the propagation of waves. If we use $x(0, \tau) = \arcsin(i)$ as an initial condition, we obtain $F_1 = \infty$ and furthermore $\tanh(\infty) = 1$. The final solution of the phase transition inside a long JTL results as

$$x(z, t) = 2 \arctan \left\{ \frac{1 - \sqrt{1-i^2}}{i} \right\} = \arcsin(i). \quad (15)$$

All junctions will have for all time the initial phase value. This is the static solution for a JTL without a propagation pulse.

If the function F_1 has any finite value, the limit for $z \rightarrow \infty$ results also in this static solution. In that case, we have a small relaxation phase of the JTL as reaction of an external current pulse, but too weak for a switching event.

Only an infinite value of F_1 results in a switching event. If we use $x_0 = x(0, \tau) = \arcsin(i) + 2\pi h(\tau)$ as an initial switching event with the unit step function $h(\tau)$, we can derive the function F_1 to be

$$F_1(\tau) = \frac{2}{\beta_L \sqrt{1-i^2}} \text{arctanh} \left\{ \frac{1 - i \tan \left(\frac{1}{2} \arcsin(i) + \pi h(\tau) \right)}{\sqrt{1-i^2}} \right\}, \quad (16)$$

with the conditions

$$\lim_{t \rightarrow 0-0} F_1(\tau) = -\infty, \quad \lim_{t \rightarrow 0+0} F_1(\tau) = \infty. \quad (17)$$

This results finally in a non-stationary solution and the position of switching

$$z_s = \frac{\tau}{\beta_L} \quad \text{i.e.} \quad z_s = \frac{\Phi_0}{2\pi I_c L} \frac{2\pi I_c R_n}{\Phi_0} t = \frac{R_n}{L} t \quad (18)$$

moves in time with a speed of $1/\beta_L$. The time delay between two junctions can be derived, if we increase the index k by one. This is equal to an increasing in space z_s by one. The switching time of a single stage in the JTL is simply

$$t_s = \frac{L}{R_n} \quad (19)$$

defined by the time constant of the R_n - L element.

If we extend this consideration on an infinite long chain of loops, the analytical solution for the switching time in Eq.(8) can be derived with a computer algebra system [8] to be

$$t_s = \frac{R_n}{\Phi_0} \left(\frac{I_b}{I_c} \right)^{3/2} \sqrt{\left(I_b - \frac{\Phi_0^2}{L} \right)^2 - I_c^2}. \quad (20)$$

The structure of this result is similar the the time constant in of the ac-solution for a Josephson-junction

$$f_J = \frac{\langle v(t) \rangle}{\Phi_0} = \frac{R_n \sqrt{I_{ges}^2 - I_c^2}}{\Phi_0}. \quad (21)$$

in the voltage state. Table II shows different simulation results and their comparison to values form Eq.(20).

L	R_n	I_c	I_b	t_s^{sim}	t_s/t_s^{sim}
3,5	1,5	200	140	3,02	1,109
3,5	1,2	200	140	3,74	1,119
3,0	1,5	200	140	2,64	1,108
4,0	1,5	200	140	3,30	1,140
4,0	1,5	200	160	2,72	1,095
4,0	1,5	200	173	2,40	1,081

TABLE II

SIMULATION AND CALCULATION OF TIME DELAY FOR DIFFERENT PARAMETER SETS OF A JTL

We find a fixed factor of 1.1 in all cases and the dependence from the bias current is similar in theory and simulation. On this base, we can validate this method to be in good agreement with the simulation results. We are mainly interested in the variations of switching time depending on random influences to each single Josephson junction. Therefore, we have to extend this method by adding noise sources in all differential equations.

NOISE INDUCED TIMING JITTER IN A JTL

The Johnson/Nyquist noise in the shunt resistor of an overdamped Josephson junction is the dominant noise source for RSFQ logic circuits. We study only the transfer of one single SFQ pulse along the JTL. The transient behavior of phase x and voltage v of a junction in the middle of a JTL can be described with the RCSJ-model given in Eq. (22). The junction capacitance C_J and the normal resistor R_n are determined by

the typical process parameter $I_c R_n = 256 \mu\text{V}$ and damping with McCumber-parameter $\beta_c = \frac{2\pi I_c R_n^2 C_J}{\Phi_0}$ equal to unity.

$$\dot{x} = \frac{2\pi}{\Phi_0} v, \quad C_J \dot{v} = I_b - I_c \sin(x) - \frac{v}{R_n} + \frac{\Phi_0(x_1 - 2x + x_3)}{2\pi L} + I_n(t) \quad (22)$$

The left and right neighbor junctions have the phases x_1 and x_3 , respectively. Their behavior can be described by the same set of differential equations. The thermal noise of the resistor R_n is modeled by a normal distributed noise current source $I_n(t)$ with mean value zero and a variance of

$$s = \langle I(t)I(t') \rangle = \frac{2k_B T}{R_n}. \quad (23)$$

The thermal activation energy is expressed as the product of the Boltzmann constant k_B and the temperature T . The numerical analysis is simplified using a normalized time using the characteristic frequency ω_c and the voltage v is replaced by the normalized voltage u in units of the characteristic voltage $I_c R_n$.

$$\begin{aligned} \beta_c &= \frac{2\pi I_c R_n^2 C_J}{\Phi_0} & \tau &= \frac{2\pi I_c R_n}{\Phi_0} t = \omega_c t \\ \beta_L &= \frac{2\pi I_c L}{\Phi_0} & u &= \frac{v}{I_c R_n} \end{aligned} \quad (24)$$

The set of differential equations in Eq.(25) is the result of this normalizations (Eq.(24)) and setting the McCumber Parameter β_c equal to unity.

$$\begin{aligned} \frac{dx}{d\tau} &= u \\ \frac{du}{d\tau} &= i - \sin(x) - u + \frac{1}{\beta_L}(x_0 - 2x + x_2) \end{aligned} \quad (25)$$

This system of stochastic differential equations can be translated in a corresponding Fokker Planck equation for the probability density $W(x, u, \tau)$ given by Eq.(26).

$$\frac{\partial W}{\partial \tau} = W - \frac{\partial W}{\partial u} \left(i - \sin(x) - u + \frac{x_0 - 2x + x_2}{\beta_L} \right) - u \cdot \frac{\partial W}{\partial x} + \frac{s_n}{2} \frac{\partial^2 W}{\partial u^2}. \quad (26)$$

We derive the distribution of the normalized noise current s_n to be $\frac{4k_B T}{\beta_c^2 \Phi_0 I_c}$. The stable solution before arriving of a SFQ pulse is approximately given as a two-dimensional Gaussian distribution of voltage and phase in the state space with a mean value of $u = 0$ and $x = \arcsin(I_b/I_c)$. We use this as an initial condition for a numerical finite differences time domain solution of the partial differential equation. The strong coupling of the junctions in connection with the low temperature of 4.2K is resulting in a heavy concentrated probability distribution, which is a challenge for the numerical solution. The later studied cells with much larger thermal noise influence are numerically much easier to handle. That is the reason, that up to now, we can only show a few results for the jitter analysis of a JTL.

We calculated a timing jitter of about $\sigma=0.12\text{ps}$ for one Josephson junction with parameters mentioned above at 4.2 Kelvin. The measurement of the cycling period for a long circular transmission line reports a timing jitter of $\sigma = 0.2\text{ps}$ for a bias level (ratio I_b/I_c) of 0.7 [9]. Also [10] reports the same high value measured on a different circuit, but with a comment about apparent problems with the external rf-shielding of the testing setup. The noise simulation carried out in [11] reports a value of $\sigma = 0.08\text{ps}$ for a bias level of 0.7. A recent extensive experimental study clearly shows the decreasing of pulse jitter in a JTL by increasing the bias level [12]. Both experiments reports also the well scaling of the timing jitter with the square root of the number of junctions in the JTL. This affirmed the hypothesis to model the thermal

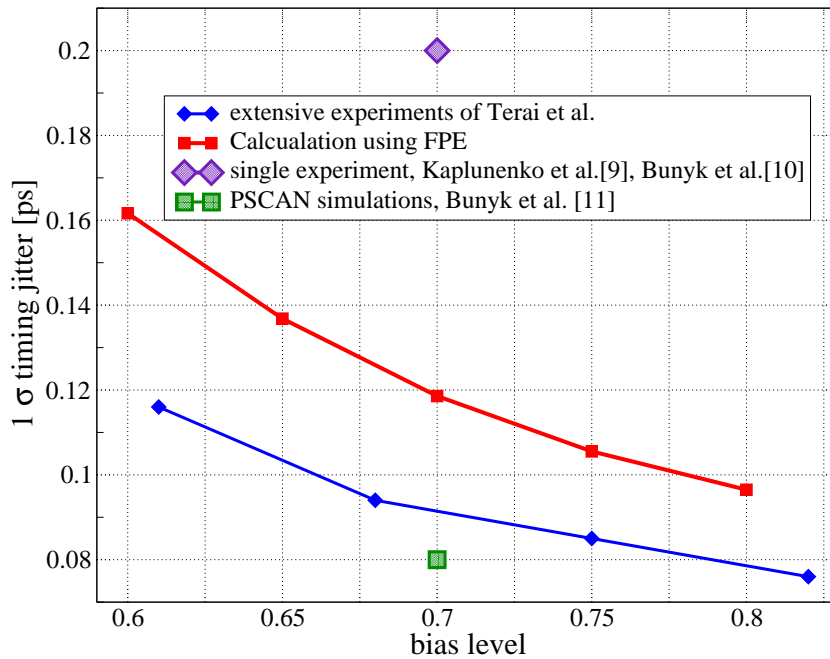


Fig. 5. Timing jitter of for the SFQ pulse transfer for one Josephson junction.

noise as a superposition of independent Gaussian white noise sources for every junction. Fig. 5 shows this measurements together with our new calculated results based on the FPE. We calculated a timing jitter of about $\sigma=0.12\text{ps}$ for one Josephson junction. The deviation between our calculations and the measurements of Terai et al. [12] can be explained by the different circuit parameters used in the experimental setup [13]. The different behavior of intrinsic and external shunted junction can also bring a certain contribution to the timing jitter of the junctions [14]. We plan a further analysis of the exact structure used in this experiments [15]. The decreasing of the timing jitter versus increased bias level can be mostly explained by the similarly decreased average time delay for transferring the pulse from one junction to the next. The relative timing jitter varies only from 2.4% to 2.05% of the transfer time using bias levels from 0.6 to 0.8, respectively.

CONCLUSIONS

The analysis of the stochastic dynamic by using Fokker-Planck equations has been used in the past for the calculation of static and dynamic error rates. Due to the exponential decreasing, these error sources are not the main problem for lower temperatures, but the third type of switching errors, the timing jitter, becomes very important for low temperatures [16]. Our previous suggested method is also providing all necessary data for the timing analysis of RSFQ logic cells. Even in the case of low temperatures, switching time variations are still large and cause timing errors in medium and large scale devices. The new possibility of calculating this timing conditions allows furthermore the modification of cells during the design process to reduce their jitter. This information is also an important part for the high level cell description in HDL-level simulations.

References

- [1] K.K. Likharev and V.K. Semenov, "RSFQ Logic/Memory Family: A New Josephson-Junction Technology for Sub-Terahertz-Clock-Frequency Digital Systems," *IEEE Trans. Appl. Superconductivity*, vol. 1, no. 1, pp. 3–28, 1991.
- [2] A.V. Rylyakov and K.K. Likharev, "Pulse Jitter and Timing Errors in RSFQ Circuits," *IEEE Trans. Appl. Superconductivity*, vol. 9, no. 2, pp. 3539–3544, 1999.
- [3] H. Toepfer, Th. Ortlepp, H.F. Uhlmann, D. Cassel, and M. Siegel, "Design of HTS RSFQ circuits," *Physica C*, vol. 392-396, pp. 1420–1425, 2003.
- [4] Th. Ortlepp, *Dynamical Analysis of Stochastic Influences in Superconducting Electronics*, Ph.D. thesis, Technical University of Ilmenau, Germany, 2004.
- [5] "JeSEF foundry for superconducting electronics at IPHT Jena Germany, RSFQ design rules," www.ipht-jena.de.
- [6] J. Nitta, A. Matsuda, and T. Kawakami, "Soliton Propagation Properties in a Josephson Transmission Line," in *Proceedings of the Seventh Kyoto Summer Institute, 27.-31.8.1984, Kyoto, Japan, 1984*, pp. 262–265.
- [7] E. Trias, J.J. Mazo, Falo F., and T.P. Orlando, "Depinning of kinks in a Josephson-junction ratchet array," *cond-mat/9911454*, 1999.

- [8] Waterloo Inc., *Computer algebra system MAPLE*, Release 6.1, 2001.
- [9] V. Kaplunenko and V. Borzenets, "Time Jitter Measurement in a Circular Josephson Transmission Line," *IEEE Trans. Appl. Superconductivity*, vol. 11, no. 1, pp. 288–291, 2001.
- [10] P. Bunyk and D. Zinoviev, "Experimental Characterization of Bit Error Rate and Pulse Jitter in RSFQ Circuits," *IEEE Trans. Appl. Superconductivity*, vol. 11, no. 1, pp. 529–532, 2001.
- [11] P. Bunyk and P. Litskevitch, "Case Study in RSFQ Design: Fast Pipelined Parallel Adder," *IEEE Trans. Appl. Superconductivity*, vol. 9, no. 2, pp. 3714–3720, 1999.
- [12] H. Terai, Z. Wang, Y. Hashimoto, S. Yoroza, A. Fujimaki, and N. Yoshikawa, "Timing jitter measurement of single-flux-quantum pulse in Josephson transmission line," *Appl. Phys. Letters*, vol. 84, no. 12, pp. 2133–2135, 2004.
- [13] S. Yoroza, Y. Kameda, H. Terai, A. Fujimaki, T. Yamada, and S. Tahara, "A single flux quantum standard logic cell library," *Physica C*, vol. 378-381, pp. 1471–1474, 2002.
- [14] Th. Ortlepp and F.H. Uhlmann, "Noise analysis for intrinsic and external shunted Josephson junctions," *Superconductor Science and Technology*, vol. 17, pp. S112–S116, 2004.
- [15] H. Terai, *personal communications*, via email, 2004.
- [16] Th. Ortlepp and H.F. Uhlmann, "Noise induced timing jitter: A general restriction for high speed RSFQ devices," *IEEE Trans. Appl. Superconductivity*, vol. 15, no. 2, pp. 344–347, 2005.

Authors:

Dr.-Ing. Dipl.-Math. Th. Ortlepp and Prof. Dr.-Ing. habil. F. H. Uhlmann
Department of Information Technology,
University of Technology Ilmenau,
P.O. Box 100565,
D-98684 Ilmenau, Germany
telephone: +49 3677 691185,
fax: +49 3677 691152,
email: thomas.ortlepp@tu-ilmenau.de