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Design Aspects of Complex Asynchronous RSFQ Digital Circuits

INTRODUCTION

Since 1948, when the first transistor has been invented, the semiconductor technique holds its exponential progress in terms of speed, integration, feature size miniaturization, and gaining of newer, deeper, and more essential applications in the people's life [1]. The huge computational power and the enormous data transfer of the modern semiconductor-based computer networks are the main factors pushing ahead the progress in all branches of the science and the industry. Nevertheless, the continuous growth of the performance of the semiconductor computers is accompanied by several factors currently limiting the progress of the high-integrated semiconductor electronics. According to the authoritative forecast [1], the decreasing of the feature sizes of the silicon chips will continue with the same speed, but the previously exponential growth of the clock frequency will slow. The reason for this is the fact, that the dominant part of the clock interval of the modern silicon chips is taken by the recharging of the interconnects' capacitances by the output currents of the gates, and only a small part - by the intrinsic switching speed of the transistors. Because, contrary to the transistors, the miniaturization of the interconnects does not enhance their performance, the speeding up of this recharging process proportionally increases the total dissipated power density [2]. The overcoming of all these factors restricting the future progress of the semiconductor electronics requires the involving of the newest technological solutions and a huge human power for R&D, which finally results into enormous amount of money for reinvestments. This has motivated the search for alternative techniques allowing more efficient (in terms of speed and price) digital information processing.

A promising candidate for this is the **L**ow-**T**emperature **S**uperconductive (LTS) electronics based on the Josephson effect. A drastic step towards the increase of its operation speed has been done in 1985 by a team of Russian scientists, which suggested an entirely new approach [3] to Josephson junction computing. There, the binary information is carried by picosecond voltage pulses instead of by voltage levels. These pulses are named ***S**ingle **F**lux **Q**uantum (SFQ)* pulses due to their quantized area:

$$\int_0^\infty U(t) \cdot dt = \Phi_0 , \qquad (1)$$

with Φ_0 = 2.07mV·ps – the single flux quantum. Thus, the binary information can be naturally generated, stored, and reproduced. The switching element of this technique is the overdamped Josephson junction having nonlinear and nonhysteretic I-V curve. This logic has been named ***R**apid **S**ingle-**F**lux **Q**uantum (RSFQ)* logic and even at that time operation frequencies up to 30GHz have been reached [4]. Currently, all superconductive digital circuits are based on the RSFQ technique. Within the modern roadmaps for electronics [1], this technique is considered as a promising alternative to

the semiconductor logic not only for development of supercomputers, but also for many advanced applications like space technologies, telecommunications, medical science, quantum computing, etc. Its unique features are [5]:

- extreme low power consumption - the energy dissipated during one switching of a single Josephson junction is of order of 10^{-19} Joule, while the signals are communicated via superconductive (i.e. lossless) transmission lines. Thus, the problem with the extreme large power dissipation of the high-integrated semiconductor digital circuits [2] could be overcome;
- extreme high operation speed achieved with relatively large lateral dimensions - simple digital RSFQ circuits with micrometer features sizes operating over 100GHz have been demonstrated long ago [6-11];
- intrinsically digital data representation - due to the nature of the flux quantization (see (1)), the different binary states are inherently defined.

Nevertheless, the RSFQ electronics still suffers from the lack of a real large-scale application. Only few successful middle-scale RSFQ devices have been reported up to now [12-13], operating at clock frequencies of only few tens GHz. The big gap between the speed performance of the simple and the middle-scale RSFQ digital devices is tightly connected to the complicated global clock distribution network of the complex synchronous RSFQ digital circuits. A significant part of the total circuitry of any synchronous RSFQ middle-scale application [12-13] belongs to the clock distribution network, which leads to three negative consequences:

- a great amount of the total dc bias current is consumed by the clocking. The large dc bias current consumption leads to parasitic magnetic fields, which can disturb the operation of the computational RSFQ electronics. Additionally, the transport of the huge dc bias current imposes hard requirements about the interface between the superconductive RSFQ chip and the normal-conductive supply network. Both effects restrict the integration level of the RSFQ digital devices;
- the global clock distribution network complicates significantly the RSFQ layouts, often requiring "critical" structures (like crossings, vias, etc.), which may lead to parasitic interactions and provoke fabrication faults, thus diminishing the fabrication yield;
- as demonstrated in [14], the spread of the fabrication technology parameters leads to instability of the time-domain characteristics of the produced RSFQ circuits. Within the complex clock distribution network of the high-integrated synchronous RSFQ applications, this effect causes a jitter of the clock signal appearance at the different parts of the chip. The latter restricts the minimization of the global clock interval, i.e. the high-speed performance of the large-scale synchronous RSFQ circuit.

All these negative effects can be more or less overcome by quantitative improvements of the currently existing RSFQ fabrication technologies and by application of new approaches for the design of high-integrated RSFQ digital circuits [15-16]. Nevertheless, the design of large synchronous RSFQ circuits meets the speed of light as a fundamental physical limitation about the global synchronization. Generally, the problem with the increasing the global clock frequency is equivalent to reducing the geometrical size of the synchronous circuit [17], i.e. the product of the feature sizes and the clock frequency can be regarded as a quantitative estimation of the global synchronization problems within the densely packaged digital circuits realized with a given fabrication

technology. About the modern semiconductor CPUs (feature sizes below 100nm; clock frequency of several GHz), the global clock synchronization already imposes very hard restrictions towards the further increasing of the speed and the circuit complexity [1], [17-19]. The modern LTS RSFQ fabrication technologies have feature sizes of few μm and intend clock frequencies of the large-scale applications above 100GHz, i.e. their product "feature sizes" × "clock frequency" is of order of 1000 greater than the one of the modern semiconductor CPUs. Therefore, the realization of a synchronous RSFQ digital circuit having multigigahertz clock frequency and even approaching the complexity of the nowadays semiconductor electronics is unimaginable with the present LTS RSFQ fabrication technologies [20].

A promising opportunity to overcome all these problems is given by the asynchronous circuit design. According to [21], an *asynchronous circuit* is a digital circuit, in which each component reacts to changes on its inputs as these changes arrive, and produces changes on its outputs when it concludes its computation. No clock signal is provided to synchronize the work of the circuit's components, and the coordination between them is performed by some kind of handshaking protocol. The asynchronous design approach offers several important advantages:

- Low power consumption - transients occur only in the circuit parts involved in the current computation, instead of at all circuit nodes at each clock interval;
- High operation speed - each computation is completed in the time needed for that particular computation, and not for the worst case. Thus, the operating speed is determined by the local latencies, not by the global worst-case latency;
- Reduced emissions of electromagnetic noise - the transitions occur at random places and at arbitrary time;
- Reduced sensitivity towards environment variations (like supply voltage, temperature, technology process, etc.) - designing synchronous circuits, one must assume that the worst possible combination of factors is present, and to clock the circuit accordingly. If this timing assumption is violated, the correct operating of the synchronous circuit fails. This is not the case by the asynchronous circuits - if properly designed, they run as fast as the current physical properties allow;
- No global synchronization - in this way, all problems originating from the global clocking are solved.

Nevertheless, the popularity of the asynchronous logic approach is quite restricted, mainly due to the lack of design techniques and supporting CAD tools. In this paper, we present our novel concept for high-level synthesis and optimization of asynchronous RSFQ digital circuits, which has been implemented into a software tool for their design and verification [22].

HIGH-LEVEL DESIGN OF ASYNCHRONOUS RSFQ DIGITAL CIRCUTS

Two kinds of design flow for digital circuits should be distinguished - for small-scale (up to several tens of switching elements) and for medium- and large-scale circuits. Their diagrams are given in Fig.1 and Fig.2, respectively.

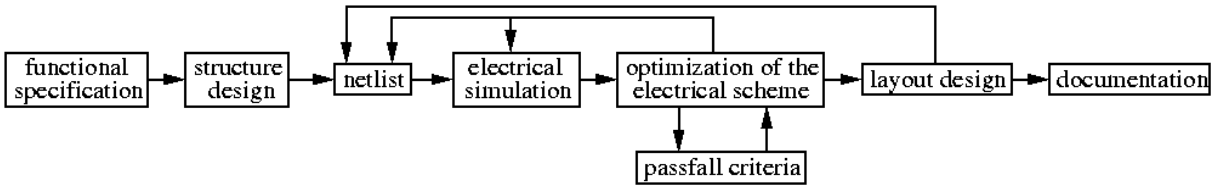

Fig.1 Design flow for small-scale digital circuits

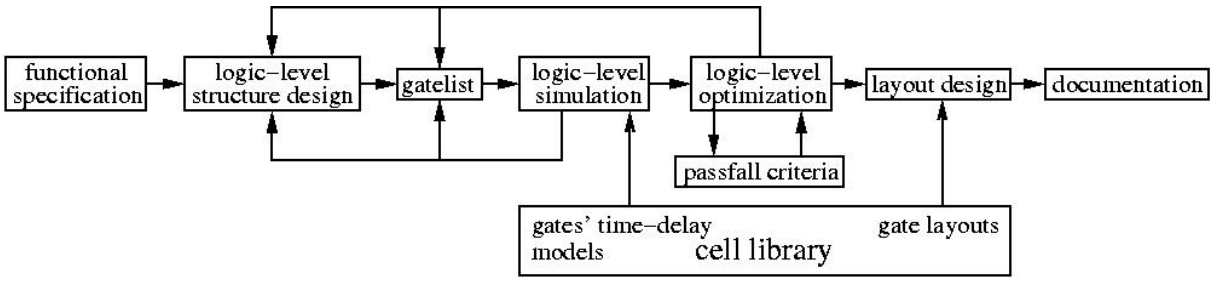

Fig.2 Design flow for medium- and large-scale digital circuits

In the case of a small-scale design, the desired functionality of the circuit is specified at first. It determines the topology of the circuit, and this topology is transformed into an electrical netlist, which is simulated with a transient electrical simulator. This step ends with a netlist of a correctly operating electrical scheme of the designed circuit. Next, the elements' values of this scheme are optimized with the goal to obtain the highest probability for correct operation of the fabricated circuit despite the fabrication process deviations. Subjected to the used optimization strategy, different sets of elements' values are generated, substituted in the netlist, and then electrically simulated. Passfall criteria distinguishing between correct and incorrect electrical behaviour of the circuit estimate each generated set. Once the optimum set of elements' values is found, they are implemented into a physical layout of the circuit. Important part of this step is the exact extraction of all parasitics. They should be included into the circuit netlist, thus shifting the elements' values out of the optimal point. New simulations and reoptimization of the circuit are then performed. Finally, a complete circuit specification should be done; otherwise the circuit cannot be properly used for high-level synthesis.

The same design flow could be performed also about medium- and large-scale digital circuits, but two negative effects become pronounced in this case:

- the time consumed for each transient electrical simulation run increases proportionally to the number of the elements of the electrical scheme;
- due to the larger number of optimized parameters, the total number of simulation runs performed during the optimization becomes extremely large.

Both effects burst into an enormous computational time needed for the optimization, and make the small-scale design flow ineffective about medium- and large-scale circuits. This problem can be solved by the cell-orientated design - a given set of blocks, designed and optimized in advance, is used to construct the complex digital circuit. In this case, the synthesis, the simulation, the optimization, and the layout design are performed at logic level, not at electrical one (see Fig.2). The latter results into much faster and efficient design procedure.

It begins again with the functional specification of the circuit, which is decomposed into a logic-block diagram instead of into electrical scheme. Thus, the high-level structure of the circuit is determined. The logic models of the building blocks (gates) are taken from a chosen cell library. Its components should be carefully optimized and adapted to the specifics of the used data coding and fabrication foundry. For our asynchronous RSFQ designs, we use the cell library [23], which is based on the dual-rail data coding [20-21] and the 4μm 1kA/cm^2 Nb/Al_2O_3-Al/Nb fabrication technology of PTB Braunschweig [24]. The obtained netlist of gates is tested by simulations for correct logical functionality. In the case of asynchronous RSFQ designs, this is a specific and difficult step, which we will consider in details in the next Section. If logical misfunctionality occurs, it should be avoided by changes within the circuit's gatelist and/or its logic-level decomposition. Once the correct logical operation is obtained, the designer begins with the logic-level circuit optimization. The logic-level optimization procedure depends strongly on the type of the designed digital logic. In the case of synchronous logic, it is subjected mainly to timing considerations (like delays, hold- and set-up time, etc.), while in the case of asynchronous logic, it includes also speed optimization, time-delay tuning, etc. (will be also discussed in the next Section). After the logic-level optimization is finished, the layout design is performed. If the layouts of the cell library components are designed correctly, this step is relatively simple and can be easily automated. A complete documentation of the resulting complex digital circuit should be done at the end of the design process.

LOGIC-LEVEL SIMULATION AND OPTIMIZATION OF ASYNCHRONOUS RSFQ DIGITAL CIRCUTS

The logic-level asynchronous RSFQ design meets several classes of problems restricting the development of complex digital circuits. The first one originates from the unique data coding within the RSFQ technique. The SFQ data are carried by picosecond voltage pulses (1) instead of voltage levels as by the classical semiconductors. However, all established tools for high-level design are addressed to the semiconductor electronics, i.e. are not compatible with the SFQ data coding.

The basic idea of our solution of this class of problems is to use a general purpose logic level description language for digital devices and to adapt it to the specifics of the asynchronous RSFQ electronics. Such powerful commercial tool is ModelSim, which offers **V**ery high speed integrated circuit **H**ardware **D**escription **L**anguage (VHDL) simulation [25]. We have developed a special approach for VHDL modelling of SFQ data exchange, which is described in [22] in details. Based on it, VHDL models of all components of our asynchronous RSFQ cell library [23] have been developed.

Another class of problems originates from the nontrivial time-domain features of the complex asynchronous digital circuits. Generally, any asynchronous circuit can be designed as delay-insensitive, i.e. to operate correctly for any time delays of its components. For this, a handshaking feedback should connect each pair of communicating units. This, however, results into extremely complicated circuit topology and reduced operation speed, making the delay-insensitive synthesis impractical about the high-speed large-scale digital designs.

In order to obtain faster asnychronous circuits having simpler topologies, certain timing constraints should be applied on their components. Any violation of these constraints

leads to a wrong circuit operation and should be eliminated during the design process. If taken from an optimized cell library (see Fig. 2), these components have fixed time delays, which may not correspond to the imposed timing constraints. Therefore, we have developed a novel technique for RSFQ delay manipulation. As described in [26], this is done by scaling of the external shunt resistors of the Josephson junctions, thus changing their Stewart-McCumber parameter β_c. In this way, the time delay of the gate is tuned without deteriorating its other parameters. The latter has already been verified experimentally in [27], making this technique a powerful tool facilitating the design of complex asynchronous RSFQ digital circuits.

Finally, we consider the time-domain instability of the asynchronous RSFQ gates. An important source for it is the parameter spread of the fabrication process. The latter is influenced by many and typically uncorrelated factors, shifting all circuit parameters (and also the time delay) out of their expected nominal values. This effect [28] can be neither exactly determined, nor influenced during the design phase. In case of synchronous applications, a certain margin is usually included into the clock interval to compensate all such time-domain deviations. This strategy, however, is not applicable in the asynchronous case.

To solve this problem, we have developed a novel approach for statistical modelling of RSFQ delays, described in details in [14]. We generate many (typically over 100 000) sets of circuit parameters, each one independently subjected to a Gaussian distribution with a mean value equal to the nominal parameter's value taken from the cell library, and a standard deviation specified by the fabrication technology. In this way, the stochastical nature of the technological spread is represented adequately. Next, a circuit netlist is generated from each set and is simulated with a Josephson junction circuit simulator. The obtained time-domain behaviour is estimated as working (good) or not operating (bad). In case of a working circuit, its time delay is automatically calculated. Finally, we build the delays' histogram and analyze it by the means of the statistics, thus deriving the mathematical model of the time-delay distribution of the RSFQ gate.

This approach allows also optimization of the time-domain behaviour of the asynchronous RSFQ gates. Contrary to the classical optimization strategies, where the aim is to adjust the circuit's parameters in order to maximize the gate's fabrication yield, the aim here is to minimize the time-delay spreads, keeping the fabrication yield reasonably large. For this, the nominal values of some properly chosen elements of the gate are varied, investigating the impact of this changing on the time-delay spread. For most of the gates of our cell library [23], we were able to shrink significantly the time-delay spread, while the yield remained still acceptable. This is described in [14] in details.

Based on our novel techniques for VHDL description of the SFQ data exchange and time-delay handling of the RSFQ digital circuits, we have developed an advanced high-level design flow for high-speed complex asynchronous RSFQ digital circuits (see Fig.3). It has been implemented into a software package for high-level simulation, verification, and optimization of asynchronous RSFQ digital circuits, which is presented in details in [22].

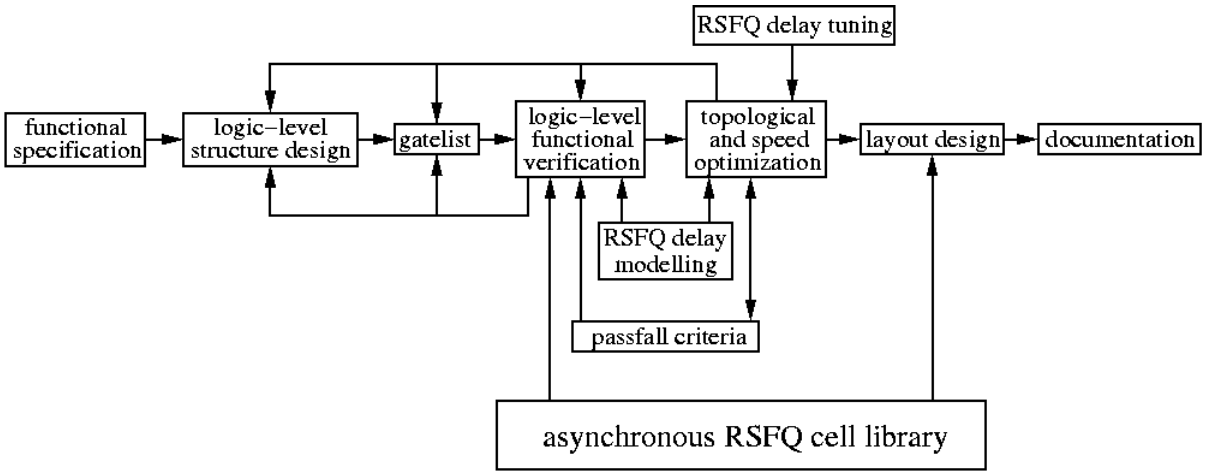

Fig.3 Advanced high-level design flow for complex asynchronous RSFQ digital circuits

CONCLUSIONS

Due to the large feature sizes of the currently existing fabrication technologies, the development of an ultra-fast large-scale RSFQ digital application is imaginable only if the asynchronous logic approach is used. In this paper, we have presented our concept for high-level synthesis and optimization of complex asynchronous RSFQ circuits. Very important parts of it are the novel methodologies for efficient tuning and exact statistical modelling of the time delays of the asynchronous RSFQ gates, whose ideas have already been verified experimentally. They allow the synthesis of faster complex asynchronous circuits with simplified topologies, which is impossible with the conventional design approaches. These novel techniques have been incorporated into a general purpose tool for high-level description and verification of logic circuits, which has been adapted to the specifics of the SFQ data coding. In this way, the synthesis of high-speed complex asynchronous RSFQ applications has been improved significantly.

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