

# 52. IWK

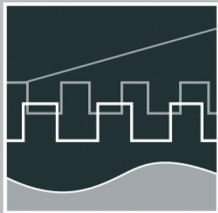
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## **FACULTY OF COMPUTER SCIENCE AND AUTOMATION**



## **COMPUTER SCIENCE MEETS AUTOMATION**

### **VOLUME II**

**Session 6 - Environmental Systems: Management and Optimisation**

**Session 7 - New Methods and Technologies for Medicine and  
Biology**

**Session 8 - Embedded System Design and Application**

**Session 9 - Image Processing, Image Analysis and Computer Vision**


**Session 10 - Mobile Communications**

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## Preface

Dear Participants,

Confronted with the ever-increasing complexity of technical processes and the growing demands on their efficiency, security and flexibility, the scientific world needs to establish new methods of engineering design and new methods of systems operation. The factors likely to affect the design of the smart systems of the future will doubtless include the following:

- As computational costs decrease, it will be possible to apply more complex algorithms, even in real time. These algorithms will take into account system nonlinearities or provide online optimisation of the system's performance.
- New fields of application will be addressed. Interest is now being expressed, beyond that in "classical" technical systems and processes, in environmental systems or medical and bioengineering applications.
- The boundaries between software and hardware design are being eroded. New design methods will include co-design of software and hardware and even of sensor and actuator components.
- Automation will not only replace human operators but will assist, support and supervise humans so that their work is safe and even more effective.
- Networked systems or swarms will be crucial, requiring improvement of the communication within them and study of how their behaviour can be made globally consistent.
- The issues of security and safety, not only during the operation of systems but also in the course of their design, will continue to increase in importance.

The title "Computer Science meets Automation", borne by the 52<sup>nd</sup> International Scientific Colloquium (IWK) at the Technische Universität Ilmenau, Germany, expresses the desire of scientists and engineers to rise to these challenges, cooperating closely on innovative methods in the two disciplines of computer science and automation.

The IWK has a long tradition going back as far as 1953. In the years before 1989, a major function of the colloquium was to bring together scientists from both sides of the Iron Curtain. Naturally, bonds were also deepened between the countries from the East. Today, the objective of the colloquium is still to bring researchers together. They come from the eastern and western member states of the European Union, and, indeed, from all over the world. All who wish to share their ideas on the points where "Computer Science meets Automation" are addressed by this colloquium at the Technische Universität Ilmenau.

All the University's Faculties have joined forces to ensure that nothing is left out. Control engineering, information science, cybernetics, communication technology and systems engineering – for all of these and their applications (ranging from biological systems to heavy engineering), the issues are being covered.

Together with all the organizers I should like to thank you for your contributions to the conference, ensuring, as they do, a most interesting colloquium programme of an interdisciplinary nature.

I am looking forward to an inspiring colloquium. It promises to be a fine platform for you to present your research, to address new concepts and to meet colleagues in Ilmenau.



Professor Peter Scharff  
Rector, TU Ilmenau



Professor Christoph Ament  
Head of Organisation



## Table of Contents



# CONTENTS

	Page
<b>6 Environmental Systems: Management and Optimisation</b>	
T. Bernard, H. Linke, O. Krol A Concept for the long term Optimization of regional Water Supply Systems as a Module of a Decision Support System	3
S. Röhl, S. Hopfgarten, P. Li A groundwater model for the area Darkhan in Kharaa river Th. Bernard, H. Linke, O. Krol basin	11
A. Khatanbaatar Altantuul The need designing integrated urban water management in cities of Mongolia	17
T. Rauschenbach, T. Pfützenreuter, Z. Tong Model based water allocation decision support system for Beijing	23
T. Pfützenreuter, T. Rauschenbach Surface Water Modelling with the Simulation Library ILM-River	29
D. Karimanzira, M. Jacobi Modelling yearly residential water demand using neural networks	35
Th. Westerhoff, B. Scharaw Model based management of the drinking water supply system of city Darkhan in Mongolia	41
N. Buyankhishig, N. Batsukh Pumping well optimi ation in the Shivee-Ovoo coal mine Mongolia	47
S. Holzmüller-Laue, B. Göde, K. Rimane, N. Stoll Data Management for Automated Life Science Applications	51
N. B. Chang, A. Gonzalez A Decision Support System for Sensor Deployment in Water Distribution Systems for Improving the Infrastructure Safety	57
P. Hamolka, I. Vrublevsky, V. Parkoun, V. Sokol New Film Temperature And Moisture Microsensors for Environmental Control Systems	63
N. Buyankhishig, M. Masumoto, M. Aley Parameter estimation of an unconfined aquifer of the Tuul River basin Mongolia	67

M. Jacobi, D. Karimanzira 73  
Demand Forecasting of Water Usage based on Kalman Filtering

## **7 New Methods and Technologies for Medicine and Biology**

J. Meier, R. Bock, L. G. Nyúl, G. Michelson 81  
Eye Fundus Image Processing System for Automated Glaucoma Classification

L. Hellrung, M. Trost 85  
Automatic focus depending on an image processing algorithm for a non mydriatic fundus camera

M. Hamsch, C. H. Igney, M. Vauhkonen 91  
A Magnetic Induction Tomography System for Stroke Classification and Diagnosis

T. Neumuth, A. Pretschner, O. Burgert 97  
Surgical Workflow Monitoring with Generic Data Interfaces

M. Pfaff, D. Woetzel, D. Driesch, S. Toepfer, R. Huber, D. Pohlers, 103  
D. Koczan, H.-J. Thiesen, R. Guthke, R. W. Kinne  
Gene Expression Based Classification of Rheumatoid Arthritis and Osteoarthritis Patients using Fuzzy Cluster and Rule Based Method

S. Toepfer, S. Zellmer, D. Driesch, D. Woetzel, R. Guthke, R. Gebhardt, M. Pfaff 107  
A 2-Compartment Model of Glutamine and Ammonia Metabolism in Liver Tissue

J. C. Ferreira, A. A. Fernandes, A. D. Santos 113  
Modelling and Rapid Prototyping an Innovative Ankle-Foot Orthosis to Correct Children Gait Pathology

H. T. Shandiz, E. Zahedi 119  
Noninvasive Method in Diabetic Detection by Analyzing PPG Signals

S. V. Drobot, I. S. Asayenok, E. N. Zacepin, T. F. Sergiyenko, A. I. Svirnovskiy 123  
Effects of Mm-Wave Electromagnetic Radiation on Sensitivity of Human Lymphocytes to Ionizing Radiation and Chemical Agents in Vitro

## **8 Embedded System Design and Application**

B. Däne 131  
Modeling and Realization of DMA Based Serial Communication for a Multi Processor System



M. Müller, A. Pacholik, W. Fengler Tool Support for Formal System Verification	137
A. Pretschner, J. Alder, Ch. Meissner A Contribution to the Design of Embedded Control Systems	143
R. Ubar, G. Jervan, J. Raik, M. Jenihhin, P. Ellervee Dependability Evaluation in Fault Tolerant Systems with High-Level Decision Diagrams	147
A. Jutmann On LFSR Polynomial Calculation for Test Time Reduction	153
M. Rosenberger, M. J. Schaub, S. C. N. Töpfer, G. Linß Investigation of Efficient Strain Measurement at Smallest Areas Applying the Time to Digital (TDC) Principle	159
<b>9 Image Processing, Image Analysis and Computer Vision</b>	
J. Meyer, R. Espiritu, J. Earthman Virtual Bone Density Measurement for Dental Implants	167
F. Erfurth, W.-D. Schmidt, B. Nyuyki, A. Scheibe, P. Saluz, D. Faßler Spectral Imaging Technology for Microarray Scanners	173
T. Langner, D. Kollhoff Farbbasierte Druckbildinspektion an Rundkörpern	179
C. Lucht, F. Gaßmann, R. Jahn Inline-Fehlerdetektion auf freigeformten, texturierten Oberflächen im Produktionsprozess	185
H.-W. Lahmann, M. Stöckmann Optical Inspection of Cutting Tools by means of 2D- and 3D-Imaging Processing	191
A. Melitzki, G. Stanke, F. Weckend Bestimmung von Raumpositionen durch Kombination von 2D-Bildverarbeitung und Mehrfachlinienlasertriangulation - am Beispiel von PKW-Stabilisatoren	197
F. Boochs, Ch. Raab, R. Schütze, J. Traiser, H. Wirth 3D contour detection by means of a multi camera system	203

M. Brandner Vision-Based Surface Inspection of Aeronautic Parts using Active Stereo	209
H. Lettenbauer, D. Weiss X-ray image acquisition, processing and evaluation for CT-based dimensional metrology	215
K. Sickel, V. Daum, J. Hornegger Shortest Path Search with Constraints on Surface Models of In-the-ear Hearing Aids	221
S. Husung, G. Höhne, C. Weber Efficient Use of Stereoscopic Projection for the Interactive Visualisation of Technical Products and Processes	227
N. Schuster Measurement with subpixel-accuracy: Requirements and reality	233
P. Brückner, S. C. N. Töpfer, M. Correns, J. Schnee Position- and colour-accurate probing of edges in colour images with subpixel resolution	239
E. Sparrer, T. Machleidt, R. Nestler, K.-H. Franke, M. Niebelschütz Deconvolution of atomic force microscopy data in a special measurement mode – methods and practice	245
T. Machleidt, D. Kapusi, T. Langner, K.-H. Franke Application of nonlinear equalization for characterizing AFM tip shape	251
D. Kapusi, T. Machleidt, R. Jahn, K.-H. Franke Measuring large areas by white light interferometry at the nanopositioning and nanomeasuring machine (NPMM)	257
R. Burdick, T. Lorenz, K. Bobey Characteristics of High Power LEDs and one example application in with-light-interferometry	263
T. Koch, K.-H. Franke Aspekte der strukturbasierten Fusion multimodaler Satellitendaten und der Segmentierung fusionierter Bilder	269
T. Riedel, C. Thiel, C. Schmallius A reliable and transferable classification approach towards operational land cover mapping combining optical and SAR data	275
B. Waske, V. Heinzl, M. Braun, G. Menz Classification of SAR and Multispectral Imagery using Support Vector Machines	281

V. Heinzl, J. Franke, G. Menz Assessment of differences in multisensoral remote sensing imageries caused by discrepancies in the relative spectral response functions	287
I. Aksit, K. Bunger, A. Fassbender, D. Frekers, Chr. Gotze, J. Kemenas An ultra-fast on-line microscopic optical quality assurance concept for small structures in an environment of man production	293
D. Hofmann, G. Linss Application of Innovative Image Sensors for Quality Control	297
A. Jablonski, K. Kohrt, M. Bohm Automatic quality grading of raw leather hides	303
M. Rosenberger, M. Schellhorn, P. Bruckner, G. Lin Uncompressed digital image data transfer for measurement techniques using a two wire signal line	309
R. Blaschek, B. Meffert Feature point matching for stereo image processing using nonlinear filters	315
A. Mitsiukhin, V. Pachynin, E. Petrovskaya Hartley Discrete Transform Image Coding	321
S. Hellbach, B. Lau, J. P. Eggert, E. Korner, H.-M. Gro Multi-Cue Motion Segmentation	327
R. R. Alavi, K. Brie Image Processing Algorithms for Using a Moon Camera as Secondary Sensor for a Satellite Attitude Control System	333
S. Bauer, T. Doring, F. Meysel, R. Reulke Traffic Surveillance using Video Image Detection Systems	341
M. A-Megeed Salem, B. Meffert Wavelet-based Image Segmentation for Traffic Monitoring Systems	347
E. Einhorn, C. Schroter, H.-J. Bohme, H.-M. Gro A Hybrid Kalman Filter Based Algorithm for Real-time Visual Obstacle Detection	353
U. Knauer, R. Stein, B. Meffert Detection of opened honeybee brood cells at an early stage	359

## 10 Mobile Communications

K. Ghanem, N. Zamin-Khan, M. A. A. Kalil, A. Mitschele-Thiel Dynamic Reconfiguration for Distributing the Traffic Load in the Mobile Networks	367
N. Z.-Khan, M. A. A. Kalil, K. Ghanem, A. Mitschele-Thiel Generic Autonomic Architecture for Self-Management in Future Heterogeneous Networks	373
N. Z.-Khan, K. Ghanem, St. Leistritz, F. Liers, M. A. A. Kalil, H. Kärst, R. Böringer Network Management of Future Access Networks	379
St. Schmidt, H. Kärst, A. Mitschele-Thiel Towards cost-effective Area-wide Wi-Fi Provisioning	385
A. Yousef, M. A. A. Kalil A New Algorithm for an Efficient Stateful Address Autoconfiguration Protocol in Ad hoc Networks	391
M. A. A. Kalil, N. Zamin-Khan, H. Al-Mahdi, A. Mitschele-Thiel Evaluation and Improvement of Queueing Management Schemes in Multihop Ad hoc Networks	397
M. Ritzmann Scientific visualisation on mobile devices with limited resources	403
R. Brecht, A. Kraus, H. Krömker Entwicklung von Produktionsrichtlinien von Sport-Live-Berichterstattung für Mobile TV Übertragungen	409
N. A. Tam RCS-M: A Rate Control Scheme to Transport Multimedia Traffic over Satellite Links	421
Ch. Kellner, A. Mitschele-Thiel, A. Diab Performance Evaluation of MIFA, HMIP and HAWAII	427
A. Diab, A. Mitschele-Thiel MIFAv6: A Fast and Smooth Mobility Protocol for IPv6	433
A. Diab, A. Mitschele-Thiel CAMP: A New Tool to Analyse Mobility Management Protocols	439

## 11 Education in Computer Science and Automation

S. Bräunig, H.-U. Seidel Learning Signal and Pattern Recognition with Virtual Instruments	447
St. Lambeck Use of Rapid-Control-Prototyping Methods for the control of a nonlinear MIMO-System	453
R. Pittschellis Automatisierungstechnische Ausbildung an Gymnasien	459
A. Diab, H.-D. Wuttke, K. Henke, A. Mitschele-Thiel, M. Ruhwedel MAeLE: A Metadata-Driven Adaptive e-Learning Environment	465
V. Zöppig, O. Radler, M. Beier, T. Ströhla Modular smart systems for motion control teaching	471
N. Pranke, K. Froitzheim The Media Internet Streaming Toolbox	477
A. Fleischer, R. Andreev, Y. Pavlov, V. Terzieva An Approach to Personalized Learning: A Technique of Estimation of Learners Preferences	485
N. Tsyrelchuk, E. Ruchaevskaia Innovational pedagogical technologies and the Information educational medium in the training of the specialists	491
Ch. Noack, S. Schwintek, Ch. Ament Design of a modular mechanical demonstration system for control engineering lectures	497



M. Müller / A. Pacholik / W. Fengler

## Tool Support for Formal System Verification

### Abstract

The design of complex real time systems requires verification within all stages of the development process. To ensure quality already in early design stages, formal verification has to be conducted on high abstraction levels and for potentially incomplete system definitions. In this paper we present an approach to formally verify the temporal behaviour of simulation models by introducing a tool chain based upon the system design environment MLDesigner and the verification tool UPPAAL.

### 1 Introduction

The design process of a complex embedded system aims to construct the right system in a correct way. To build the right system means to integrate the expected behaviour related to the users needs. This is ensured by simulation based validation [1]. For a system to be correct means, it is free of faults in a way, that specified properties can be ensured. This can be proved by formal verification [2].

Today simulation based validation is applied on system level, whereas verification is applied on implementation or block level. There are no techniques available to prove temporal properties in a high level validation model. A complete verification can only be conducted, if block level implementations are available. For example, SystemC is often proposed to be used for system level specifications. However, verification is either conducted dynamically, during simulations, or formally for SystemC models, for which RTL<sup>1</sup> code generation is possible. By the knowledge of the authors formal verification and constraint verification is not possible for generalized SystemC models.

To overcome this gap, we present a constraint driven approach to verify system level properties in early design stages. The verification flow realized in our work is depicted in Figure 1. The simulation model is supplemented with formal constraint information. Then this validation model is transformed into a verification model, which is used as input for a verification tool. Results from the verification tool can be back-annotated into the simulation model.

This paper is organized as follows. First related work is presented. Then we describe the verification flow and the transformation tool in detail. The paper ends with our conclusions and an outlook to the future work.

<sup>1</sup>Register Transfer Language

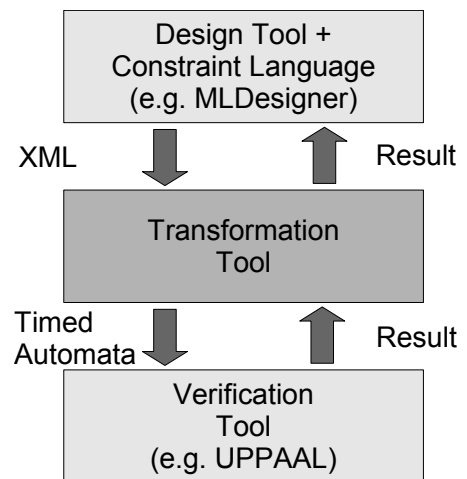


Fig. 1: Verification Flow

## 2 Related Work

Based on the requirements identified and proposals made in [3] an approach for verifying a system model's temporal properties has been developed. As proposed, a structured constraint language has been defined and the transformation of time constraint expressions to systems of timed automata has been developed and implemented in [4]. By exploring the state-space of resulting automata the verification of the time constraints can be conducted. The tool UPPAAL is supposed to be utilized for this verification.

Two approaches for designing the systems have been considered, using MLDesigner discrete event models, as proposed in [3], or UML activity, sequence and state diagrams, as proposed in [4]. The tool presented in this paper has implemented the MLD-based approach.

### 2.1 System Modelling

MLDesigner [5] is a tool based on the ideas of the Ptolemy project [6]. System models can be easily created by using existing customizable functional blocks and connecting them. New blocks can be created using the Ptolemy Language, a facility to describe functional blocks in terms of C++ code fragments. The tool MLDesigner organizes the structural connection, creation, execution and debugging of models. The tool provides the ability to link different models of computation within one system. This enables to create efficient simulation models, but limits the capabilities of implementation code generation.

According to the underlying ideas we can find a lot of similarities between SystemC 2.0 [7] and the MLDesigner Discrete Event (DE) modelling domain. A scheduler is used to organize the execution (simulation) of functional blocks. Timing information is added to the simulation in terms of delay. Data is exchanged using memories and/or pointers. Signals are event based, using the scheduler to inform the functional blocks. When describing hardware, there are some drawbacks according to hardware specific support (e.g. data types) compared to SystemC. In our opinion MLDesigner represents the more general approach on resource and systems modelling. Furthermore it provides powerful debugging opportunities according to the discrete event modelling approach.

The MLD system models are optimized for fast simulation speeds. Due to these optimizations (extensive use of pointers, abstract data types, simulation management, describing functional behaviour in terms of C++ code), it is hard to extract a state model to apply model checking techniques directly. In our approach we substitute the C++ code with timing constraints, a structured language defined in EBNF describing the behaviour based on events, abstracting from data structures. Of course, finite state modules (domain FSM) can be embedded in discrete event models (domain DE).

### 2.2 Constraint Languages

There are different ways to classify properties. One is to distinct between constraints and assertions where constraints are limitations to both the environmental behaviour (regarding to the inputs) and the expected system behaviour (regarding to system outputs) [8]. Another is to state all side effect free specifications as system constraints, as done in the Object Constraint Language (OCL) [9].

In this paper every specified behavioural property is named *constraint*. The role of such a property depends on the view on the system or its fragments. A property can be expected to be already fulfilled or asserted to be fulfilled by the current device under verification. Regarding to



the system modelling environment depicted above, we need to specify the use of (sub)systems within their environments. This includes to specify restrictions on inputs and outputs (safety properties), following called *specification constraints*. We also need to specify behavioural constraints between inputs and outputs, representing a (preferably minimal) subset of the systems expected behaviour, following called *implementation constraints*.

### 2.3 Verification Approach

There exist different kinds of models, that are suited for formal verification: clocked state models, timed automata, Petri nets, interval Petri nets, process algebra models, etc. These models provide different possibilities to model data, synchronization and timing. On the other side there are different, optimized internal data structures to represent state space and algorithms to apply state traversal and property checking, e.g. BDD<sup>2</sup> based symbolic verification. Because of the use of zero timed events in system models, we cannot use clocked state models. We need a state model involving timing in terms of clocks. Thus we decided to use timed automata, providing channel based communication, a synchronizing scheme, which is very similar to events. For verification we use the tool UPPAAL [10]. It provides a good support and is freely available.

## 3 Enhanced system models

Although well suited for developing event based behavioural system models, MLDesigner does not feature adequate means to describe the temporal behaviour of model elements [3]. So MLD model elements have to be artificially enhanced by Constraint Language expressions. There are four different model elements to be considered for applying temporal constraints: on one hand *System*, *Module* and *FSM* as complex (sub)model descriptions, on the other hand the subordinate model element *Instance*, which represents a functional part inside a complex model.

Of importance for model consistency is to keep the right *perspective*, when formulating the constraint expressions for a certain model element. This concept of perspective is originated in the design perspective of MLD, which limits the view to the elements residing in one hierarchical level and does neither provide nor require complete knowledge of the full model hierarchy. This has a major influence on the complexity of the event identifiers used within the constraint expressions.

Since the functional behaviour within a system is supposed to be provided by *Instance* blocks, they have to carry **implementation** constraint expressions, that describe the temporal dependencies between their input and output signals. The perspective is thereby limited to the boundaries of the particular instance.

The *System* and *Modules* as complex system definitions contain instances and their relations. The perspective is a *local perspective* set to the system's own hierarchical level, so the constraints expressed on this level have to be **specifications** related to the (sub)system's inner signals. Concerning verification the necessity may arise to make assertions on the occurrence of any signal from any instance on any subsystem level. So, for the *System* an additional *global perspective* needs to be defined, which exceeds the MLD provided view and requires knowledge of the complete model hierarchy. Here **global specification** constraints have to be formulated, that refer to signals throughout all model hierarchy levels.

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<sup>2</sup>binary decision diagram

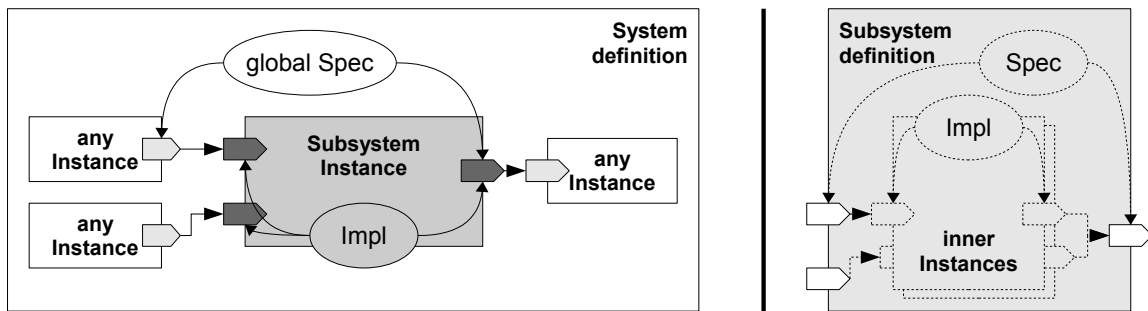


Fig. 2: MLD model elements and constraints

An *FSM* block contains an automaton structure (states and transitions). The perspective is limited to the boundaries of the FSM. The internal behaviour of an FSM depends on the *states*, so the **FSM implementation** constraints timing the state transitions are stored there. *Transitions* contribute to the internal behaviour by featuring *conditions* and *actions* - expressing the dependence of the transition from input events on one hand and the dependence of output events from transitions on the other.

The MLD modelling paradigm enables a once defined module or primitive to be instantiated in systems or modules various times on different hierarchy levels. Since the transformation produces a flat model, system wide unique identifiers have to be introduced. The concept of distinct constraint perspectives combined with respectively enhanced event identifiers eases the element handling and prevents conflicts on the resulting single system level.

#### 4 The tool MLD2UPPAAL

The tool MLD2UPPAAL conducts the transformation from the enhanced MLD model to the UPPAAL timed automata system by passing three main conversion stages. Two intermediate model formalisms have been developed to support the transformation and provide a basis for different model manipulations. A summary of this workflow is shown in Figure 3.

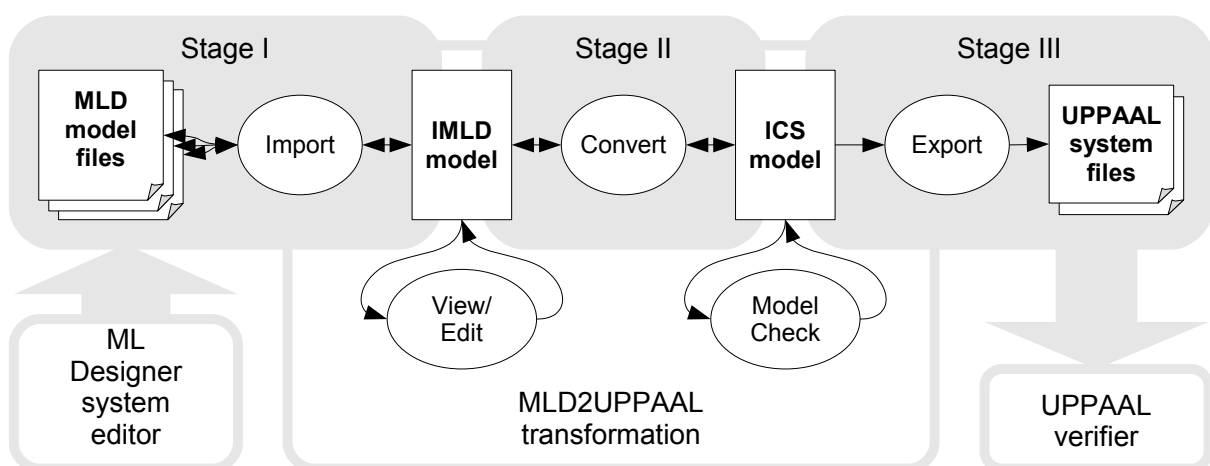


Fig. 3: MLD2UPPAAL workflow

Since an MLD model features a hierarchical structure, the model and each subsystem and element definitions are stored in separate files. In the first processing stage a given set of model

files, including the top level system file and all referenced files, are imported into an *Intermediate MLD Model (IMLD)* instance. Main purpose of this intermediate formalism is to join the MLD system and subsystem definitions into one model while maintaining the hierarchy information. At this stage the application allows varying the level of hierarchy resolution and the revision of the constraint expressions. As the workflow indicates, the original model definition is kept consistent to the intermediate models by backpropagating content changes. The second stage converts the intermediate MLD model into an instance of the *Intermediate Constraint System Model (ICSM)*. During this conversion the system structure is flattened, which results in the substitution of all subsystems according to whether they are to be resolved or not. Unresolved subsystems are treated as simple instance blocks with implementation constraints, whereas resolved subsystems instances are replaced by their inner structure and local specification constraints to provide assertions about that system partition. The ICS model notation allows the check of syntactic and semantic constraint consistency in consideration of the concept of perspective mentioned above. Once the check is completed successfully, the ICS model is transformed to timed automata using UPPAAL templates to map the constraint properties. An UPPAAL-compliant XML-notation is stored in model and query files, that serve as input for the UPPAAL verifier.

The tool is implemented as a Java application, that appears as shown in Figure 4, and was successfully tested against selected examples.

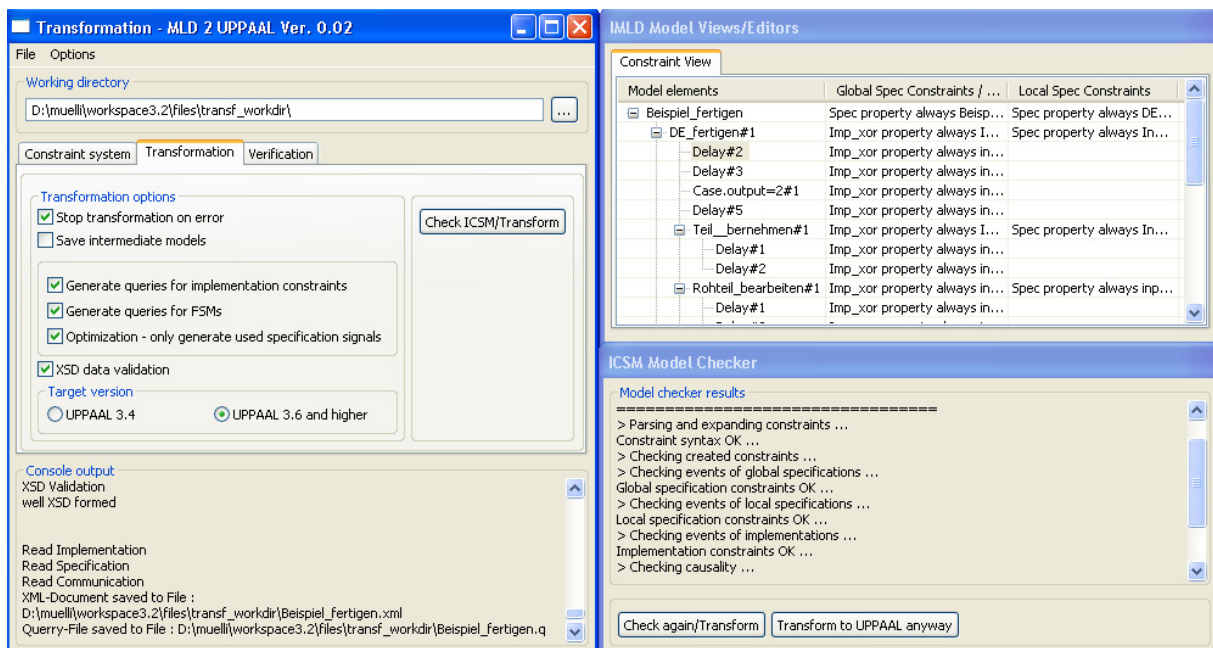


Fig. 4: MLD2UPPAAL screenshot

## 5 Conclusions and future work

By introducing the temporal constraint language and applying it to MLD designer system models we showed the possibility to add formally verifiable properties to models with high degrees of abstraction. The tool implemented in this work's context gives an example of how to bridge the gap between design and verification formalisms. Since it has been derived from the application framework introduced in [11], a customization to various design sources

and verification targets is easily possible. The given transformation of constraints to UPPAAL automata can be easily extended by adding custom templates. Currently we are going to apply our verification method to a number of design models to validate and benchmark it regarding model complexity. Using completely formally interpretable simulation models will make the models more directly verifiable and thus reduce the amount of additional information to be supplied in form of constraints. An according approach concerning extended finite temporal properties has already been presented in [12].

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